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Recent insights in direct extraction of access resistance components in NSFET and CFET devices with the cascaded transistor method

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In this work, we present recent insights into access resistance extraction based on a cascaded transistor test-structure. In the first part, we propose a new methodology to isolate the channel resistance component by varying the overdrive voltage. This procedure is applied to both n- and p-NSFET devices to analyze the impact of rapid thermal anneal treatment and inner spacer size variation, respectively. Results are assessed with both electrical measurements and TCAD simulations. In the second part, we present an upgraded cascaded transistor test-structure for CFET devices offering additional functionalities. Initial results are presented, analyzing the impact of the wiring scheme and the contact size. Finally, contact resistivity extraction is performed and compared to large transmission line test-structures for NSFET and CFET devices, respectively. © 2026 The Author(s). Published by IOP Publishing Ltd.

1. Introduction

A new method based on cascaded transistors (CASC) has been recently proposed[1)] and assessed via TCAD simulations[2)] to analyze the access resistance (R_{access}) components inside FinFET and nanosheet-FET (NSFET) devices (Fig. 1). We define as R_{access} all the resistive components that are not gate-controlled and are consequently limiting the ON-current inside FET devices. R_{access} can be separated into the contact resistance (R_{cont}), the source/drain resistance ($R_{S/D}$), and, possibly, an additional interface resistance (R_{int}) component when a heterojunction is present between S/D and channel.[3–5)] This is typically the case in pFET devices with SiGe S/D and Si channel.[6,7)] It has, however, been evidenced that R_{int} was minimized in Gate All Around devices (such as NSFET) as compared to FinFET devices because of the confined volume.[8)] Please note also that $R_{S/D}$ is typically composed of two contributions: the resistance of the epitaxial material (R_{epi}) and the resistance of the extension (R_{ext}). The extension area is the portion of the fin or nanosheet situated between the epitaxial material and the junction, wherein the diffused dopants from the epi represent the majority. As demonstrated in,[9)] this R_{ext} contribution can also be important inside NSFET devices. Finally, it is necessary to add the (gate-controlled) channel resistance (R_{ch}) that can be significant for NSFET devices (given the limited section of the channel) to these components that are limiting the ON-current.

With the continuous downscaling of FET devices and the advent of nanosheet-based devices from the 2-nm technological node (Fig. 2),[10,11)] S/D epitaxial volumes, channel sections, and contact sizes are further reduced, increasing $R_{S/D}$ and R_{cont}, respectively. Hence, the analysis and optimization of R_{access} components are critical steps to understand and improve device performance.[12–15)]

This paper is based on the work presented for the first time during the SSDM 2025 conference.[16)]

2. Results and discussion

2.1. Channel resistance extraction from overdrive sweep

A limiting factor of the extractions performed so far is that the gate-controlled channel resistance (R_{ch}) cannot be separated from the $R_{S/D}$ component. Typically, the channel contribution is minimized by performing the measurement at a large voltage overdrive (V_{OV}). However, as we move from FinFET towards NSFET, R_{ch} is not negligible anymore due to the limited section of the NS channel through which current is flowing. Hence, we have implemented an extraction methodology based on the overdrive sweep as introduced by Paul et al.[17)] for a simple FET device into our CASC test-structure.

This methodology was tested on a n-NSFET with a Contacted Poly Pitch (CPP) of 45 nm (also named Gate Pitch), a Gate Length (L_G) of 16 nm, Si:P epitaxial S/D, and a split on rapid thermal anneal (RTA) (no RTA versus 950 °C spike). The total R_{access} normalized per W_{eff} ($=2 \times$ NS width $+ 2 \times$ NS height) to cut off the potential impact of nanosheet dimensions, is drawn as a function of the number of cascaded transistors NCASC in Fig. 3(a). The die per die analysis of $R_{S/D+ch}$ (=slope) and R_{cont} (=intercept) is presented in Fig. 3(b), and the median R_{cont} and $R_{S/D+ch}$ components analysis in Fig. 3(c). For both samples, R_{cont} and $R_{S/D+ch}$ are extracted as a function of V_{OV} (Fig. 4(a)). For large V_{OV} (>0.8 V), R_{cont} is constant and, assuming $R_{S/D}$ is also constant, the only component varying with V_{OV} is R_{ch}. Hence, at large V_{OV}, R_{ch} can be extracted from the slope of R_{access} versus $1/V_{OV}$ (Fig. 4(b)). The resulting fully separated R_{access} components (Fig. 4(c)) illustrate the impact of RTA treatment: $R_{S/D}$ is reduced (due to enhanced doping activation in Si:P) and, consequently, R_{cont} is also reduced. The R_{ch} component is slightly reduced (due to increased diffusion reducing channel length) but remains dominant. These CASC results are in perfect

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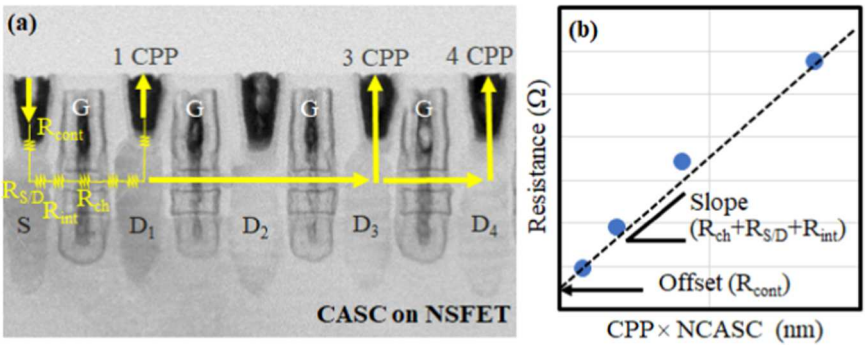

Fig. 1. (a) XTEM view of the CASC test-structure for NSFET with a schematic representation of the R_{access} components. (b) Extraction methodology. By measuring a series of adjacent transistors (NCASC) and plotting their $R_{ON,lin}$ as a function of the total length (NCASC × CPP), it is possible to extract R_{cont} (offset at NCASC × CPP = 0) and $R_{S/D}$+R_{epi}+R_{int} (slope R versus NCASC × CPP).

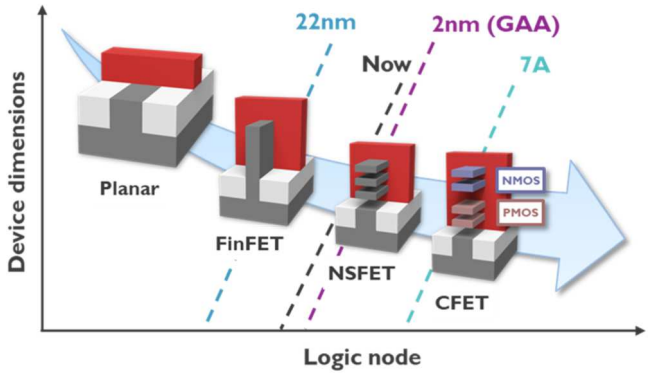

Fig. 2. Technology roadmap for logic devices from FinFET to Nanosheet-FET (NSFET) towards Complementary-FET (CFET) architectures.

agreement with the positive impact of the RTA treatment observed on the abs($I_{D,LIN}$)-(V_G-V_T) curves (Fig. 5(a)) measured on the device (CPP = 48 nm, LG = 16 nm). From I_{ON}-I_{OFF} clouds on the same devices (Fig. 5(b)), we nevertheless observe, in addition, that the OFF-current (I_{OFF}) is also increased in parallel with the ON-current (I_{ON}). Mechanisms taking place are described in detail in.[18] Typically, local Si_3P_4 clusters are present in the Si:P epi as grown, but they are not contributing to the electrical conductivity. During post-epi-growth RTA treatment, a fraction of the P atoms from these clusters are activated, while the remaining part moves into interstitial sites. This is producing both enhanced doping activation (enhancing I_{ON}) and P diffusion (degrading I_{OFF}).

We have also tested the methodology on a p-NSFET (CPP = 45 nm, L_G = 20 nm) with SiGe:B S/D and a split on the inner spacer (ISP) size (~4 nm for S1 versus 8 nm for S2), as illustrated in Fig. 6. When the ISP size is reduced, both $R_{S/D+int}$ and R_{ch} are reduced while R_{cont} remains constant. As illustrated in Fig. 6(c), the portion R_{ext} of $R_{S/D}$, which is drastically reduced, corresponds to the resistance component below the ISP. For a smaller ISP, epi is grown closer to the NS channel, which reduces the effective channel length and thus the R_{ch} components. These CASC results are in correct agreement with the abs($I_{D,LIN}$)-(V_G-V_T) curves (Fig. 7(a)) measured on the device (CPP = 48 nm, L_G = 19 nm), wherein an increase of $I_{D,LIN}$ can be observed for the small ISP. From I_{ON}-I_{OFF} clouds on the same devices (Fig. 7(b)), we can moreover observe that I_{OFF} is not degraded while I_{ON} is increasing.

To understand and model the impact of the ISP size, we have calibrated a TCAD simulation deck for these two p-NSFET devices employing Synopsys Sentaurus software.[19] The simulated structure device topology has been defined starting from TEM images (Contacted Poly Pitch, NS dimensions, Gate Length, S/D epi size and position, Local Interconnect size and position) (Fig. 8(a)). In Fig. 8(a), we present a 2D TCAD material map wherein ISP size is respectively equal to 8 nm (S1) and 4 nm (S2), as well as the 3D carrier distribution (Fig. 8(b)). XTEM view of similar p-NSFET samples with close dimensions is presented in the inset. The presence of traps between the SiN inner-spacers and the Si nanosheet is simulated by introducing donor traps at this interface. The density of interface traps

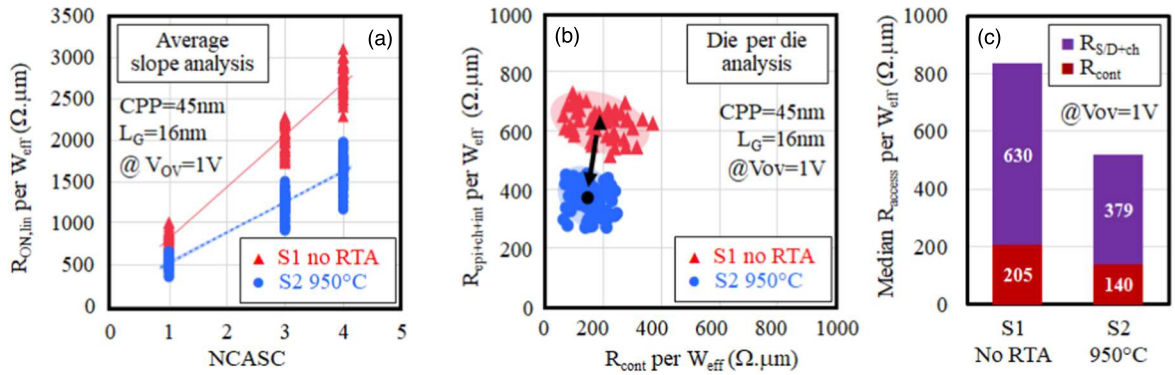

Fig. 3. (a) R_{access} as a function of NCASC for n-NSFET samples varying annealing (no RTA versus 950 °C) and median slope (b) Die per die and median R_{cont} and $R_{S/D+ch}$ (c) Median $R_{S/D+ch}$ and R_{cont} components illustrating the impact of RTA treatment.

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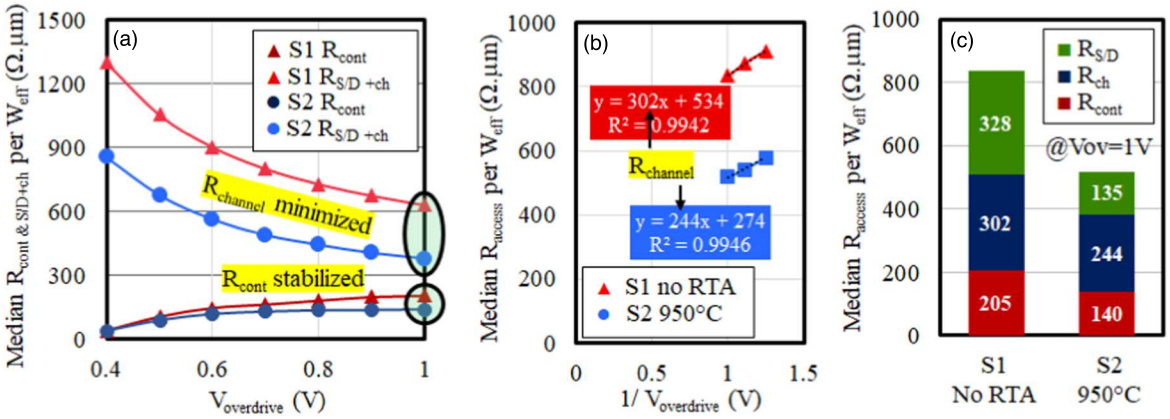

Fig. 4. (a) Median R_{access} components versus V_{OV} for n-NSFET samples. (b) R_{ch} extraction method from overdrive sweep. (c) Median $R_{S/D}$, R_{ch}, and R_{cont} components illustrating the impact of RTA treatment.

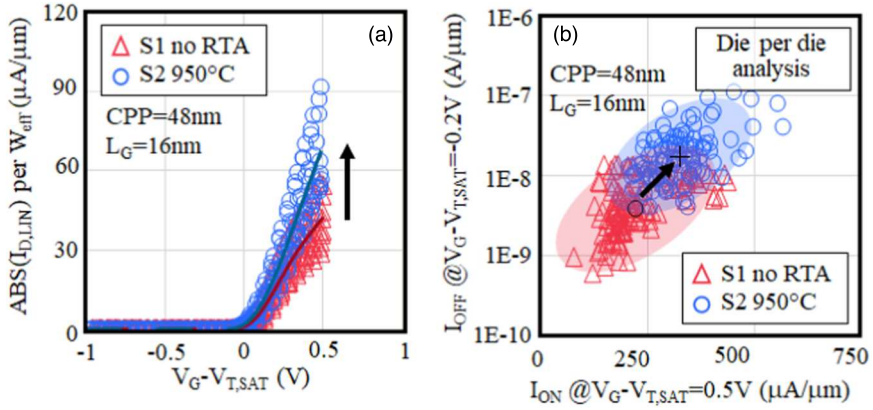

Fig. 5. (a) Die per die abs($I_{D,LIN}$)-V_G-V_T for n-NSFET samples varying annealing (no RTA versus 950 °C). (b) Die per die I_{ON}-I_{OFF} for n-NSFET of the same samples. A boost of I_{ON} as well as an increase of I_{OFF} with anneal are evidenced.

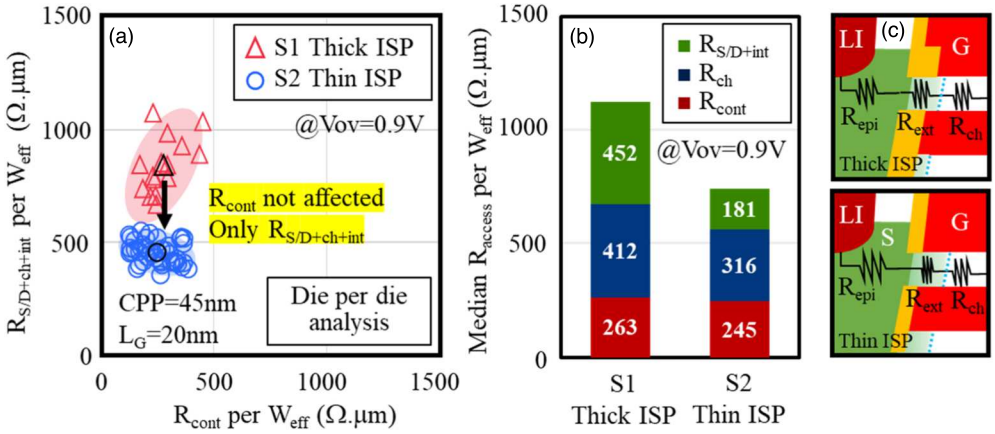

Fig. 6. (a) Die per die and median R_{cont} and $R_{S/D+int+ch}$ for p-NSFET samples varying inner spacer (ISP) size (S1 = 8 nm, S2 = 4 nm). (b) Median $R_{S/D+int}$, R_{ch}, and R_{cont} components at V_{OV} = 0.9 V. (c) Sketch illustrating the components of $R_{S/D}$ (=R_{epi}+R_{ext}) as well as the impact of ISP size.

(Dit) energy distribution within the silicon bandgap is simulated based on experimental results,[20] and the magnitude was scaled to reach 1×10^{13} cm^2eV^{-1} at 0.35 eV above the valence band energy, in line with previous studies.[9,21] The contact resistivity (ρ_{cont}) is also scaled to reach 2.5×10^{-8} $\Omega.cm^2$ based on previous experimental results and methodology.[22–24] By comparing the experimental and simulated I_D-V_G curves both in linear (LIN) and saturation (SAT) regimes, we can confirm the proper calibration of our TCAD deck (Fig. 9(a)). By simulating the LIN regime with $R_{cont} = 0$ (to isolate R_{cont} component) and using the voltage overdrive sweep method to isolate R_{ch}, we have been able to extract the different R_{access} components from our simulated $I_{D,LIN}$-V_G curves for S1 and S2, and to compare them with the experimental data (Fig. 9(b)). A nice qualitative agreement with experimental curves is obtained. TCAD results are evidencing the detrimental role of SiN/Si interface traps along the ISP (Fig. 9(c)). In addition to the overall $I_{D,LIN}$ improvement, the relative performance gap between the two samples with different ISP widths is significantly reduced when no traps are simulated. The 2D absolute net carrier (AbsNetCarrier) maps in Fig. 9(d), for both p-NSFET

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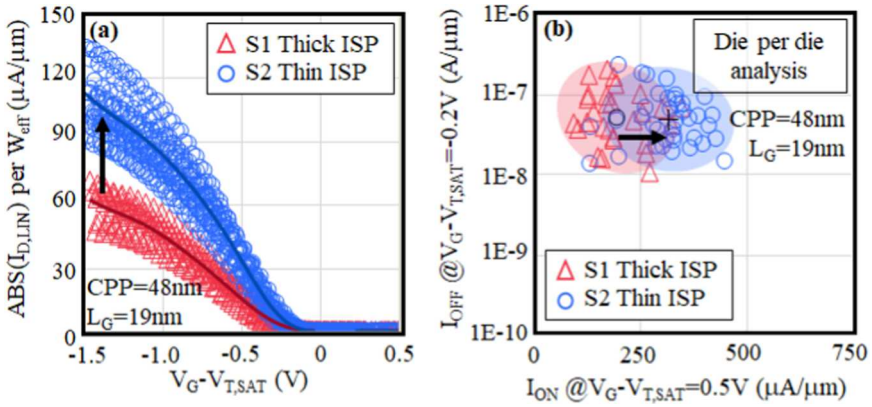

Fig. 7. (a) Die per die abs($I_{D,LIN}$)-V_G-V_T for p-NSFET samples varying ISP size (S1 = 8 nm versus S2 = 4 nm). (b) Die per die I_{ON}-I_{OFF} for p-NSFET of the same samples. Boost of I_{ON} for reduced ISP size is evidenced.

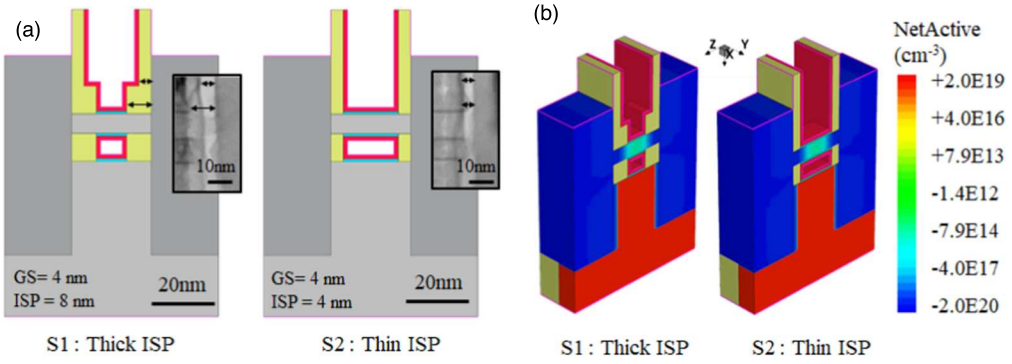

Fig. 8. (a) 2D TCAD material map for both p-NSFET samples varying ISP size (S1 = 8 nm versus S2 = 4 nm). (inset) XTEM view of the typical ISP variation split introduced (b) 3D TCAD Net Active Dopant map for the same samples.

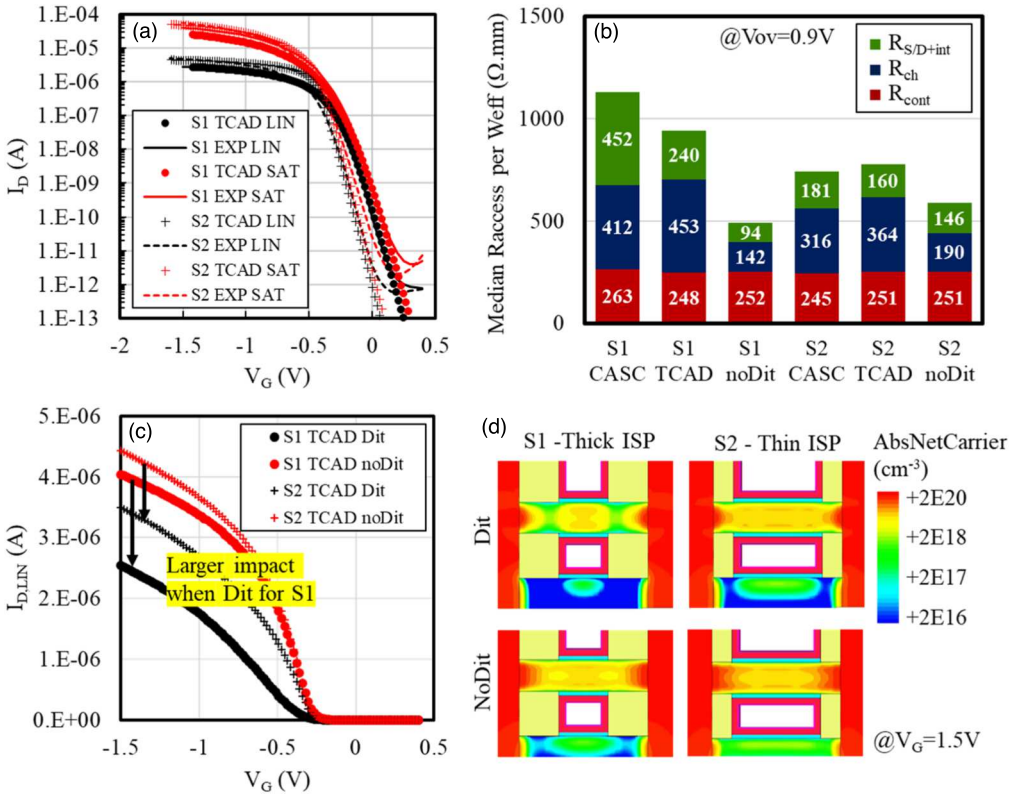

Fig. 9. (a) Median experimental and TCAD abs($I_{D,LIN}$)-V_G and abs($I_{D,SAT}$)-V_G for p-NSFET samples varying ISP size (S1 = 8 nm versus S2 = 4 nm). (b) $R_{S/D+int}$, $R_{ch,}$ and R_{cont} components from CASC, and TCAD (with and without Dit) at V_{OV} = 0.9 V (c) TCAD abs($I_{D,LIN}$)-V_G for both p-NSFET samples with and without interface traps. (d) 2D TCAD absolute net carrier (AbsNetCarrier) maps for both p-NSFET samples with and without interface traps at V_G=1.5 V.

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samples at $V_G = 1.5$ V, show that ISP/channel interface traps induce carrier depletion close to the gate edge at the ON-state. This effect is particularly pronounced in S1 (thicker ISP), due to the larger SiN/Si surface area and a larger portion of NS not covered by the gate. This has a major impact on R_{ext} (and hence $R_{S/D}$) as well as on R_{ch}, as evidenced in Fig. 9(b).

Improved performance (increased drive current) is obtained for the device with reduced ISP thickness. This approach can, however, lead to increased parasitic capacitance. Hence, alternative processing solutions to reduce trap densities at the spacer material/Si interfaces are another option, as discussed in.[9)]

2.2. New cascaded test-structure for access resistance analysis in CFET devices.

To further reduce the footprint of devices in layout, a new device architecture named complementary field-effect transistor (CFET) has been introduced as a successor to Nanosheet-FETs for future logic nodes.[25–28)] Exploiting the vertical dimension, CFET is composed of stacked n-type and p-type NSFET for CMOS logic operation. CFET can reduce the device area, but also offers high compatibility with conventional FinFET and NSFET fabrication processes. A novel CASC test-structure has been designed to measure both top and bottom devices inside CFET devices (Fig. 10).

Middle-of-line metal (MOL) resistances are continuously more detrimental in scaled device architectures.[29)] For this reason, the new test-structure has been designed with different MOL connection schemes. To evaluate this new capability, connections to a CFET top n-type device (CPP = 60 nm, $L_G = 22$ nm, M0 = 22 nm) from the front (TOF) and the bottom (TOB) were tested. The impact of the interconnects on the R_{cont} component is evidenced while the $R_{S/D+ch}$ component is maintained constant (Fig. 11). This can be explained by the smaller width of the via connecting M0T from the top (V0T) in TOF versus the larger width of the via connecting it top-down (V0TD) in TOB, as illustrated by the insets. This is leading to R_{cont} increase and larger die-to-die variability.

We have also studied a split on the contact size (M0 = 20 to 24 nm) on the same devices (Fig. 12) for the TOB interconnect scheme. Although the standard deviation across the wafer is significant, an evolution of the median R_{cont} can be extracted from the die per die analysis of R_{access} components, with a decrease of median R_{cont} observed for larger contact size. Note also that the die-to-die variability is larger for the smaller contact size. We estimate that this is linked to an increased difficulty in accurately controlling the contact size across the wafer for smaller contacts.

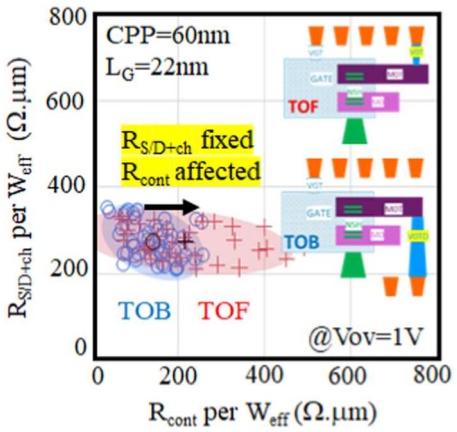

Fig. 11. Die per die and median R_{cont} and $R_{S/D+ch}$ for CFET samples for front (TOF) and bottom (TOB) connection schemes of the top n-type device (insets).

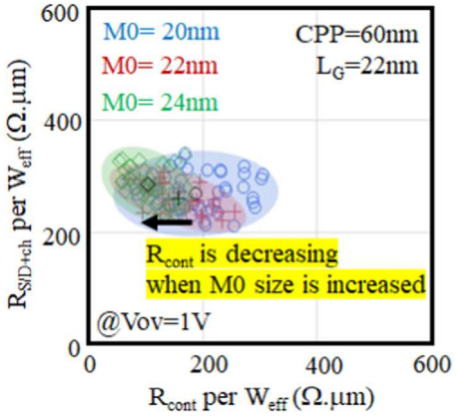

Fig. 12. Die per die and median R_{cont} and $R_{S/D+ch}$ for CFET top n-type devices (with TOB interconnect) varying M0 contact size (20, 22, and 24 nm).

Finally, a new methodology has been proposed to extract R_{ch} (see Fig. 10(b)), varying the CPP and L_G of the same (small) amount. Since the spacing between gates is maintained constant, R_{epi} and R_{cont} components are not varied, and the R_{ch} contribution can be isolated. The advantage of this concept is that R_{ch} can be extracted for small V_{OV} values and analyzed as a function of V_{OV}. In Fig. 13, the R_{access} components of a CFET top n-type device were analyzed with this concept (for CPP = 60 nm and $L_G = 22$ nm versus CPP = 64 nm and $L_G = 26$ nm). The decrease of R_{ch} with

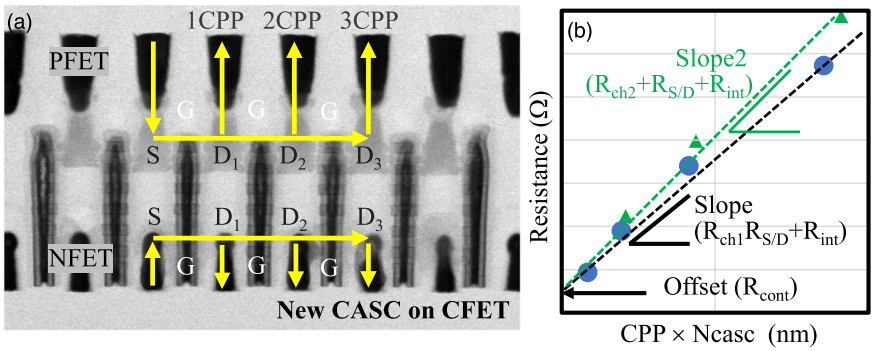

Fig. 10. (a) XTEM view of the CASC test-structure for CFET with a schematic representation of the R_{access} components. (b) Extraction methodology as explained in Fig. 1. On this new version of the CASC, R_{ch} can moreover be isolated by varying the CPP and LG by the same amount.

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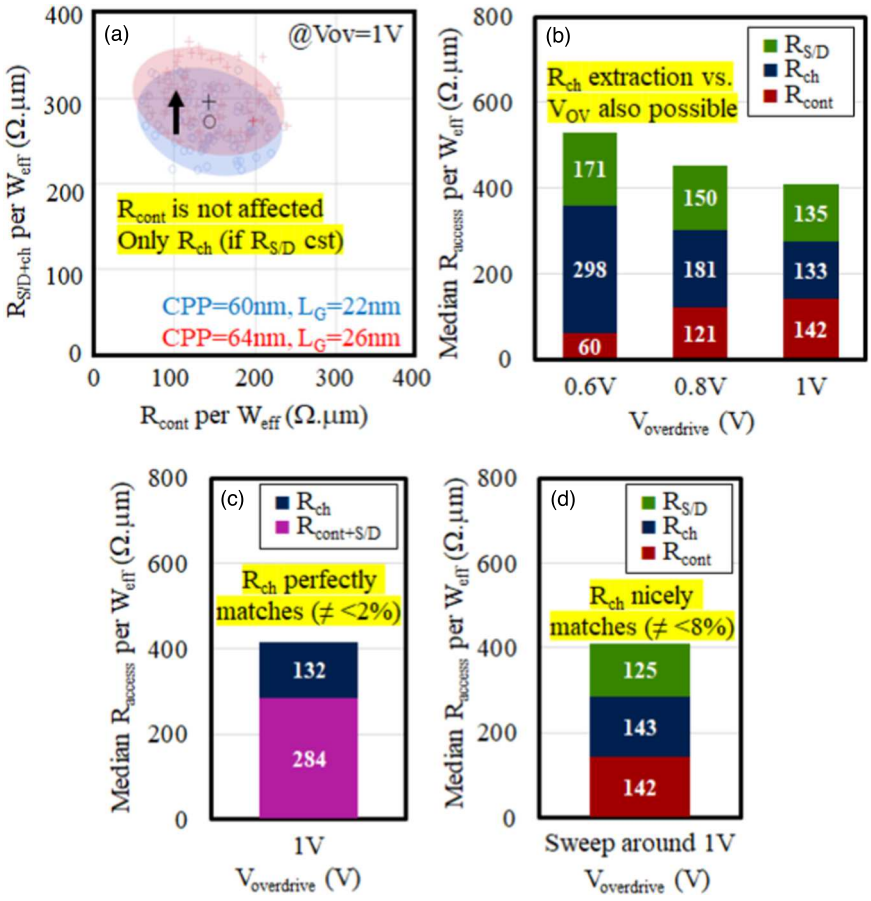

Fig. 13. (a) Die per die and median R_{cont} and $R_{S/D+ch}$ for CFET top n-type devices for CPP = 60 nm, L_G = 22 nm and CPP = 64 nm, L_G = 26 nm. (b) Median $R_{S/D}$, $R_{ch,}$ and R_{cont} components (at V_{OV} = 0.6, 0.8, and 1 V). (c) Classical extraction of R_{ch} on transistor at V_{OV} = 1 V. (d) Median $R_{S/D}$, $R_{ch,}$ and R_{cont} components extracted on the same device with overdrive sweep methodology (around V_{OV} = 1 V).

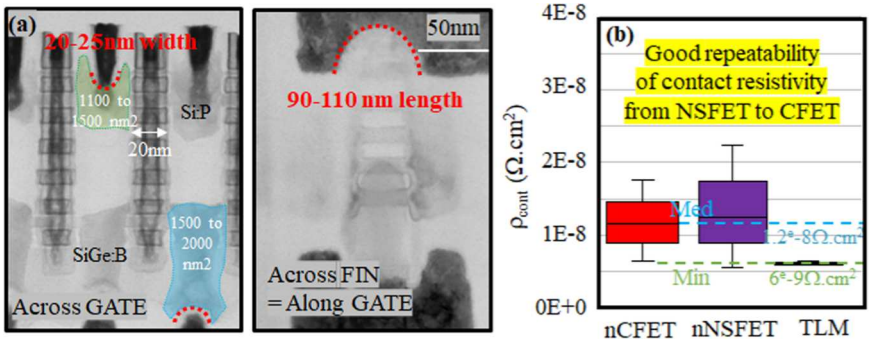

Fig. 14. (a) XTEM analysis of the CFET top n-type device along and across the gate to estimate the contact area. (b) Contact resistivity (ρ_{cont}) and comparison with POR n-NSFET device and with reference value on TLM test-structure.[10)]

V_{OV} is evidenced (Fig. 13(b)). Classical extraction of R_{ch} on a transistor (varying L_G) was also performed (Fig. 13(c)). The main disadvantage of this method is that R_{cont} and $R_{S/D}$ contributions cannot be separated. Very good agreement was obtained on R_{ch} extraction (less than 2% difference). Finally, extraction based on V_{OV} sweep, as presented in the previous section, was also performed on the same sample (Fig. 13(d)), and a good concordance between both extraction methods is obtained for R_{ch} extraction (less than 8% difference).

Calibrating the contact area (A) with XTEM (Fig. 14(a)), the contact resistivity (ρ_{cont}) of the CFET top n-type device can be extracted. The contact size is indeed much smaller than the transfer length, and we can assume that $\rho_{cont} = R_{cont}$ /A. Good agreement with n-NSFET POR device (using the same Si:P S/D epi and metal stack for the contact) is evidenced (see details in[12)]) (Fig. 14(b)). This proves that (active) doping in Si:P is maintained in the transition from NSFET to CFET architecture for this process. Average ρ_{cont} value is the same ($2e^{-8}$ $\Omega.cm^{-2}$), and variability is even slightly reduced for CFET. It's also interesting to note that the minimum ρ_{cont} value is the same ($6e^{-9}$ $\Omega.cm^{-2}$) for NSFET and CFET, and that it's corresponding to the value extracted on large defect-free TLM (Transmission Line Model) structures for the same Si:P epi and contact metals.

3. Conclusions

The CASC test-structure has been upgraded for CFET analysis. Both refined analysis of R_{cont} (including the MOL

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contribution) and extraction of R_{ch} are now possible. Gaining access to such information is critical to understand CFET device limitations and identify the key improvements needed to boost its performance. This was illustrated via analysis on n-NSFET (impact of RTA treatment), p-NSFET (impact of ISP size), and CFET (impact of interconnect scheme and contact size) devices.

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