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Low charge noise quantum dots with industrial CMOS manufacturing

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Silicon spin qubits are promising candidates for scalable quantum computers, due to their coherence and compatibility with CMOS technology. Advanced industrial processes ensure wafer-scale uniformity and high device yield, but traditional transistor processes cannot be directly transferred to qubit structures. To leverage the micro-electronics industry expertise, we customize a 300 mm wafer fabrication line for silicon MOS qubit integration. With careful optimization of the gate stack, we report uniform quantum dot operation at the Si/SiO_2 interface at mK temperature. We measure a record-low average noise with a value of 0.61 $\mu eVHz^{-0.5}$ at 1 Hz and even below 0.1 $\mu eVHz^{-0.5}$ for some operating conditions. Statistical analysis of the charge noise measurements show that the noise source can be described by a two-level fluctuator model. This reproducible low noise level, in combination with uniform operation of our quantum dots, marks CMOS manufactured spin qubits as a mature platform towards scalable high-fidelity qubits.

The demand for greater computational power has put quantum computation in the limelight: the concept of using quantum states for information processing promises a huge speedup and solutions to certain problems that are intractable on classical computers[1]. In the past decades, quantum computing has shown marked development, with small-scale quantum algorithms and quantum advantage achieved on different platforms[2–4]. In moving towards practical quantum computing applications, the research focus is shifting from fundamental qubit operation to large qubit systems[5]. Particularly, qubits fabricated with industrial semiconductor manufacturing technologies recently received great attention[6–8]. The capability of the semiconductor industry in fabricating billions of nanostructures with remarkable uniformity and reliability could indeed be leveraged for the full integration of large-scale quantum processors[9,10]. The rationale here is that the first practical quantum algorithm would require the number of physical qubits to be in the million scale[11], similar to the transistor count of integrated circuit chip transistors back in 1990s[12].

Tantalizingly, the structure of silicon spin qubits closely resembles the CMOS transistor technology[13]. Nanoscale electrodes define the quantum dot structure trapping a single electron or a hole and its spin states encode the qubit[14]. With industrial fabrication, semiconductor nanostructures are patterned subtractively for accurate wafer-scale critical dimension control, where lithography defined patterns are transferred onto the gate electrodes by dry etching rather than the academic-style lift-off process[15]. Comprehensive metrology tools and close process monitoring steps ensure high reproducibility and yield. Moreover, the material science and characterization technology developed around the CMOS industry allow deep insight into the performance limiting factors and optimization directions. All this could provide spin qubits a shortcut for upscaling.

The spin state is also an excellent platform for quantum information encoding and processing[16]. By isotopically purifying the silicon substrate, long quantum coherence has been achieved[17,18]. Single and two qubit gates with operation fidelities higher than the error correction threshold have been demonstrated and efforts towards scaling have been shown with a six-qubit device[18–24]. In addition, spin qubits can be operated at elevated temperatures above 1 K, addressing several upscaling requirements on cooling power and wiring interconnect[25–27]. For the next step towards large qubit arrays, advanced semiconductor manufacturing is commonly expected to be needed to realize the architectures required for scaling up[16,28,29]. However, state-of-the-art spin qubits are mostly fabricated in laboratory-based environments[18–24]. Though there are several exciting demonstrations of qubits made by advanced industrial fabrication with good yield and transport uniformity, the final qubit performance typically shows a certain level of degradation over that of lab devices[6–8]. Device charge noise, which is one of the limiting factors for spin coherence and an important metric characterizing the device quality at cryogenic temperatures[19,30–34], is typically high in fab devices with different materials and structures[8,35–37].

To minimize the charge noise, it is important to understand its origin. The semiconductor/oxide interface has been identified as the source of charge noise and has been intensively studied over the last 40 years[38]. The McWhorter model is widely accepted in MOSFET devices[39], it was first

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introduced to argue that noise in electrical devices is a consequence of an ensemble of defects each represented by a different switching time. In this model, defects in the oxide cause carrier number fluctuations in the MOSFET channel. However, in quantum devices it has been shown that charge noise is not a result of carrier number fluctuations[38,40,41]. Rather, defects at the Si/SiO_2 interface or in the oxide, for these quantum devices, can be described as bistable systems known as two-level fluctuators (TLFs) that couple via the Coulomb interaction[42]. Each TLF has a unique Lorentzian spectrum. A random distribution of TLFs, all added together, results in the infamous $1/f$ noise[43]. However, the microscopic nature of the TLFs remains inconclusive. While many different proposals have been employed to explain the origin of the TLFs including tunneling atoms or tunneling electrons[40,41] it remains difficult to identify microscopic defects from typical measurements. Low noise devices with high quality interfaces could reveal individual TLFs and show their microscopic origin.

In this work, we customize a state-of-the-art 300 mm wafer fabrication flow for silicon MOS qubit structures[7]. Through full gate stack optimization, we demonstrate that the Si/SiO_2 interface could provide low-noise environments for qubit operations rather than detrimental. Across multiple devices, all the quantum dot structures show stable and uniform operation at milli-Kelvin, and an average charge noise level of 0.6 $\mu eVHz^{-0.5}$ at 1 Hz. This ultra-low noise level at different devices and operation conditions allows statistical analysis of the key metrics of the charge noise spectrum. With numerical simulations, we find that the charge noise can be well described with a simple TLF model and provide further insights into spatial density and position.

Results

Device fabrication and interface characterization

Industrial CMOS fabrication processes are used for our device fabrication[7]. We optimize the process flow for spin qubits, specifically for the planar overlapping gate scheme[44]. The overlapping structure has been the main design for high fidelity qubit operations[18,20,22,23], and the integration with the standard industrial fabrication allows wafer-scale accurate critical dimension control and high device yield[7,8,10,35]. Additionally, the planar, gate-based quantum dot structure is compatible with large-scale qubit arrays[16,28,29]. We also employ 300 mm e-beam lithography for the pitch critical quantum dot gates and optical lithography for the size relaxed features. E-beam enables fast turnaround for device designs, and the process can be transferred to advanced optical lithography as similar photoresist and hardmask are used. The fabrication starts with a 12 nm thermally grown oxide, which defines the high-quality Si/SiO_2 interface for quantum dot confinement along the vertical direction. Following that, we deposit the first gate layer across the wafer and pattern it subtractively. Rather than metallic gates, we use polysilicon as the gate metal to reduce interface strain at cryogenic temperatures[35,45]. We then deposit an oxide of 7-8 nm of ALD SiO_2. By repeating the above processes, we achieve the overlapping gates as shown in Fig. 1a.

However, subtractive patterning with dry etching can be more intrusive than academic-style metal lift-off processes[46]. This is further exacerbated for overlapping gate devices, in which each device is subjected to multiple etch steps[35]. The degraded dielectric and interface contribute to quantum dot non-uniformity and higher charge noise. To overcome this, we carefully optimize the process flow, and study the Si/SiO_2 interface with cryogenic hall mobilities[47], as shown in Fig. 1b (methods). In comparison to the first gate level, we find that the mobility drops considerably for higher gate layers. Nonetheless, the degradation is significantly reduced with optimized etching conditions, guaranteeing high quality structures for full qubit integration.

We perform further quantum transport measurements on the first gate layer, where the Si/SiO_2 is protected by the gate from the following processing. The additional transport characterization allows us to compare the effect of implementing different process optimization steps, rather than different layer comparisons. The quality of the primary Si/SiO_2 interface can be evaluated for a large-scale qubit array as well as for the implementation of the single-etch gating scheme[48]. With a base temperature lower than 10 mK, we can reach a peak mobility of 30×10^3 $cm^2V^{-1}s^{-1}$ at a charge density of 4×10^{11} cm^{-2} (Fig. 1c), which is significantly higher than previously reported Si MOS Hallbars with ~10 nm SiO_2 gate oxide[47,49]. From a Metal-to-Insulator fit[50] we determine a percolation density of 8×10^{10} cm^{-2}. This matches the lowest values reported for MOS gate stacks[47,49] and is comparable to SiGe heterostructures[51]. To gain further insight into the interface quality limiting factor, we operate the device in the quantum hall regime as shown in Fig. 1d and extract the Dingle ratio[52] (see Supplementary Information section 1). The Dingle ratio is an indication of the spacing between the scattering centers to the conduction channel in 2D electron gas (2DEG) systems, with higher values mean larger spacing. We report a Dingle ratio ~ 3, which is not as high as GaAs or SiGe heterointerfaces[53,54] but larger than the typically number of ~1 on Si MOS samples[47], suggesting that rather than defects directly at the Si/SiO_2 interface, defects further away, either inside or on top of the oxide also play an important role in our optimized gate stack.

Electrical characterization of single quantum dots

For spin qubits, gate defined quantum dots are used to trap single spins[14]. Beyond the single spin regime, the quantum dots are commonly used as used as charge sensors to read out the spin states via different spin-to-charge conversion methods[55–57]. In this regime, only a single charge can flow through the quantum dot at any given time due to Coulomb repulsion, despite the presence of other charges inside the dot, and the current is very sensitive to the environmental electrical potential[58]. Such a structure is called a single electron transistor (SET).

As shown in Fig. 2a, the SET highly resembles a planar MOSFET transistor but with more gate electrodes[59]. The SET top gate (ST) induces an electron channel while the tunneling barrier gates (LB and RB) define the single quantum dot in between, which is a nanoscale electron island. Figure 2b shows the quantum dot charge stability map by measuring the SET current as a function of biases on LB and RB. The diagonal lines correspond to Coulomb oscillations where electrons tunnel through the quantum dot one by one[58]. Between the Coulomb oscillations, the electron numbers are fixed. From the barrier maps and regular Coulomb oscillations we observe that our system is gate defined and not defect driven.

To study the SET uniformity in the milli-Kelvin temperature range, we measure the $I_D V_G$ characteristics by sweeping each gate individually while keeping the other two at a fixed high voltage potential. In other words, we operate the quantum dot as a conventional MOSFET transistor. In Fig. 2c, we show the average $I_D V_G$ characteristics of 12 devices (12 ST gates and 24 barrier gates). Furthermore, we extract the threshold voltage and sub-threshold swing at standard maximum transconductance point (methods). The devices show remarkable uniformity as seen in the cumulative distribution functions plots in Fig. 2b, with a standard deviation ~70 mV for the barrier threshold voltage and < 20% (5 mV dec^{-1}) for the sub-threshold swing. We note that above SET studies focus on single quantum dots in the many-electron regime, while large qubit arrays require many quantum dots in the last (or few) electron regime, and more studies are needed to address this challenge. Nonetheless, the statistical analysis on SETs in the mK range still highlights the uniformity with CMOS manufacturing and provides initial guidelines for the design of a large-scale spin qubit array[8,60].

Charge noise

An electron spin in a (Silicon) quantum dot has long coherence as there is no direct coupling to charge fluctuations. By isotopically purifying the silicon substrate, recent studies show single spin dephasing times T_2^* beyond 10 μs and even 100 μs[8,17–19,21,30]. The remaining spin-orbit interaction (SOI), either intrinsic from the Si/SiO_2 interface[44] or extrinsic with micromagnet structure[8,20–23,61], indirectly couples the spin to the environment's electrical field noise. Many of the best reported spin qubits show that the device charge noise is in fact the limiting factor for the qubit coherence and the quantum gate fidelity[19,30,62].

To study the device noise, we focus on the SET charge noise, measured in the many electron regime, as it has been shown to well represent the qubit

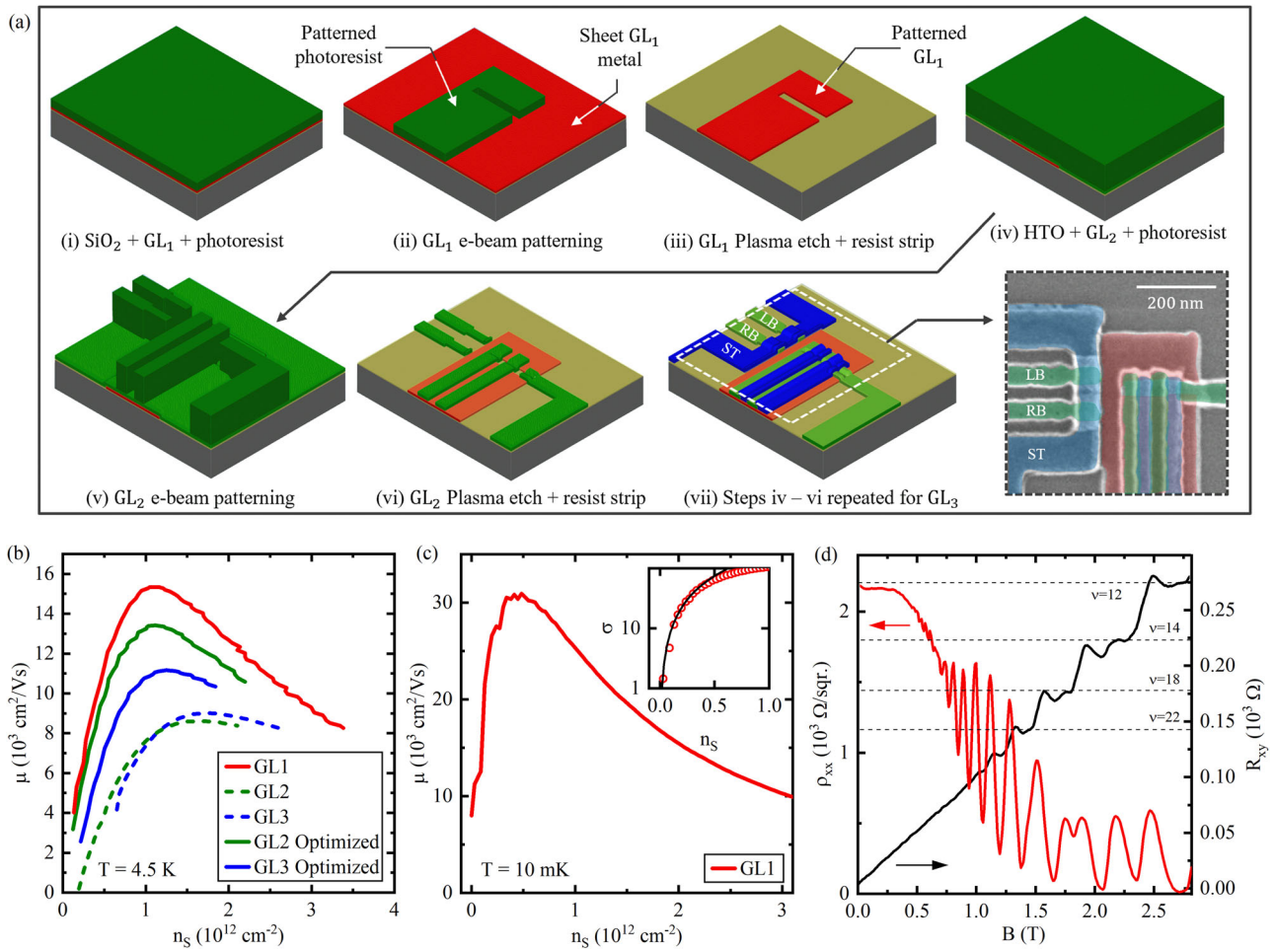

Fig. 1 | Device fabrication and interface characterization. a Schematic of the subtractive patterning steps to fabricate the overlapping qubit structures. (i) A full sheet of gate material and photoresist are deposited through the 300 mm wafer. (ii) The photoresist is patterned with electron beam lithography. (iii) The 1st gate layer is patterned using dry etching techniques. (iv) For the 2nd gate layer, the steps start with deposition of ALD SiO_2, 2nd gate layer, and photoresist. (v) Then the photoresist is patterned with e-beam, and (vi) transferred to the gate material with dry etching. (vii) Step iv-vi are repeated for the 3rd gate layer. The resulting scanning electron microscope (SEM) image of the qubit structure is shown in the bottom right. **b** Hall mobility (μ) with respect to charge carrier density (n_S) of the Si/SiO_2 interface under different gate layers. The effect of multiple patterning steps is evident in the reduced mobility of higher gate layers (gate level 2 and 3, dashed lines). Through process optimization we show an improved mobility for gate level 2 and 3 (solid lines). **c** Hall mobility of gate level 1 at 10 mK, showing a peak mobility of $30 \times 10^3 cm^2 V^{-1} s^{-1}$ and a percolation density of $8 \times 10^{10} cm^{-2}$. **d** Quantum Hall effect of gate level 1 showing clear plateaus in the transverse resistance (R_{xy}) and Shubnikov de Haas (SdH) oscillations in the longitudinal resistance (ρ_{xx}). The SdH oscillations are visible starting $B = 0.5T$ and the oscillation minima go to zero at $B = 2T$, further indicating a high quality single subband transport channel.

noise[30–32,63], and typically the noise figure at 1 Hz is used as the metric to benchmark between different structures and material platforms. On the flanks of the Coulomb peaks, where the SET is the most sensitive to environmental noise, we record the current noise spectrum. We extract the quantum dot potential fluctuation from this current noise with the device transconductance and capacitance ratio (methods), and the final charge noise spectral density is shown in Fig. 3a. This measurement is repeated on all Coulomb peaks ranging from $V_{ST} = 3.5$ V to 4.0 V, as shown in Fig. 3b. For statistical analysis, we perform the same procedure across 12 different devices, which gives 223 different spectra in total. In Fig. 3c, d, we show violin plots of the charge noise at 1 Hz (S_0) and the power factor (γ) extracted from each noise measurement, respectively (see Supplementary Information section 3). The charge noise shows a standard deviation of 0.27 μe $VHz^{-0.5}$ with the average of 0.61 μe$VHz^{-0.5}$ and several points lower than 0.1 $\mu eV/\sqrt{Hz}$. This is the state-of-the-art low charge noise for MOS devices[8,34–36], and comparable to SiGe heterostructures[30,31,33,54].

On closer examination of each charge noise spectrum, we found that most have a power law dependence $1/f^{\gamma}$, where γ is the power factor. This indicates a wide spatial distribution of TLFs but different frequency distributions as γ deviated from 1 slightly in some cases, which has also been recently observed in Si/SiGe quantum dots[33]. However, some spectra are Lorentzian in type[36], or even the combination of a power law and Lorentzian, as seen in Fig. 4a. The Lorentzian noise spectrum suggests the presence of a single dominating TLF[43], which can be expected given the random site of TLFs and the nanoscale quantum dots; for sufficiently low average densities of TLFs, statistical fluctuations in nanoscale devices are expected to result in some devices only observing a (few) dominant TLF(s).

The nanoscale quantum dots together with the low charge noise spectra could therefore serve as an excellent probe for TLFs and their microscopic nature. In Fig. 4b, we plot each S_0 at the corresponding ST bias. Across an ST bias range from 3.5 to 4 V, we see a uniform distribution of S_0. In other words, as we change V_{ST}, different ensembles of TLFs are activated or deactivated randomly within the same frequency range, but the overall active number of TLFs at different electrical field is the same. We further examine the charge noise with respect to different metrics (see Supplementary Information section 3). No correlation between S_0 and γ is observed, suggesting that the TLFs are uniformly distributed in the examined frequency range due to the wide spread of the relaxation times. The exponent γ represents the distribution of TLFs in frequency. If the defects are distributed log-uniform in frequency, the expected γ is roughly 1. An

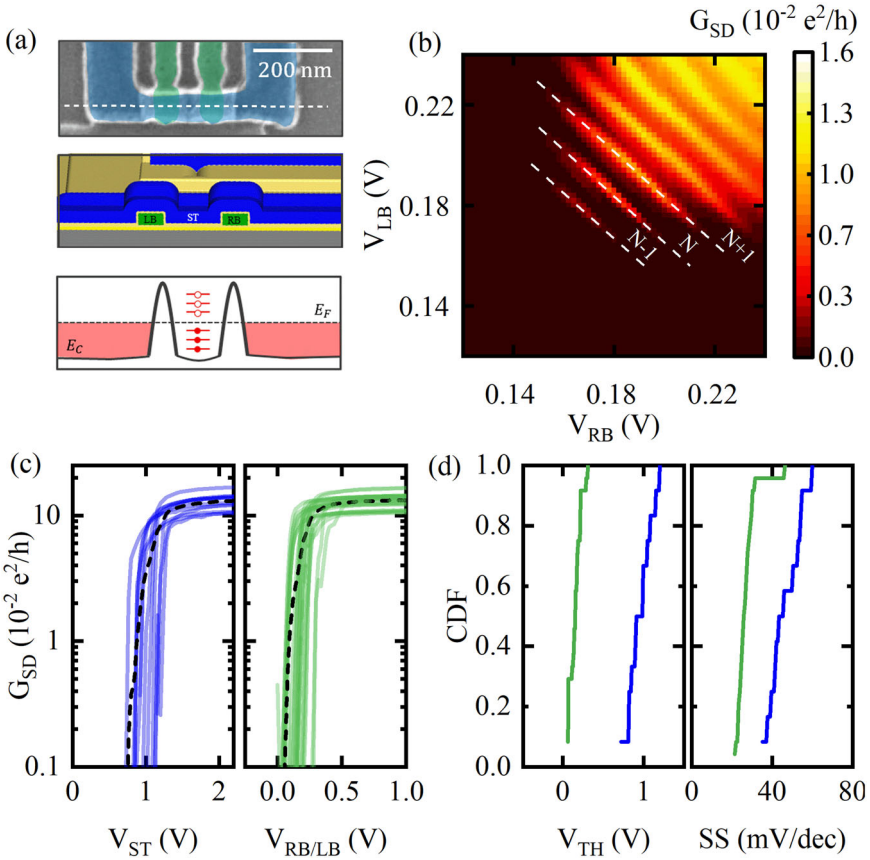

Fig. 2 | SET operation and device uniformity. **a** The SET device structure. The top is the SEM top view. The barrier gates have a critical dimension of 30 nm with a space of 60 nm. At the white dashed line, the schematic cross section is shown in the middle. The bottom shows the conduction band edge diagram, where the SET top gate (ST) forms the electron channel and the left and right barrier gates (LB and RB) induce the barriers above the Fermi level and define the quantum dot. **b** Barrier gate stability map at a fixed $V_{ST} = 3.5$ V. The single quantum dot between the barriers gives the diagonal Coulomb oscillation lines in the map (white dashed lines). **c** $I_D V_G$ characteristics of the top gate (blue lines) and barrier gates (green lines) across 12 SETs at 10 mK. **d** The cumulative distribution functions (CDF) of the threshold voltage (V_{TH}) and sub-threshold swing (SS) of the SET gates. The almost vertical lines, especially for the barrier gates, highlight the level of uniformity with advanced manufacturing techniques.

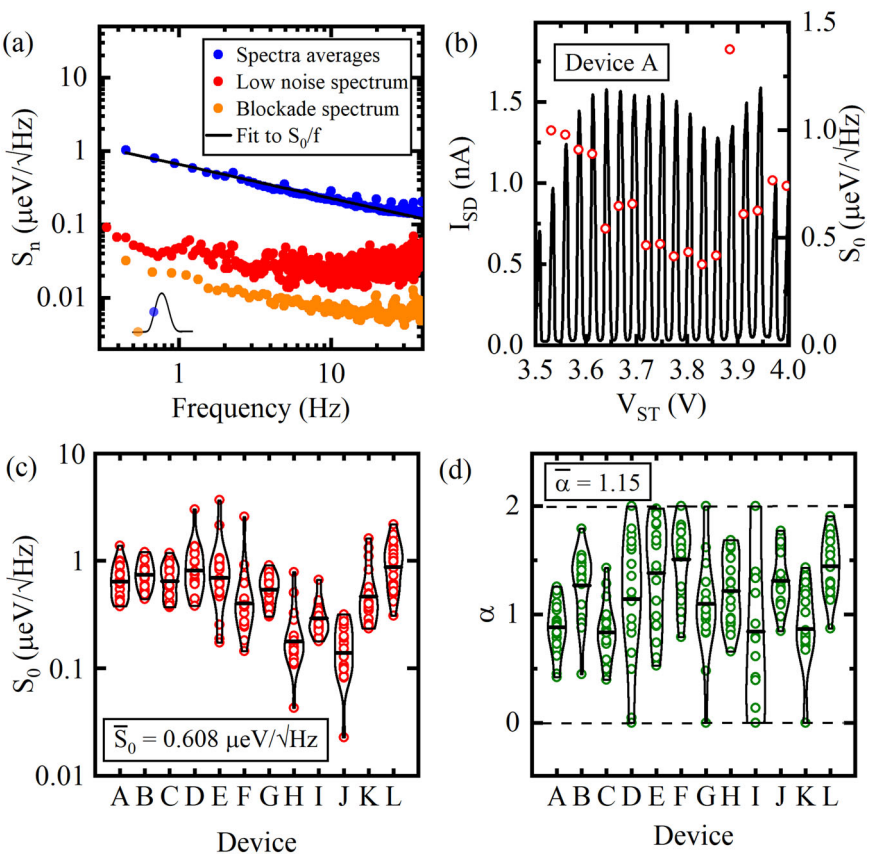

Fig. 3 | SET current spectroscopy and device statistics. **a** Noise spectral density of the quantum dot. The resulting spectrum of the average of all 223 measurements showing a standard $1/f$ spectrum (blue) showing a standard $1/f$ spectrum. Spectral density of the charge noise in Coulomb blockade (orange) highlights that the background noise does not limit the measurements. The noise spectrum of one of the lowest charge noise spectra measured on Device H (red). **b** Coulomb oscillations of device A (black) by sweeping the ST bias. The charge noise at different peaks is overlayed. **c**, **d** The violine plot of S_0 and γ across 12 SETs and 223 peaks, with the mean value shown as a solid line.

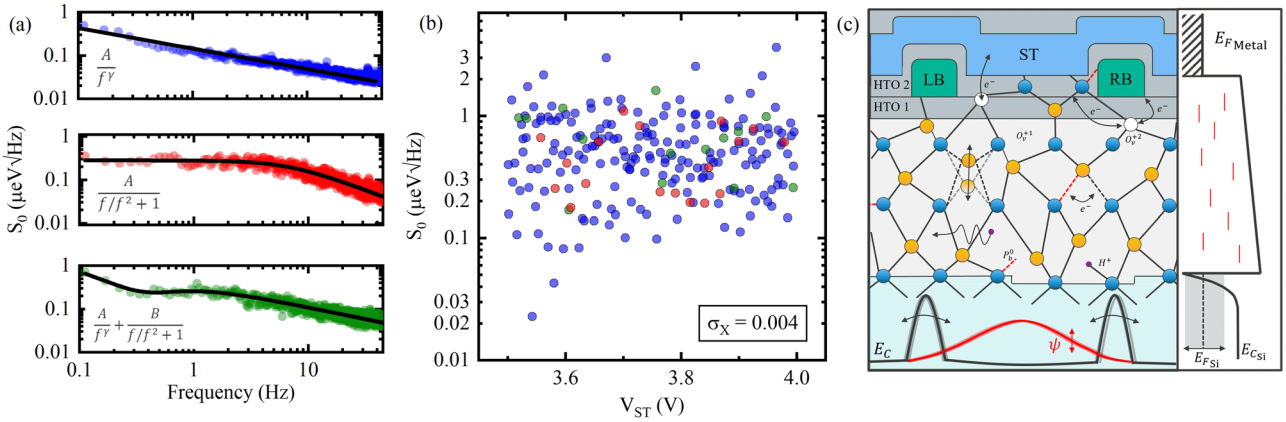

Fig. 4 | Charge noise metrics correlation. a Charge noise spectra with power law (blue), Lorentzian (red), and combination of power law and Lorentzian (green). The Lorentzian spectrum can be observed when a single TLF dominates the charge noise spectrum. This is more likely to happen due to the random spatial distribution of TLFs and low overall TLF density. **b** Scatter plot of S_0 with respect to V_{ST}. The different colors represent the shape of the spectra from (**a**). No correlation is observed suggesting negligible screening and uniform distribution of TLFs in energy. **c** Schematic depicting the types of defects in SiO_2 (including dangling bonds, tunneling atoms, tunneling electrons and oxygen vacancies)[38]. The defects directly affect the electron wavefunction in the quantum dot. Right insert is the band diagram representation of the random TLF energy distribution in the oxide.

increased (decreased) distribution in frequency or a dominating TLF could result in $\gamma < 1$ $(\gamma > 1)$[64]. We find a wide distribution of γ between 0 and 2, suggesting the spectra dataset has a good coverage of TLFs with different switching times. In addition, varying the ST bias changes the number of electrons in the quantum dot, and we detect a systematic change in the quantum dot size and lever arm, which is the ratio of the ST-to-dot capacitance to the overall dot capacitance. As electrons in the quantum dot could partially screen the electrical field, varying the electron numbers could influence the charge noise pickup, especially in the few-electron regime[33,65,66]. But we do not identify a correlation between the charge noise and the lever arm suggesting that the screening effect is weak in our SET structures. Detailed statistical studies in the few electron regime is required for further insights. The above results suggest a uniform distribution of TLFs, which agrees with the standard TLF model[43]. Similar results have been reported with superconducting qubits[38] from defects in the superconducting oxides, where most results are limited to fast TLFs in the radio frequency regime due to the nature of the microwave resonators in the qubits acting as a frequency filter. Albeit of different physical origin, our results suggest that near DC, i.e., nine frequency decades away, slow TLFs around 1 Hz are also uniformly distributed at the Si/SiO_2 interface and/or in the oxide, as shown schematically in Fig. 4c.

Noise simulations

Our statistical measurements and analysis on the quantum dot charge noise suggests its microscopic origin: randomly distributed TLFs over a nanoscale device area. To further verify this postulation, we employ a simplified TLF model to reconstruct and validate the experiments. Following our previous study in ref. 64, we use double well potential (DWP, charge dipole) type defects to represent the TLFs as they best match the quantum dot charge noise Conversely, the full electron trapping/detrapping type of defect would lead to much larger noise distributions than what we observe in our data – as well as much larger than in previously published literature results[8,33]. We assume a two-dimensional distribution of TLFs in the silicon oxide, and only the TLF density (n_{TLF}) and its depth in the oxide (z) are tunable variables in the simulation. With the above conditions, TLFs are randomly placed over an area centered around a many-electron quantum dot. We perform a Monte Carlo simulation with 1000 random sets of TLF configurations and extract each noise spectrum of the quantum dot potential. Further details about the simulation can be found in Supplementary Information section 6.

Figure 5a shows the average noise at 1 Hz ($\bar{S_0}$) as a function of n_{TLF} and z. In Fig. 5b, c, we plot the kernel density for the γ and S_0. Decreasing n_{TLF} or reducing z increases the distribution of S_0 and γ around the averaged values, as the probability of finding a single dominating TLF increases. We find $n_{TLF} = 1.6 \times 10^{10}$ cm^{-2} and $z = 6$ nm to best represent the experimental distributions as shown in the overlaying distributions in Fig. 5d, e. The good simulation-to-experiment agreement on charge noise and power factor for both average values and distribution further supports that randomly distributed TLFs over the quantum dot lead to the device charge noise. In addition, we would like to point out that other combinations of n_{TLF} and z could still have reasonable match between simulation and experiments, and three-dimensional distribution of TLF could give a better matching than simple two-dimensional (Supplementary information section 6). Based on our simulations, we believe that advanced CMOS processing reduces disorder associated with the Si/SiO_2 interface, and that defects within the oxide play an important role in this scenario. The Si/SiO_2 interface does not need to be detrimental to quantum dot performance, and disorder at the interface, deep in the oxide, or even at the upper oxide/gate interface should be taken into consideration for further optimization[67].

This simple TLF model also enables the construction of a charge noise environment to predict the qubit performance. With the co-simulation framework reported in ref. 64, we estimate the two-qubit SWAP gate fidelities with above TLF distribution (see Supplementary Information section 7). The average SWAP error in our models is lower than 0.1%, highlighting the low noise level of Si MOS quantum dots with industrial manufacturing. Meanwhile, a relatively large variation in qubit fidelity due to the randomly distributed TLFs can also be captured in the simulation, suggesting that statistical analysis on the qubit metrics is needed to properly assess the qubit environment.

Discussion

We show the integration of Si MOS quantum dots with full industrial 300 mm wafer fabrication. By leveraging the know-how of CMOS technology, we optimize the full gate stack for high performance spin qubit devices with high yield and uniformity, as previously reported in 7. The Si/SiO_2 interface shows state-of-the art Hall mobility and critical density. Considering the nanoscale nature of the quantum dots versus the full 300 mm wafer, we characterize multiple SETs for statistical analysis. The SET gates demonstrate uniform turn on curves and single quantum dot formation in the milli-Kelvin temperature range. We further characterize the SETs using current spectroscopy techniques and extract record-low average charge noise of 0.61 μeVHz$^{-0.5}$ on Si MOS structures. The stable, uniform, and low noise operation is comparable to the best reported SiGe heterostructure base devices, which shift the interface to the deeper Si/SiGe

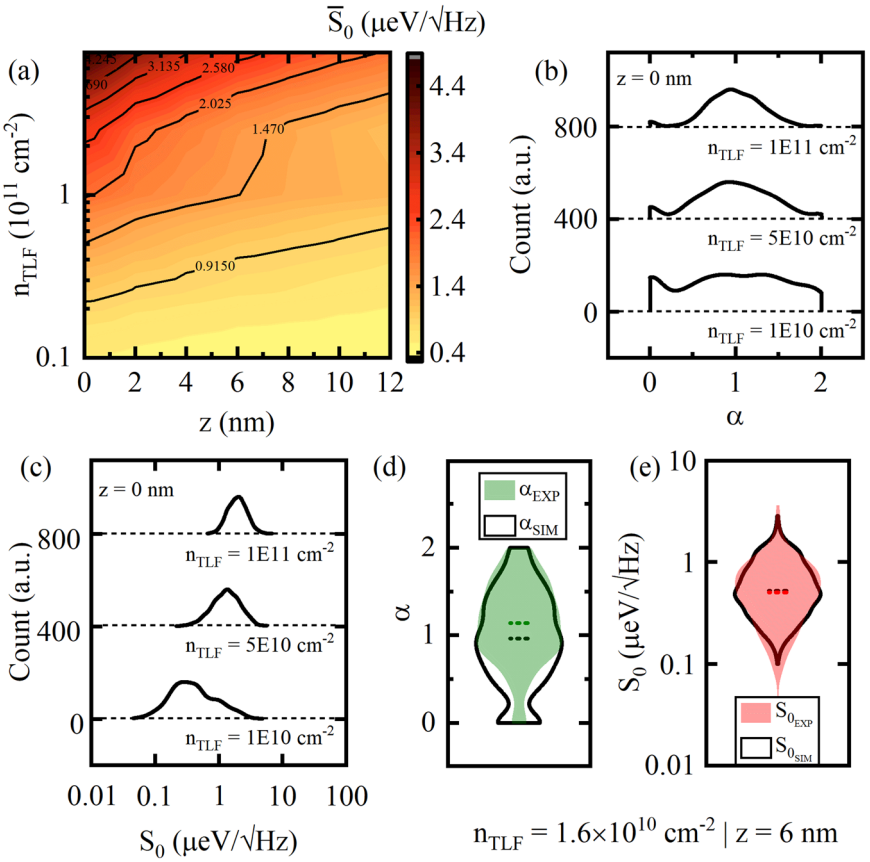

Fig. 5 | Charge noise simulations. a Contour plot of the simulated quantum dot charge noise with respect to the TLF density (n_{TLF}) and the depth in the oxide (z). **b**, **c** The kernel distribution estimation of γ, S_0 at different n_{TLF} generated from 1000 simulations. **d**, **e** The violin plots of γ and S_0 with experimental data with the mean value shown as a dotted line. Overlayed are the simulation results that best matches the experimental average and distribution ($n_{TLF} = 1 \times 10^{10}$ cm^{-2}, $z = 6$ nm).

quantum wells to reduce the influence from disorders. However, the Si/SiGe buried quantum well brings significant drawbacks in terms of valley splitting[50,68] as well as crosstalk[69], limiting the yield rate and addressability of large qubit arrays. Our results confirm the Si MOS is and remains a compelling material platform for spin qubits and the maturity of industrial fabrication for the qubit development.

The low noise quantum dot together with its nanoscale size could be an excellent probe for TLFs and their microscopic nature. The statistical analysis of the charge noise shows uniform distributions with respect to different metrics. Noise spectra reconstructed with a simple TLF model can also match the experiments well. These findings are strong evidence that the quantum dot charge noise indeed originates from randomly distributed DWP type defects over the nanoscale area. Future studies could investigate the influence of gate oxide thickness on charge noise and explore novel detection methods for slow TLFs across the gate stack.

A thorough understanding of the qubit environment is crucial for upscaling to large and reproducible qubit arrays. Our statistical analysis of the quantum dot charge noise and the TLF model provides important insights into the microscopic origin of charge noise. Our methodologies also have the advantage of faster throughput and statistical relevance compared to much slower experimental data from individual qubits – the slow throughput of the latter currently limiting our understanding and being subject to uncorrected drift phenomena that affect qubit metrics[30]. We therefore believe that our results and methodologies will allow efficient feedback into the qubit design optimization process and help advance the scaling up of spin qubit devices.

Methods

300 mm device integration

The quantum dot devices are fabricated with a 300 mm integration flow. The fabrication starts with intrinsic silicon wafers. Optical lithography was used to defined alignment markers and ohmic implantation. Then electron beam lithography (EBL) is used to pattern the pitch-critical quantum dot gates. Here we employ EBL for flexible and short turnaround replacement for advanced optical lithography[70]. For better process compatibility, we use the same photoresist for EBL as advanced optical lithography. Apart from the light/e-beam sensitive layer, there is also a hardmask layer at the bottom of the photoresist, which helps preserve the pattern during the etching process[15]. As shown in Fig. 1a, the quantum dot gate stack starts from thermally grown SiO_2, followed by the polysilicon layer with chemical vapor deposition and photoresist. Then the photoresist is patterned by EBL and transferred to the polysilicon gate subtractively with plasma dry etching. The 2nd and 3rd gate layer starts with the deposition of inter-gate dielectric. Then similar processes as the 1st gate layer are used for patterning. After that, we switch back to optical lithography. Another layer of silicon oxide is deposited followed by optically defined ESR antenna or EDSR micromagnets as qubit control structures. Finally, the quantum dot structures are encapsulated with a back end of line module, including a thick layer of silicon oxide, qubit gate via contact, metal bonding pad, and forming gas annealing. Through the integration process, we employ inline and post-line process monitoring. Tight critical dimension (CD) control is achieved for all gate layers, with a standard deviation ~1 nm for quantum dot gates. After full processing, electrical characterization of different metrology structures is carried out to verify the processing. Additionally, room temperature leakage and $I_D V_G$ sweeps of the quantum dots are carried out to determine the yield as described in 7, with this particular process resulting in a 95% yield. More details about the integration flow, process monitoring, and proof of principle qubit operation can be found in ref. 7,35.

In our previous study, we report charge noise in the few μeV Hz$^{-0.5}$ range (3.6 μeV Hz$^{-0.5}$ with single data point in ref. 35). Through full gate stack optimization, we achieve the low noise environments in this work. For the first gate level, the improvement in the Hall mobility is due to a thicker dry oxide layer (12 nm vs 8 nm) than our previous work[48], which can be attributed to a further oxide/deposited oxide interface. For the higher gate

layers, we increase the deposited ALD silicon oxide thickness from 5 nm to 8 nm. To reduce the damage in the dry etching process, we replaced the etchant from chlorine-based to hydrogen bromide[71], as the heavy bromide ion could provide better selectivity at the end of polysilicon etching, which would reduce the physical bombardment damage. In addition, we carefully control the etching time by monitoring the emission spectra during the dry etching process.

Hall bar characterization

The fast turn-over interface characterization is carried out in a cryogenic probe station with base temperature of 4 K and a 2.5 T magnet. This allows us to refine the process and identify high quality gate stacks with optimized processes for further detailed characterization. The advanced interface characterization is carried out in a dilution fridge with a base temperature of 8 mK and a 3 T magnet. Both setups employ a standard Hall bar measurement procedure where a positive voltage is applied to the top gate to form a 2-dimensional electron gas (2DEG) at the Si/SiO_2 interface. The current through the sample is measured through an IV transimpedance amplifier. Additionally, the longitudinal and transverse Hall voltages are measured simultaneously using standard lock-in techniques. The Hall carrier sheet density n_S is extracted from the Hall resistance $R_{xy} = \mathbf{B} \cdot n_S \cdot e$, where B is the magnetic field, n_S is the 2DEG density, and e is the electron charge. The carrier mobility μ is obtained from $\mu = n_S \cdot e \cdot \rho_0$ where ρ_0 is the resistivity. The percolation density is extracted from a metal-to-insulator transition (MIT) fit of the density dependent conductivity $\sigma \sim (n_S - n_p)^{1.31}$. The measurement is repeated on three different Hall bars across the wafer, and we found good agreement.

Quantum dot threshold voltage and subthreshold swing

A fourth order routine is used to calculate the derivative of the measured $I_D V_G$ data. The maximum derivative (maximum transconductance g_m) of the curve is used to calculate the threshold voltage V_{TH} and the conductance K_0. All gates of the quantum dot were operated in the linear regime where the drain current is given by $I_D = K_0(V_G - V_{TH} - V_D/2)V_D$. Thus, the $I_D V_G$ is used to fit K_0 and V_{TH}. The conductivity K_0 equals the fitted slope divided by the drain voltage. The threshold voltage V_{TH} is the intercept of the tangent line $g_{m_{max}}$ with the x-axis minus $V_D/2$.

Electrical characterization of the quantum dots

The devices are tuned systematically with the following procedure. From the barrier gate stability map, we identify the barrier gate voltage. We then sweep the top gate bias from 3.5 V to 4.0 V to measure the Coulomb oscillations. If a background current is observed between the Coulomb oscillations, the barrier gates are readjusted, and the measurement repeated. The source drain bias is then swept with respect to the top gate voltage to obtain Coulomb diamonds. We measure the drain current noise and convert the time domain signal to the effective single-sided (double sideband) spectral density with a Hann window. During the data collection, the spectrum is smoothed with an exponential averaging filter of $s_t = \alpha_{exp} x_t + (1 - \alpha_{exp}) s_{t-1}$, where s_t (s_{t-1}) is the current (previous) spectrum and α_{exp} is the smoothing factor. We use α_{exp} of 2/31 (or weight of 30) and a total measurement time 10 times longer than the single spectrum collection time (as the spectrum is stable and we do not see difference with longer measurement times). The current noise spectrum is converted to charge noise spectrum using $S_0 = \alpha\sqrt{S_I}/(dI/dV_{ST})$, where α is the lever arm of the quantum dot, and dI/dV_{ST} is the slope of the Coulomb peak. Further details on extracting the quantum dot charge noise can be found in the Supplementary Information section 2.

Data availability

The data that support the findings of this study are available from the authors upon reasonable request.

Code availability

The analysis and plotting codes used in this study are available from the authors upon reasonable request.

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Author contributions

A.E., M.M.K.S., and C.G. performed the experiments. S.K. integrated the devices with support from S.M., Y.C., and J.J. M.M.K.S. performed the simulation with support from G.S. R.L., M.M., D.W., B.G. I.R., P.V.D. and K.D.G. conceived and supervised the project. A.E., R.L., and K.D.G. wrote the manuscript with input from all the authors.

Competing interests
The authors declare no competing interests.

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