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Wideband D-band Antenna Array Co-Designed with Wirebonded Power Amplifier on a PCB Carrier

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***Abstract*—The co-design, fabrication and characterization of an active D-band antenna array with large bandwidth for use in next-generation, high-speed wireless systems is presented. A silicon-germanium (SiGe) BiCMOS D-band power amplifier (PA) is compactly integrated on the backside of a printed-circuit-board (PCB)-based 4×1 antenna array with a vertical substrate-integrated-waveguide-based corporate feed network, minimizing its impact on the array's radiation pattern, while keeping the array width below λ/2. This co-design is performed by employing a tailored wirebonding process to minimize interconnect loss and by optimizing the antenna array's input impedance to maximize the PA's peak output power. The former is achieved by thinning the integrated circuit (IC) and embedding it into a milled cavity in the PCB carrier, thereby leveling the IC and PCB surfaces to minimize the bond wire length. To attain the latter, a grounded co-planar waveguide-to-substrate-integrated-waveguide transition is proposed to tailor the antenna input impedance and compensate for the remaining effects of the bond wires. After assembly, the active antenna array is characterized in terms of gain, bandwidth and equivalent isotropic radiated power (EIRP). The module features a peak combined gain of 26 dBi over a 3dB-gain bandwidth of 23 GHz and a maximum EIRP of 22.8 dBm with a 25 GHz EIRP bandwidth.**

***Index Terms*—D-band, power amplifier, integrated circuit, printed circuit board, substrate-integrated-waveguide, antenna array**

I. Introduction

THE growing demands for high data rate and fine-resolution sensing applications in the 6G framework necessitate the exploration of new frequency bands. Particularly, the D-band (110–170 GHz), with its large, yet unexploited frequency spectrum, arises as a promising contender [1]–[12]. At such frequencies, significant propagation losses must be overcome by levying high-gain antenna systems, consisting of high-gain amplifier structures and directional antenna arrays [5], [7]. Consequently, to maintain high output power, efficient, yet cost-effective integration strategies of antenna arrays with compact amplifiers are key [13]. Flip-chip methods have already been proven to provide low interconnect losses between integrated circuit (IC) and an antenna-in-package [14] or antenna-on-board [15], but they require finer lithographic resolution in the package or board design—an issue that becomes even more pronounced with the ever-decreasing dimensions of ICs [16]. Wirebond integration provides a cost-effective alternative, with a higher compatibility with low-cost carrier substrates. Wirebonding, however, may significantly influence the matching at the interface between array and IC [7]. Therefore, to realize high-gain active antenna systems compatible with low-cost assembly and fabrication techniques, co-design is essential to minimize the parasitic effects of antenna-to-IC interfaces.

In this work, we present the co-design of a compact printed-circuit-board (PCB)-based 4×1 D-band antenna array with an integrated, wire-bonded SiGe D-band power amplifier, featuring stable gain over a 23 GHz bandwidth through a tailored wirebond process and an impedance-transforming grounded-co-planar-waveguide (GCPW)-to-substrate-integrate-waveguide (SIW)-transition at the array input. The vertical feed structure of the corporate fed array enables backside integration, lowering interference between power amplifier (PA) and array, and ensuring a subarray width below λ/2 to allow array scaling. First, the effects of the bond wires are minimized by thinning the PA IC and placing it inside a milled cavity within the PCB to level the IC and PCB surfaces. Next, the GCPW-to-SIW transition and the 4×1 array are co-designed to maximize PA output power and bandwidth, while accounting for bond wire effects. After assembly, the measured prototype, consisting of the 9 dBi gain array and 18 dB gain PA, showcases a 23 GHz 3 dB-gain bandwidth, with a peak combined gain of 26 dBi and an effective isotropically radiated power (EIRP) of 22.8 dBm.

Comparing to active D-band arrays in literature, shown in Table I, it is clear that this implementation achieves state-of-the-art performance, while relying on cost-effective assembly techniques through this co-design strategy. It features high gain, competitive bandwidth and the highest single-channel EIRP of any SiGe implementation, while retaining scalability, enabling a further increase of the system's gain and EIRP.

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TABLE I
STATE-OF-THE-ART ACTIVE D-BAND ANTENNA ARRAYS.

Ref.	Freq. (GHz)	PA Tech.	Antenna Type/ # Elements	Gain (dBi)	BW (GHz)	EIRP/ Channel (dBm)
[17]	134	40nm CMOS	DRA / 4	4.4&	36	15
[18]	139	28nm CMOS	Dipole Array / 2	2.3&	27	12.2
[19]	140	130nm SiGe	DRA / 4	5.8&	15	21
[20]	114	130nm SiGe	Slot Array / 8	6&	1	14.2
[7]#	135	InP	Patch Array / 8	36$	6	27.5
This	**130**	**130nm SiGe**	**PCB / 4**	**26**	**25**	**22.8**

Full Tx module $ Includes baseband/conversion gain & Antenna only

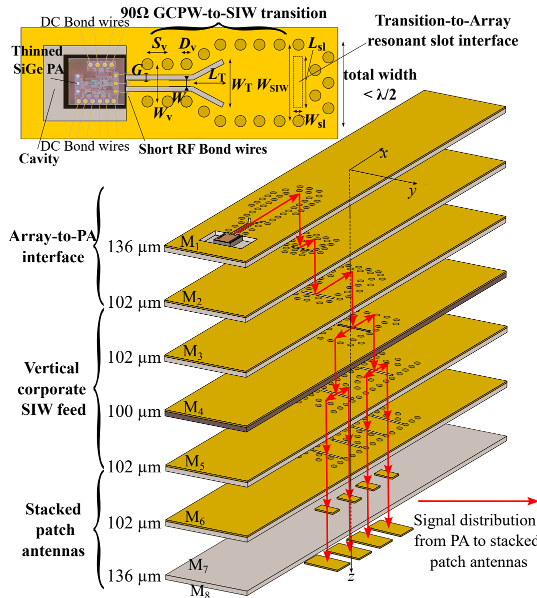

Fig. 1. Vertically integrated corporate-fed array with compactly integrated PA, implemented on a high-density interconnect PCB. A cavity in the top PCB surface allows closer integration of the thinned IC to the signal conductor on M_1 by reducing their relative height difference. Additionally, a GCPW-to-SIW transition is implemented to match the antenna input impedance to the IC output impedance for optimal power transfer, incorporating parasitic bondwire effects. The total width of the subarray component remains smaller than $\frac{\lambda}{2}$, allowing for future array scaling. The transition dimensions are given by: W = 50 µm, G = 87.5 µm, L_T = 0.4 mm, W_T = 0.65 mm, W_{SIW} = 1.05 mm, D_v = 0.2 mm, S_v = 0.4 mm, W_v = 0.625 mm, L_{sl} = 0.9 mm and W_{sl} = 75 µm

II. CO-DESIGNED ACTIVE D-BAND ARRAY ARCHITECTURE

A. System Overview

The proposed active D-band antenna array, presented in Fig. 1, showcases the compact integration of a SiGe PA onto the backside of a PCB-based D-band antenna array using a tailored wirebond process and a dedicated GCPW-to-SIW transition. By deploying a milled cavity and thinning the IC, the bond wire lengths are minimized. Additionally, through co-design with the custom antenna interface, an optimal load impedance is provided to the PA, resulting in (i) maximum output power, (ii) wideband operation, (iii) stable flat gain, and (iv) enabling array scalability in future deployment.

The antenna array, consisting of four antenna elements fed by a vertical corporate SIW feed network [21], is implemented into the PCB-carrier consisting of eight metal layers and seven layers of Megtron 7 substrate. Unlike in [21], where the SIW feed is considered the input of the array, here, the array is fed by a GCPW-to-SIW transition. By vertically integrating the feed network of the antenna array, the SiGe PA [22] can be integrated on its non-radiating side, preventing radiation degradation from the IC bond wires and transition structures, while also shielding the IC from antenna radiation. The total 3 dB-gain bandwidth of the active antenna array is designed for operation within the 120-145 GHz band, while ensuring that the output power of the PA remains within 1 dB from its optimum and minimizing bond wire loss. The total width of the array after integration should remain smaller than or equal to $0.49\,\lambda$ for scalability.

B. Co-Design

To evaluate the effects of the bond wires on interconnection loss and impedance matching at D-band frequencies, a full-wave two-port electromagnetic (EM)-model of the PA-to-array interface is constructed using CST Microwave Studio, depicted in Fig. 2. The PA is modeled according to the stackup of the IHP SG13G2Cu process technology [22], using a copper groundplane and $40\times40\,\mu$m aluminum pads. The PCB is modeled as shown in Fig. 1. The two simulation ports are placed at the IC's output pads and GCPW antenna interface, respectively, while their interconnection is realized with 25 µm-thick gold bond wires. The two-port model simulates the impedance transformation caused by the bond wires from the antenna interface to the PA output. Fig. 2(a) illustrates the conventional integration with wirebonding, where the PA IC is deployed directly on the PCB surface and wirebonded to a standard 50 Ω antenna array. The antenna input impedance Z_{Ant} (50 Ω) matches the ideal load impedance for this PA. However, the inclusion of the bond wires significantly alters the load impedance Z_{L}. The resulting mismatch degrades the peak output power of the PA by more than 1 dB, lowering its overall output power. This is represented on the Smith chart in Fig. 2(c), which depicts the PA's simulated 1 dB-loadpull contour, obtained using Cadence, as well as the impedance presented by the wirebonded antenna array Z_{L}. This 1 dB-loadpull contour indicates the region where the output power of the PA remains within 1 dB from its optimum.

In our approach, we first aim to minimize the effects of the bond wires on Z_{L} by minimizing their lengths. This is achieved by first milling a cavity in the PCB surface where the PA is placed and, then, thinning the IC further until the PCB and IC surfaces are closely aligned. In this case, the PCB manufacturer supports cavities of up to 150 µm in depth. This already greatly reduces the height difference between the IC and the array input. To further decrease this difference, the chip was also thinned using a chemical-mechanical polishing (CMP) process to a thickness of 150 µm. In Fig. 2(b), the resulting wire bond profile is depicted. Fig. 2(c) shows that reducing bond wire length improves performance, though the load impedance remains outside the 1 dB loadpull contour.

To further maximize output power, the array impedance Z_{Ant} is co-designed with the bond wires. Load-pull simulations indicate that terminating the short bondwires by a 90 Ω impedance, results in the most optimal load impedance Z_{L} presented to the PA output. As such, by transforming the antenna impedance Z_{Ant} to 90 Ω, the impedance transformation

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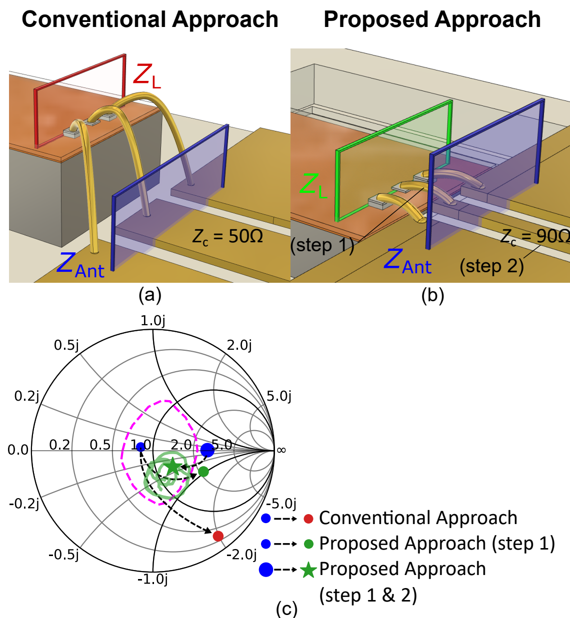

Fig. 2. 3D representation of the EM-model used to evaluate (a) the conventional integration method and (b) the proposed approach, along with (c) the antenna and load impedance realized by the conventional approach and our proposed approach. The pink curve represents the 1 dB-loadpull contour of the PA. The markers indicate the impedance at 130 GHz. The green star marker, indicating the final co-designed active array, is situated within the 1 dB-loadpull contour, indicating optimal PA operation. The transparent green curve indicates this final impedance over the full 120-145 GHz band.

caused by the bond wires is taken into account, moving Z_L, indicated by the green star, into the 1 dB-loadpull contour. The required impedance transformation is achieved by deploying a GCPW-to-SIW-transition at the input of the SIW-based array, interfaced via a resonant slot. This transition achieves a broadband match between the SIW-fed antenna array, and the desired 90 Ω GCPW trace by converting the SIW's TE_{01} mode to the GCPW quasi-TEM mode over the 120-145 GHz band by a gradual tapering mechanism. The bandwidth of the conversion is controlled by the taper dimensions L_T and W_T. Specifically, increasing L_T improves the transition bandwidth but enlarges its footprint. W and G control the characteristic impedance Z_c of the GCPW and are chosen such that this Z_c is 90 Ω by decreasing W to 50 µm and tuning G. Hence, by first leveling IC and PCB, and subsequently co-designing the 4×1 array with the GCPW-to-SIW transition, the desired bandwidth can be covered through wirebonding, indicated by the simulated PA gain shown in Fig. 3(a). This figure indicates the gain contribution of the PA in the aforementioned integration approaches, obtained by combining the PA's measured S-parameters with the full-wave model of the interconnect and antenna. Our proposed approach significantly reduces the gain ripple to below 2 dB, while the PA gain loss due to load mismatch and insertion loss has now decreased to a reasonable 1 dB. Meanwhile, the conventional approach shows a significant gain penalty of up to 15 dB in the considered band. Moreover, the PA's transmission characteristic indicates significant distortion, with variations in PA gain of up to 12 dB caused by the frequency-dependent behavior of the long bond wires, severely limiting bandwidth. The figure

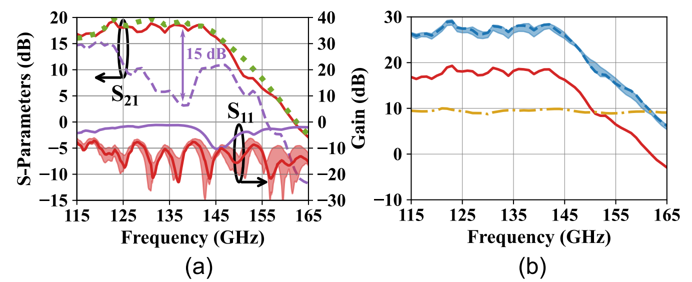

Fig. 3. (a) PA gain with ideal, conjugately matched terminations (dotted green), with the conventional approach (dashed purple) and proposed integration method (solid red curve). $|S_{11}|$ of the wirebonded antenna array for a conventional approach (solid purple) and with the proposed integration method (solid red curve and band). (b) Simulated broadside gain of the GCPW-fed antenna array (dashdotted yellow), PA gain after applying the proposed co-integration techniques (solid red) and simulated total gain of the assembled active array with sensitivity analysis variations (dashed blue curve & band).

also shows the $|S_{11}|$ of the wirebonded array in both the conventional approach, showing the substantial mismatch and low bandwidth, and the proposed integration approach, which shows drastically improved matching and bandwidth. Next, the total active array gain is calculated by taking the passive array gain into account, resulting in Fig. 3(b). A simulated peak gain of 28 dBi along with a 25 GHz 3 dB-bandwidth is obtained. Additionally, the PA is simulated to be able to deliver a peak power of 15 dBm to the antenna at 130 GHz, yielding an EIRP of 24 dBm when adding the passive array's gain.

Finally, a sensitivity analysis is performed to gauge the performance degradation of the active array due to variations in antenna dimensions (10 % in substrate thicknesses, slot lengths and patch dimensions, see also [21]) and integration variations (10 % in bond wire lengths, heights and 50 µm in bond wire connection points). These are included by simulating them in a combined full-wave EM-model to obtain Z_L for each variation. This analysis confirmed that the bond wire lengths and substrate thickness are the two most critical parameters to ensure both good matching and gain. The result of this analysis is shown by the colored bands in Fig. 3, indicating limited impact in S_{11} and $<$ 1.5 dB of variation in passband gain.

III. Active Antenna Array Measurements

Before integration, the passive GCPW-fed array is characterized. Fig. 4(a) shows the simulated and measured reflection coefficient, as well as the normalized far-field radiation patterns, measured in the mmWave spherical anechoic chamber [23] at Eindhoven University of Technology (TUe). The reflection coefficient, normalized with respect to 90 Ω, remains below -10 dB over the 120-145 GHz band, as desired.

Next, the active integration is performed. Close-up images of the integrated array are displayed in Fig. 5. A 3D-measurement using a Hirox HRX-01 microscope is performed to confirm the reduced height difference between the IC and PCB surfaces. This shows a cavity depth of 160 µm and an IC thickness of 150 µm. This significantly reduces the obtainable bond wire length to 150 µm.

Next, an EIRP measurement is performed using the setup detailed in Fig. 6. A VDI WR6.5 VNAX range extender is

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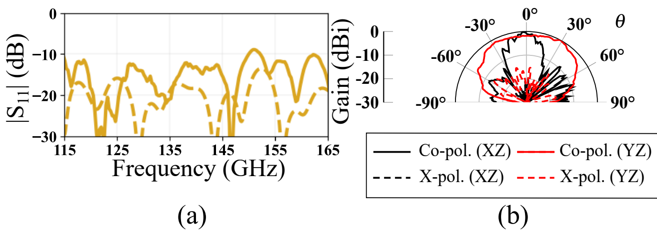


Fig. 4. (a) Simulated (dashed curve) and measured (solid curve) reflection coefficient and (b) Principal cuts of the measured normalized far-field pattern at 130 GHz of the probed passive 4×1 antenna array.

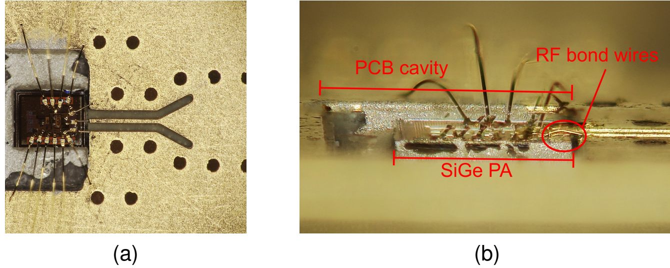
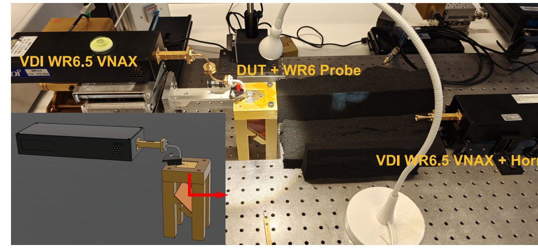


Fig. 5. (a) Top view and (b) side view of the transmit array assembly, showing the wirebond process after IC thinning and cavity milling, indicating that the proposed integration strategy results in particularly flat RF bondwire profiles.



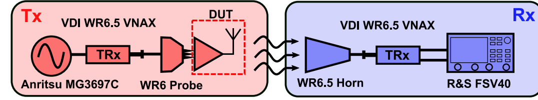


Fig. 6. Measurement setup used for the EIRP measurements.

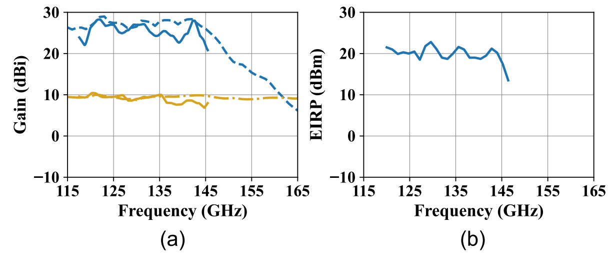


Fig. 7. (a) Measured (solid blue curve) and simulated (dashed blue curve) gain of the full active D-band array, along with the measured (solid yellow curve) and simulated (dashdotted yellow curve) gain of the GCPW-fed array. (b) Measured EIRP of the active D-band array.

mounted on a positioner stage, which enables interfacing with a GGB WR6.5 waveguide probe. The probe then interfaces with the device-under-test (DUT) mounted in a 3D-printed holder containing a copper reflector. This reflector-based setup enables probed array measurements, while facilitating measurement of the emitted broadside radiation with minimal radiation pattern distortion. The receiver consists of another VDI VNAX extender with a mounted WR6.5 horn antenna. The local oscillator (LO) and intermediate frequency (IF) ports of the receiving VNAX are connected to a Rohde & Schwarz FSV40 spectrum analyzer to process the received signal.

First, the output power of the transmitting VNAX is measured using a VDI PM5B waveguide power meter. Combined with the passive array's gain, this yields the EIRP of this reference transmitter. The passive array is then measured using the setup described above and a reference measurement is obtained. Finally, the measurement is repeated with the active array and the received power is compared to the reference measurement. The difference in measured power, combined with the EIRP of the reference transmitter, yields the saturated EIRP of the active array. Fig. 7 shows that the active array has a peak EIRP of 22.8 dBm at 130 GHz, closely matching the simulated value of 24 dBm. The EIRP also exhibits a bandwidth of 25 GHz. Moreover, the active array consumes around 300 mW of DC power, comparable to other implementations in literature [17]–[19]. This yields a PAE of 8 %.

To determine the gain of the active antenne array, the setup from Fig. 6 is adopted. Both range extenders are replaced by a VDI WR6.5 sub-harmonic mixer (SHM), whose LO is provided by an Anritsu MG3697C signal generator. The IF ports of the mixers are connected to a Rohde & Schwarz ZNA67 vector network analyzer (VNA). An S_{21} measurement is then performed using the DUT. By performing an additional calibration measurement with a known antenna, the gain of the DUT is calculated through the gain transfer method [24].

For the calibration measurement, a waveguide-fed version of the array, previously characterized in an anechoic chamber [21], was used, since its radiation pattern in the frontal hemisphere will be identical to that of the DUT. Fig. 7 shows the result of the calibrated broadside gain measurement of both the passive and active array, compared to their simulated counterparts. This shows good agreement between simulation and measurement, indicating that the active array achieves an average gain of 24 dBi with a peak gain of 26 dBi. Moreover, the measurement also shows a 3 dB-bandwidth of 23 GHz between 120 and 143 GHz. Moreover, the measurement results of the passive array are also in good agreement with simulations. The flat gain profile of the passive antenna array indicates the efficiency of the underlying compact feed network is sufficient to maintain the array gain over the operating bandwidth.

IV. Conclusion

The co-design of a SiGe PA integrated with a wideband PCB-based D-band antenna array is presented. The effectiveness of wirebond integration at frequencies beyond 100 GHz based on proper co-design is demonstrated. This was achieved by (i) thinning the PA IC and embedding it into a cavity in the PCB, leveling the IC and PCB to minimize the length of the bond wires, and (ii) introducing a GCPW-to-SIW transition to the antenna input to tune its impedance for maximum EIRP. Combining these steps proved to be crucial to maintain the high power and wideband nature of the integrated components. Measurement results show state-of-the-art performance with a peak gain of 26 dBi, a gain bandwidth of 23 GHz, a peak EIRP of 22.8 dBm and an EIRP bandwidth of 25 GHz.

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