

A 460 Gb/s PAM-4 Linear Distributed Driver with 105 GHz BW for TFLN Modulators in 130nm SiGe BiCMOS

Leandro da Silva^{1*}, Cedric Bruynsteen¹, Jakob Declercq¹, Armands Ostrovskis², Fabio Pittala²,
Guy Torfs¹, Nishant Singh¹, Xin Yin¹

¹IDLab, Ghent University - imec, Ghent, Belgium

²Keysight Technologies Deutschland GmbH, Böblingen, Germany

*leandro.dasilva@imec.be

Abstract— We present a linear single-ended distributed driver implemented in 130nm BiCMOS process with f_T/f_{max} of 470/650 GHz, designed for single-ended push-pull thin-film lithium niobate (TFLN) traveling-wave Mach-Zehnder modulators (TW-MZMs). High-linearity and low group-delay variation are achieved by using 10 cascode gain cells with large emitter degeneration resistors (23.5 Ω) and no capacitive peaking. The driver delivers an overall gain of 14.5 dB, a bandwidth of 105.7 GHz, and an output swing of 2.25 Vpp. Time domain experiments demonstrate 232 Gbaud PAM-4 (464 Gbps gross aggregate rate) with the use of offline DSP.

Keywords— amplifiers, distributed amplifiers, BiCMOS.

I. INTRODUCTION

The rapid growth of cloud services, real time large-language models and high fidelity media streaming is driving demand for higher single-lane optical data rates. To achieve these demands, the optical transmitters must push well into the 200+ Gbaud symbol rates, while meeting stringent linearity and power budgets [1], [2]. At device level, the electro-optical modulators (EOMs) and their associated drivers play a critical role in determining the achievable link bitrate. Thin-film lithium niobate (TFLN) modulators offer a potentially faster alternative to silicon photonics (SiPh) modulators while remaining highly efficient. While SiPh devices are still attractive for CMOS compatibility and dense integration, their modest bandwidth, low extinction and high insertion loss can pose a challenge for high baudrates [3]. TFLN provides lower optical loss, a smaller $V_\pi L$ and a natural support for single-ended push-pull drive, which halves the required voltage swing as illustrated in Fig. 1 and has demonstrated the capability to be heterogeneously integrated on SiPh wafers [4], [5].

In order to support smaller footprints and increased data rates, shorter TFLN modulators can be used. These require wideband drivers with a reasonable output swing and low group-delay variation to preserve extinction ratio and avoid nonlinear phase distortion (thus easing equalization). Additionally, using TFLN modulators with a wider signal trace and narrower spacing between the electrodes reduces RF loss and boosts bandwidth and electro-optic overlap at the cost of a reduced characteristic impedance of about 40 Ω [6]. While a 50 Ω source is capable of driving such a load with minor reflections, a matched 40 Ω driver maximizes power transfer, while the wider output lines allow for a higher DC current in the distributed driver.

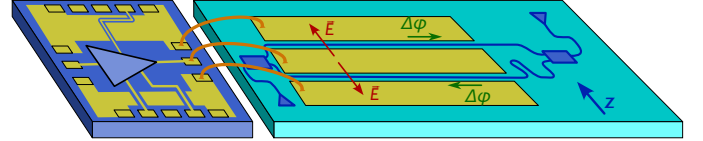


Fig. 1. Single-ended driver connected to a push-pull TFLN MZM, where the single signal electrode generates two opposing electric fields, one pointing toward and the other against the lithium niobate crystal orientation. This leads to opposite optical phase shifts in the interferometer arms, doubling modulation efficiency.

We present a linear single-ended distributed driver in a 130 nm SiGe BiCMOS process ($f_T/f_{max} = 470/650$ GHz), designed to drive a push-pull TFLN TW-MZM with 40 Ω characteristic impedance. The driver uses cascode gain cells with substantial resistive degeneration to reduce the input capacitance of each cell (thus increasing Bragg frequency and linearity), achieving an overall gain of 14.5 dB. An optimized electromagnetic (EM)-driven layout and the avoidance of capacitive peaking ensure a smooth magnitude response and minimal group-delay ripple, reducing equalization requirements. The driver is fully DC-coupled to minimize the baseline wander associated with long run-length signals, and incorporates a distributed termination to mitigate bandwidth degradation caused by reflections due to termination parasitics.

The remainder of the paper is organized as follows: section II describes the design of the driver and section III presents the measured performance and provides a comparison to other state-of-the-art distributed drivers.

II. CIRCUIT DESIGN

The driver is composed of 10 cascode gain cells which are periodically distributed along the input and output transmission lines (TLs) as shown in Fig. 2. The loaded input TL is designed for a 50 Ω characteristic impedance, while the output TL targets 40 Ω . To achieve these values, the input TL uses the minimum allowed width of 1.6 μm , whereas the output TL adopts a width of 5 μm as a trade-off between current density, characteristic impedance and phase matching with the input TL. Both TL segments have the same length of 150 μm to facilitate the layout and to avoid the need for bends.

Increasing the degeneration resistor R_e enhances linearity and reduces each gain-cell's input capacitance, improving bandwidth, but also reduces the cell's transconductance G_m ,

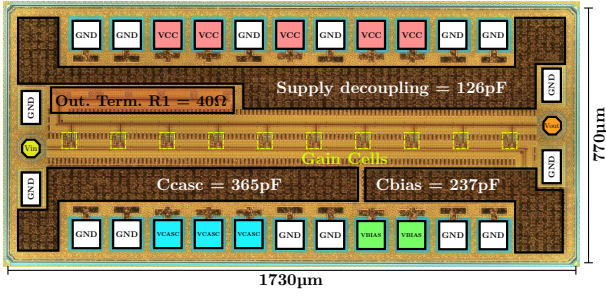


Fig. 6. Die micrograph showing the location of input and output GSG pads, gain cells, output termination and decoupling nets.

maximum achievable data rate. Small-signal S-parameters were measured with the chip's internal $40\ \Omega$ termination sourcing the DC current, while compression power sweeps and time-domain measurements were taken with an external bias-T providing the output DC bias to avoid supply clamping. When biasing through the internal output termination, the power consumption of the driver amounts to 650 mW (100 mA at 6.5 V), while it is 167.5 mW (67 mA at 2.5 V) when a bias-T is employed to set the output voltage level and supply the current.

A. VNA Measurements

Fig. 7 shows the measured and simulated S-parameters for the designed driver. Measurements were performed with a Keysight N5247B PNA-X, using N5293AX03 frequency range extenders and MPI's T110A GSG100 probes, covering a frequency range from 10 MHz to 110 GHz. The achievable bandwidth is 105.7 GHz, with a low-frequency gain of 14.5 dB. Good input matching is achieved, with an S11 below -14 dB for the entire frequency range, while S22 is under -10 dB up to 51 GHz, having a peak of -4.5 dB at 80 GHz. Group delay variation is ± 5.7 ps for the entire frequency range. Gain compression is shown in fig. 8 for 1, 30 and 50 GHz, achieving output-referred 1-dB compression points of 12.2, 13.1 and 12.0 dBm, respectively (corresponding to voltage swings of 2.25 to 2.56 Vpp across $40\ \Omega$).

B. Time-Domain Experiments

To perform time-domain experiments, we combined Keysight's M8159A frequency-domain interleave unit (FDIU) with the M8199B arbitrary waveform generator (AWG) to form a single equivalent AWG with an effective sampling rate of 512 GSa/s and a usable bandwidth beyond 120 GHz, as shown in Fig. 9. This source delivers a pseudo-random binary sequence (PRBS15) of PAM4 symbols filtered by a raised-cosine (RC) filter (roll-off = 0.01) and a channel correction filter applied up to half the baud rate ($f_{corr} = \text{baud}/2$). Clock and data for the FDIU are provided from four channels of the M8199B. The FDIU drives the device under test (DUT) through a bias-T (BT110R) used as DC-block and an MPI T110A RF probe. The DUT output is then probed and a stable DC voltage level is set via a second bias-T. The N1046A sampling head captures the data at 32 samples per

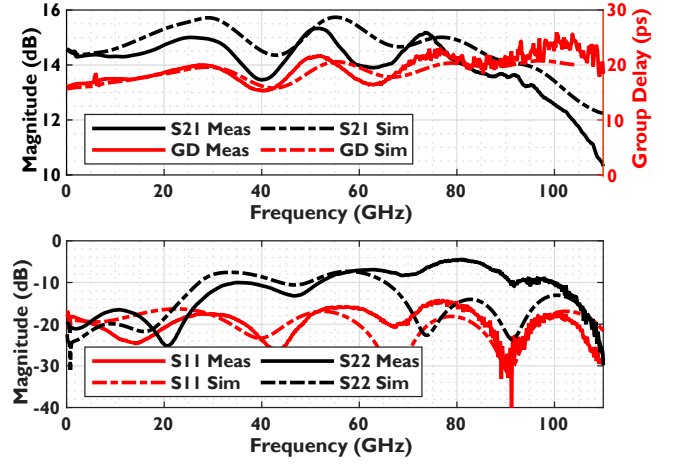


Fig. 7. S-parameter simulation and measurement results. The low-frequency gain is 14.5 dB and the bandwidth is 105.7 GHz. Input matching (S11) is below -14 dB for the whole band. S22 stays below -10 dB up to 51 GHz. Group delay is within ± 5.7 ps for the measurement range.

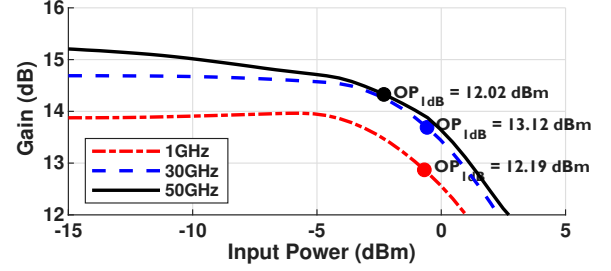


Fig. 8. Gain compression measurement for 1, 30 and 50 GHz. Markers show output referred 1 dB compression points.

symbol and the post-processing includes a 50-tap feed-forward equalizer (minimum mean-squared error with Wiener-Hopf solution) and eye diagram plotting. The resulting eye diagrams are shown in Fig. 10, with open eyes up to 232 GBd, or 464 Gbps.

C. Comparison to State-of-the-Art

Table 1 compares the performance of the proposed driver alongside recent state-of-the-art implementations. Among SiGe designs, this work achieves higher gain-bandwidth product (GBP) than [3] and [7] while delivering a $3\times-10\times$ improvement in energy efficiency.

Although AC-coupled SiGe [8] and InGaAs [9] designs report higher GBP via capacitive division, their high-pass response induces severe baseline wander for PAM4 signals. Our work prioritizes a DC-coupled response to eliminate this penalty, while maintaining a competitive P_{1dB} of 13.1 dBm, outperforming both RFSOI [10] and InGaAs [9] alternatives.

IV. CONCLUSION

We present a single-ended distributed driver for TFLN push-pull TW-MZM modulators, achieving 14.5 dB gain and a 105.7 GHz 3-dB bandwidth. Electrical measurements demonstrate a flat group delay, with ± 5.7 ps variation across the measurement band and a 464 Gbps data rate, meeting the

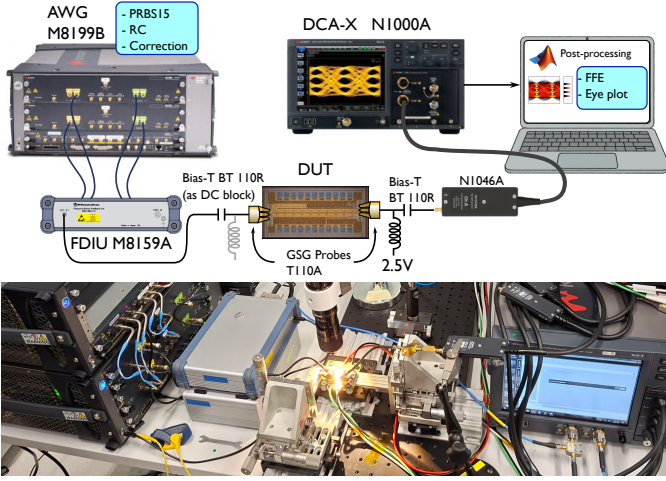


Fig. 9. Block diagram (top) and picture (bottom) of the setup for time domain measurements.

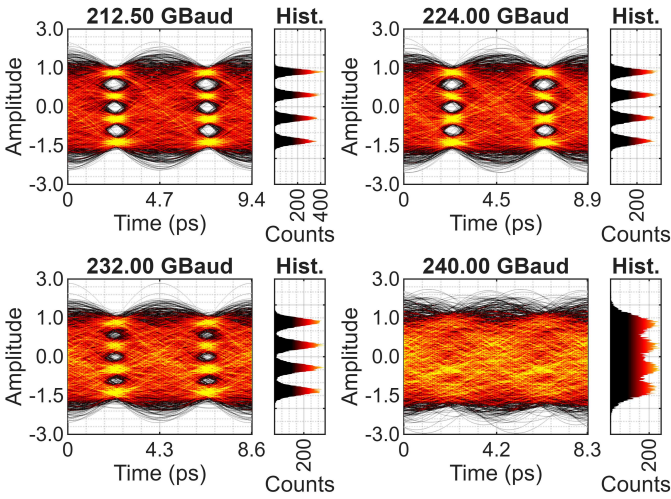


Fig. 10. Eye diagrams after equalization showing operation up to 232 Gbaud.

required 400 Gbps/lane required for next-generation optical communications. The total power dissipation is 650 mW for small-signal characterization using internal terminations to 167.5 mW during large-signal data transmission via an external bias-tee. Our design achieves the highest GBP among reported DC-coupled drivers, while maintaining superior power efficiency (361 fJ/bit) at 464 Gbps.

Table 1. Comparison with state-of-the-art distributed drivers.

Ref.	Venue/Year	Tech.	Gain dB	BW GHz	P _{DC} mW	GBP GHz	P _{1dB} dBm	Efficiency pJ/bit
This	RFIC/2026	SiGe	14.5	0-106	168	561	13.1	0.361
[3]	RFIC/2025	SiGe	15.0 ^{&}	0-65	810	366	16.8 ^a	3.62
[7]	GeMiC/2025	SiGe	10.8 ^{&}	0-80	390	277	10.3	0.975 ^a
[8]	EuMIC/2022	SiGe	19.0	1-170	350	1515	14.0	N.A.
[9]	MWTL/2025	InGaAs	11.7	4-420	115	1600	2.5	N.A.
[10]	JSSC/2025	RFSOI	8.8	0.5-137	182	376	12.9	N.A.

^a - estimated from graphs/data

[&] - differential design

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