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Evaluation of a Plasmon-Based Optical Integrated Circuit for Error-Tolerant Streaming Applications

SAMANTHA LUBABA NOOR[1], XUAN WU[2], DENNIS LIN[3], POL VAN DORPE[3], FRANCKY CATTHOOR[3], PATRICK REYNAERT[2] (Senior Member, IEEE), and AZAD NAEEMI[1] (Senior Member, IEEE)

[1]Georgia Institute of Technology, Atlanta, GA 30332 USA
[2]KU Leuven, 3000 Leuven, Belgium
[3]IMEC, 3001 Leuven, Belgium

CORRESPONDING AUTHOR: S. L. NOOR (lubaba.noor@gmail.com)

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ABSTRACT In this work, we have designed and modeled an integrated plasmonic computing module, which operates at 200 GHz clock frequency for high-end streaming algorithm applications. Our work includes designing the individual optical components (modulator, logic gate, and photodetector) and high-speed electronic driver circuits and integrating the components considering their interactions. We have also holistically evaluated the system-level performance of the computing module, taking into account various factors such as power consumption, operational speed, physical footprint, and average temperature. Through rigorous numerical analyses, we have found that with the existing technology and available materials, the plasmonic computing module can best achieve a bit-error-ratio (BER) of 10^{-1}. The performance can be improved by using a high electrooptic coefficient material in the phase shifter and increasing the driver circuit's swing to greater than 1 V.

INDEX TERMS Bit-error-ratio (BER), optical computing, plasmonic integrated circuit, plasmonics, sub-3 nm FINFET technology, system-level modeling, thermal analysis.

I. INTRODUCTION

PLASMON-BASED optical computing holds significant promise for error-tolerant streaming applications, including machine learning at the edge. Inspired by the unique opportunities of plasmonics for information processing, extensive theoretical, and experimental investigations on plasmonic devices have been carried out over the past decade [1], [2], [3], [4], [5]. However, to date, most research efforts on plasmonics for computing have focused on demonstrating or designing devices as stand-alone components in proof-of-principle experiments using CMOS-incompatible materials like Au or Ag [6], [7]. However, integration of plasmonics with Si photonics and Si-CMOS electronics requires full technological compatibility with the mainstream CMOS front-end fabrication process. Moreover, consideration of component interaction within an integrated system is crucial during device design, as the optimization of a device relies heavily on connecting device parameters. Also, the metal losses in plasmonic devices (which is a major bottleneck of plasmonics up to now) may lead to a potential thermal showstopper of a system because the maximal temperature could become too high for reliable operation. Therefore, thermal analysis should be included during device and system design. Furthermore, designing and integrating high-speed electronic circuits for driving plasmonic devices and data readouts is essential. Nevertheless, there is not any systematic and comprehensive research work that has addressed all major aspects of a plasmonic computing system holistically.

In this work, we have designed and modeled an integrated plasmonic computing module, including electronic driver and detection circuitry and carefully included/studied all the research gaps mentioned in the previous paragraph. We use the IMEC sub-3 nm FinFET technology with a minimum finger width of 5 nm [8], [9] for the driver circuit design, and simulations are based on hardware-influenced

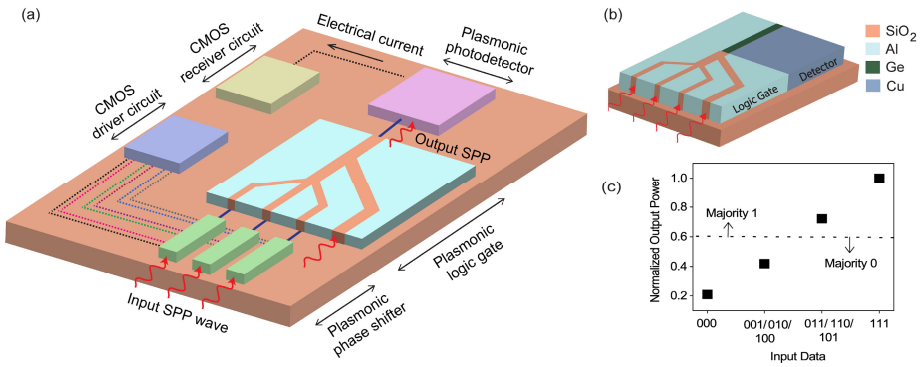

FIGURE 1. (a) Representation of a plasmonic computing module. The phase shifter, photodetector, and CMOS circuits are represented as black boxes. The optical and electrical connections are shown as solid and dotted lines, respectively. (b) Integrated logic gate and photodetector. (c) Normalized output power of the logic gate for different inputs.

Technology Computer-Aided Design (TCAD)-based models. Using extensive numerical analysis, we evaluate the system-level performance of the computing module by considering factors such as throughput, energy consumption, footprint, and device temperature.

II. PLASMONIC COMPUTING MODULE

The designed plasmonic computing module, shown in Fig. 1(a), consists of plasmonic phase shifters/modulators that encode data to plasmonic signal/surface plasmon polariton (SPP), a plasmonic logic gate for wave-computation, a plasmonic photodetector to convert the logic gate output to an electrical signal, and CMOS electronic driver and receiver circuits. We will first provide a brief introduction of the individual components.

A. PLASMONIC PHASE SHIFTER FOR PHASE MODULATION

A metal–insulator–metal (MIM) slot waveguide (WG)-based phase shifter is employed in the computing module to encode data for transmission into the plasmonic domain. We use phase modulation as it allows varying applications of the logic gate in the computing system, which is inaccessible in amplitude modulation-based wave computing [10]. The considered phase shifter was experimentally demonstrated by Haffner et al. [11]. The slot material of the WG is an organic chromophore, which is a highly nonlinear $\chi^{(2)}$ material. By applying a voltage between the metal claddings or electrodes of the plasmonic WG, the effective index ($n_{\text{eff,PS}}$) of the WG and phase of the plasmonic carrier signal can be controlled due to the linear electrooptic effect in the chromophores. The change in effective index ($\Delta n_{\text{eff,PS}}$) is high when the slot is narrow due to the presence of highly confined SPPs and enhanced interaction enabling short μm-long phase shifters. As a result, the MIM slot width is set at $d = 60$ nm. The height of the plasmonic WGs is maintained at 100 nm in all the devices of our design.

Due to large $\Delta n_{\text{eff,PS}}$, the voltage–length product of the plasmonic phase shifter ($V_\pi L_\pi$) can be several orders of magnitude smaller than the Si-based photonic phase shifters, resulting in far more compact modulators. For example, photonic phase shifters exhibit $1000's$ of Vμm [12] of voltage-length product. On the other hand, for the demonstrated plasmonic phase shifter [11], the voltage-length product can be as low as $V_\pi L_\pi = 50$ Vμm when the organic electrooptic (OEO) material and metal are DLD-164 and Au, respectively. The propagation loss of the MIM WG is calculated using the experimental ellipsometry data from [11]. The calculated propagation loss of the MIM WG is 0.63 dB/μm. Although the narrower slot width of the MIM WG results in an increased propagation loss, the gain in $\Delta n_{\text{eff,PS}}$ overcompensates for the losses [11]. It is important to note that although Au is used for the phase shifter in [11], Cu results in similar WG propagation properties and can be utilized to ensure Si CMOS process compatibility.

The main design parameters of the phase modulator are the input optical power, length, and driving voltage. There are trade-offs among these parameters. For example, a short modulator reduces the capacitive load for the driver circuit and loss and also makes the designs more compact. However, it will require a larger voltage to get a specific phase shift, necessitating a more complex driving circuit. Hence, the optimal choice should be made at the system level.

B. PLASMONIC LOGIC GATE

The main logic element in the computing module is a three-input plasmonic logic gate [10] [Fig. 1(b)], which is based on Al-SiO_2-Al MIM WGs. Three plasmonic phase shifters are coupled to the three input WGs of the logic gate to phase encode the SPP signals and define the input data. Ideally, the SPP signal is encoded such that the phase difference between bit 0 and bit 1 is $\Delta\phi = 180°$. The details of the logic gate and its operation are provided in the supplementary section S1. The gate has four possible output levels, depending on the number of bit 1 present in input data. As a result, it can implement non-Boolean functions like majority operation, as shown in Fig. 1(c) and threshold logic function [13]. The calculated insertion loss of the logic gate is 3.3 dB, which includes propagation loss in the plasmonic WGs and losses in the bends and junctions of the logic gate.

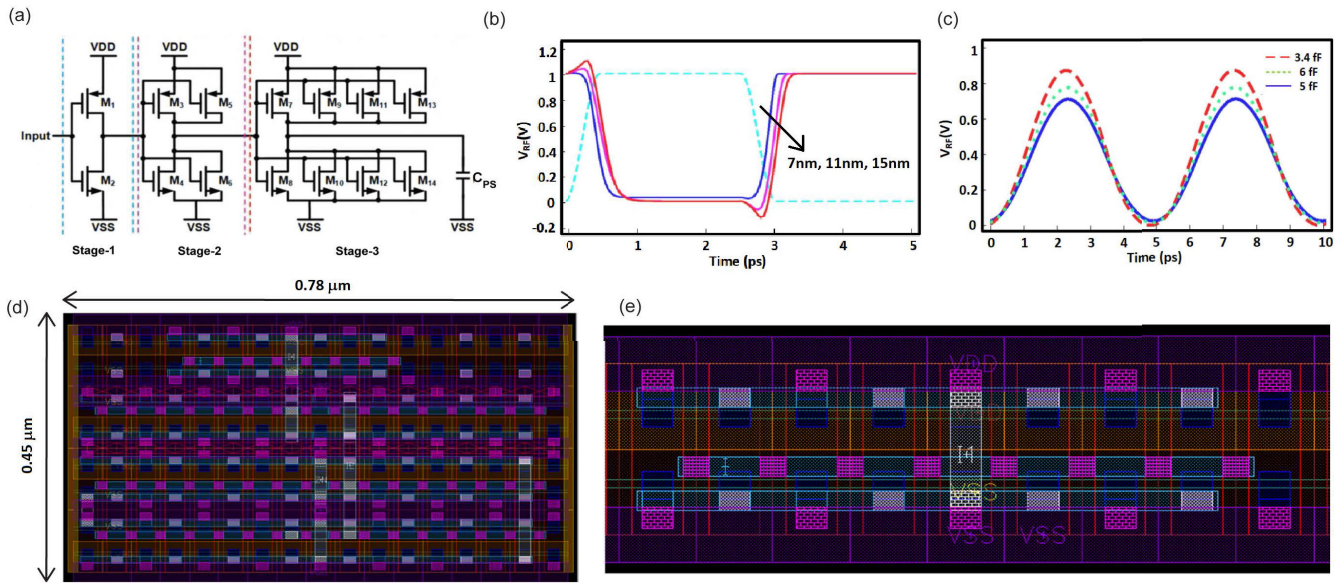

FIGURE 2. **(a) Representative example of a CMOS buffer circuit. (b) Output of an inverter with different transistor gate lengths. (c) Output of the buffer circuits with different capacitive loads. (d) Layout of a buffer with inverters ratio of 8:16:32 that drives a 3.4 fF phase shifter load. (e) Zoomed-in view of the first stage of the buffer of (d).**

C. PLASMONIC PHOTODETECTOR

The output of the plasmonic logic gate is converted to an electrical signal using an Al-Ge-Cu metal–semiconductor–metal (MSM) WG-based plasmonic photodetector. We have integrated the photodetector with the logic gate and optimized the photodetector's configuration in a previous work, considering the trade-off between responsivity and bandwidth [14]. The responsivity and intrinsic bandwidth (transit time-limited) of the optimized photodetector are $\mathcal{R} = 0.31$ A/W and 250 GHz, respectively [14]. A summary of the photodetector is provided in the supplementary section S1.

D. TRANSIMPEDANCE AMPLIFIER

The TIA converts the photodetector's output current to voltage. To design the TIA, we have employed the IMEC sub-3 nm FinFET technology. Based on our simulation, the TIA design ensures a high RC-limited bandwidth ($\approx$200 GHz) of the loaded photodetector (TIA acts as the load). This enables high-speed operation at the system level. The calculated input resistance and capacitance of the TIA are $R_{\text{TIA}} = 1.2$ KΩ and $C_{\text{TIA}} = 0.43$ fF, respectively. A summary of our proposed design is also provided in S2, and more details will be published later.

E. DRIVER CIRCUIT OF THE PHASE SHIFTER

We indicated in Section II-A how the phase shifter's length affects the CMOS driving circuit. As there are trade-offs between the phase shifter's capacitance and driving voltage, in this section, we look at various driving voltages and phase shifter capacitances.

The RF signal, which drives the phase shifter, is generated by a high-speed CMOS comparator circuit. The large capacitance of the phase shifter suppresses the comparator's output voltage. As a result, an inverter chain-based buffer circuit [15], [16] is designed to drive the phase shifter. Fig. 2(a) shows the representative structure of a buffer circuit with the inverter ratio of 1:2:4. The number of stages and the number of inverters in each stage depends on the required output voltage (V_{RF}) and the capacitance of the phase shifter (C_{PS}). To work with the 200 GHz clock frequency, the buffer's signal propagation delay plays an important role. Generally, the delay can be minimized with a larger supply voltage (VDD) or a smaller CMOS gate length. The optimized buffer configuration depends on the trade-off among propagation delay, power consumption, required output voltage, and footprint.

Capturing the data at 200 Gb/s is too challenging to complete in mature CMOS technology generations due to the low f_t/f_{max}. Therefore, we use the IMEC sub-3 nm equivalent node with a minimum finger width of 5 nm to design the buffer. The transistor's leakage plays a dominant role in IMEC sub-3 nm technology. Due to leakage, the buffer consumes more power to get the required output voltage (V_{RF}). Three transistor models [high voltage transistor (HVT), standard threshold voltage transistor (SVT), and low voltage transistor (LVT)] with different threshold voltages and speeds are considered to alleviate the leakage issue. HVT (LVT) models have high (low) threshold voltages, resulting in lower (higher) power consumption but low (high) switching speed. In comparison, SVT models have standard threshold voltages with a moderate delay and power consumption. Although LVT models ensure high-speed operations, due to its enhanced leakage, we choose SVT model. Transistor gate length also affects leakage

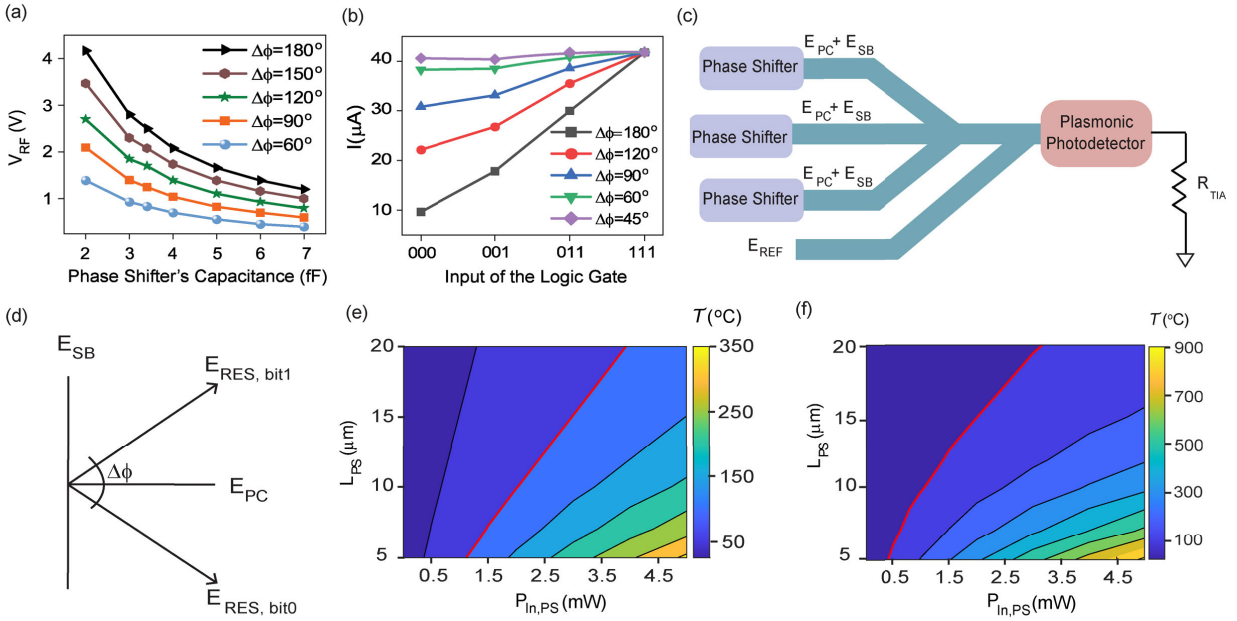

FIGURE 3. (a) Driving voltage for the varying capacitance of the phase shifter. (b) Effect of the phase difference between bit 0 and bit 1 ($\Delta\phi$) on the output of the plasmonic logic gate. The total input power of the plasmonic logic gate is assumed 0.3 mW. (c) Integration of plasmonic devices including a three-input logic gate connected to phase shifters and a plasmonic photodetector with transimpedance amplifier (TIA) load. The field signals labeled are for 111 input. (d) Definition of bit 0 and bit 1 using the modulated (E_{SB}) and unmodulated (E_{PC}) output fields of the phase shifter. The average temperature in the plasmonic devices for varying length and input power of the phase shifter when (e) $\Delta\phi = 60°$ and (f) $\Delta\phi = 180°$. The 100 °C temperature limit is shown using the red line.

current: shorter gate lengths increase speed but also raise leakage current. For example, Fig. 2(b) shows the simulated results of an inverter's performance with varying transistor (SVT model) gate lengths. The output swing has decreased with the 7 nm gate length due to leakage. From our analysis, we select the 11 nm transistor gate length in the buffer design, which is a sweet spot for our target realization.

Using the SVT transistor model with 11 nm gate length, the buffer circuit is designed for varying load/phase shifters. For example, Table 1 summarizes the performance of three buffers for driving two different phase shifters at 200 GHz clock frequency and Fig. 2(c) shows the output voltage waveforms. The buffer circuit's performance is simulated with postlayout results in Cadence. Fig. 2(d) shows the layout of the buffer (8:16:32) driving a 3.4 fF load capacitance and for clarity, Fig. 2(e) shows the layout of the first stage (eight times inverter) of the buffer. As the gates of pMOS and nMOS within each stage are connected together, the upper part of the gate is used for pMOS, and the lower part of the gate is used for nMOS with shared gate contact to save footprint. In the schematic simulation, the buffer with a 1:2:4 inverters sizing ratio has a similar output voltage swing with an 8:16:32 inverters sizing ratio after postlayout simulation. So, the parasitics of interconnection play a dominant role in circuit performance. In advanced nodes, it is essential to do the design iteration and optimization based on the layout extracted parasitics.

Although we have shown three representative cases of buffer in Table 1, the buffer circuit needed for the plasmonic computing module is primarily defined by the phase shifter's configurations (C_{PS} and V_{RF}). Fig. 3(a) studies the required V_{RF} with changing C_{PS}. To get this figure, we first calculate C_{PS} for varying lengths of the phase shifter, L_{PS} (details in the supplementary section S3). We next find the required V_{RF} to get a specific phase shift ($\phi = \Delta\phi/2$) using the voltage-length product ($V_{RF} = V_\pi L_\pi/\phi L_{PS}$). It can be seen from Fig. 3(a) that with increased C_{PS}, the required V_{RF} decreases for a fixed $\Delta\phi$ due to the increase in the phase shifter's length. However, the increase in C_{PS} significantly suppresses the output swing of the buffer, as the buffer should be larger to drive the higher capacitance. It also increases the power consumption in the buffer circuit and signal propagation delay. Moreover, loss in the phase shifter increases due to the increase in the phase shifter's length. Fig. 3(a) also shows that the required V_{RF} decreases with smaller $\Delta\phi$ for a fixed phase shifter configuration. However, as $\Delta\phi$ is reduced, the output levels of the plasmonic logic gate come closer, as shown in Fig. 3(b). As a result, we do not consider $\Delta\phi < 60°$ in our design.

From the discussion above, we understand that several key system-level trade-offs should be considered during the design of the buffer circuit related to the required V_{RF}, energy consumption and delay in the buffer, chip size, power loss in the phase shifter, and resolution (spacing between adjacent levels) of the plasmonic logic gate's outputs. Since the problem is multifaceted, an integrated system consisting of all the components needed to build a plasmonic logic is required for the analysis.

III. MODELING AND ANALYSIS OF THE PLASMONIC INTEGRATED SYSTEM

In this section, we analytically model and evaluate the system-level performance of an integrated computing module consisting of the plasmonic phase shifter, a three-input logic gate, and a plasmonic photodetector with the TIA load, as shown in Fig. 3(c).

A. ANALYTICAL MODEL

1) DEFINITION OF BIT 0 AND BIT 1

The analytical model of the output of the phase shifter is shown in supplementary section S4. The output of the phase shifter (E_{RES}) is the superposition of the generated/modulated (E_{SB}) and carrier/unmodulated (E_{PC}) signals. Using (S4), the amount of signal phase shift at the output of a phase shifter of length L_{PS} can be written as

$$\phi = \tan^{-1}\left(\frac{\omega_{\mathrm{SB1}} + \omega_{\mathrm{SB2}}}{\sqrt{2}\omega_{\mathrm{PC}}} \tan\left(\frac{V_{\mathrm{RF}}\kappa\omega_{\mathrm{pc}}L_{\mathrm{PS}}}{d}\right)\right) \quad (1)$$

E_{RES} acts as the input of the logic gate in the integrated system. We define that E_{RES} corresponds to bit 1 when V_{RF} is positive and bit 0 when V_{RF} is negative. Using (S4), the unmodulated carrier field, E_{PC} is the same for bit 0 and bit 1, whereas the modulated field, E_{SB} has an opposite sign, which can be visualized in Fig. 3(d). Ideally, for the operation of the logic gate, we need to choose a voltage–length combination of the phase shifter such that $\phi = \pm 90°$, resulting in $\Delta\phi = 180°$. For example, $V_{\mathrm{RF}} = 2.5$ V and $L_{\mathrm{PS}} = 10$ μm or $V_{\mathrm{RF}} = 1$ V and $L_{\mathrm{PS}} = 25$ μm results in $\Delta\phi = 180°$.

2) OUTPUT POWER AND POWER LOSS OF THE INTEGRATED DEVICES

Using (S4), the total input power of the three arms of the logic gate can be expressed as

$$3P_{\mathrm{In,PS}} \exp(-2\alpha L_{\mathrm{PS}})(\cos^2\theta + 2\sin^2\theta). \quad (2)$$

Here, $\theta := V_{\mathrm{RF}}\kappa\omega_{\mathrm{pc}}L_{\mathrm{PS}}/d$ and $P_{\mathrm{In,PS}}$ is the input power of a phase shifter. The output power of the integrated devices can be found by multiplying (2) by the transmission factor of the logic gate and the photodetector. The output power of the integrated devices can be expressed as

$$P_{\mathrm{Out,PD}} = \left[3P_{\mathrm{In,PS}} \exp(-2\alpha L_{\mathrm{PS}})(1 + \sin^2\theta) + P_{\mathrm{REF}}\right] \times T_{\mathrm{Maj}} \times \eta \times \exp(-2\alpha_{\mathrm{PD}}L_{\mathrm{PD}}). \quad (3)$$

Here, the bracketed term represents the total input power of the logic gate. T_{Maj} is the transmission coefficient that considers the loss in the gate, including the loss in the MIM WG, WG bending loss, and loss in the WG junctions. η is the coupling efficiency between the logic gate and the photodetector and P_{REF} represents the input signal power at the reference arm. Moreover, $2\alpha_{\mathrm{PD}}$ and L_{PD} are the power attenuation constant and length of the plasmonic photodetector, respectively.

The total power loss of the integrated devices can be found by subtracting the output signal power from the input power. The total loss of the integrated devices is

$$P_{\mathrm{Loss}} = 3P_{\mathrm{In,PS}} + P_{\mathrm{REF}} - P_{\mathrm{Out,PD}} \quad (4)$$

P_{Loss} contributes to heat generation in the devices due to the power absorbed in the metal of the plasmonic WGs. Excessive heat can lead to device instability, degradation, and reduced performance. Therefore, it is important to find how much heat is generated and hence, we first perform a thermal analysis of the integrated system.

B. THERMAL ANALYSIS

To find out the average temperature in the plasmonic devices, we consider a 1-D thermal model. We assume that the cooling method can draw out all the generated heat, bringing the temperature at the bottom of BOX (bottom SiO_2) to ambient temperature ($\mathcal{T}_{\mathrm{Amb}} = 25$ °C). For high-performance and high-power devices, where heat flux density can reach 1 KW/cm^2 [17], [18] or higher, direct liquid cooling is used. For example, IMEC's liquid jet impingement cooling method with locally distributed outlets [19] has the capability of extracting 500 W/cm^2 of heat flux [20]. Further improvement of the cooler is expected to enable more than 1 KW/cm^2 heat removal [21], and we assume that the cooling method can handle heat flux density, $Q_{\mathrm{Flux}} = 1$–1.5 KW/cm^2.

The effectiveness of dissipating the generated heat and cooling the devices depends on the thermal resistances of the BOX layer ($R_{\mathrm{Th,SiO_2}}$). The thermal resistance of the BOX layer can be calculated using the following relation:

$$R_{\mathrm{Th,SiO_2}} = \frac{h_{\mathrm{BOX}}}{K_{\mathrm{SiO_2}} \times \mathrm{Area}}. \quad (5)$$

Here, $K_{\mathrm{SiO_2}} = 1.38$ W/mK, which is the thermal conductivity of SiO_2. h_{BOX} is the thickness of bottom SiO_2 and Area represents the total footprint of the devices. Using the 1-D model, the average temperature in the plasmonic devices can be found as

$$\mathcal{T} = \mathcal{T}_{\mathrm{Amb}} + R_{\mathrm{Th,SiO_2}} \times P_{\mathrm{Loss}}. \quad (6)$$

The average temperature in the plasmonic devices is calculated for varying length and input power of the phase shifter, as shown in Fig. 3(e) and (f). For a fixed input power, as L_{PS} increases, the average temperature decreases due to the increase in area that reduces the thermal resistance. Moreover, temperature increases with the increase of $\Delta\phi$ due to the increase in power loss associated with longer phase shifter.

The properties of the organic material used in the phase shifter degrade if the devices are heated up beyond 100 °C. To keep the average temperature below 100 °C, there is a limit on the maximum tolerable energy dissipation and consequently, maximum input optical power. From Fig. 3(e) and (f), we can find the maximum limit of input optical power that ensures $\mathcal{T} < 100$ °C. We use this information in Section III-C2 to select the system design space.

C. SYSTEM ERROR PERFORMANCE

1) SIGNAL-TO-NOISE RATIO

To analyze the system error performance, we consider the majority operation for the logic gate. The decision of the majority operation (majority 0/majority 1) mainly depends on I_{110}, I_{001}, and the noise associated with these levels. As a result, we first find the output power of the majority gate connected to three phase shifters for 110 and 001 input combinations. Using Fig. 3(c), the output field of the gate for 110 input is (assuming lossless)

$$E_{\text{Out},110} = E_{\text{SB}} + 3E_{\text{PC}} + E_{\text{REF}} \tag{7}$$

E_{REF} is the field in the reference arm of the gate and we assume, $E_{\text{REF}} = 3E_{\text{SB}}$. In (7), though we add the fields, at the output node, the field strength of the middle straight arm/WG is different compared to the fields of the upper and lower bent arms/WGs of the logic gate.

The total signal power at the output of the majority gate, consisting of the modulated and unmodulated signal is

$$P_{\text{Tot},110} \propto T_{\text{Maj}} \left|(E_{\text{SB}} + 3E_{\text{PC}} + E_{\text{REF}})\right|^2. \tag{8}$$

Here, we account for the loss in the logic gate as a whole by multiplying by the factor T_{Maj}. Since E_{SB} is the modulated signal, the modulated output signal power is

$$P_{\text{Mod},110} \propto T_{\text{Maj}} \left(|E_{\text{SB}}|^2 + 2|E_{\text{REF}}E_{\text{SB}}|\right) \tag{9}$$

$P_{\text{Mod},110}$ can be converted to I_{110} current level using the responsivity ($\mathcal{R}$) of the plasmonic photodetector. In practice, I_{110} and I_{001} current levels will fluctuate due to the presence of noise in the system. The signal-to-noise ratio (SNR) associated with 110 input is

$$\text{SNR}_{110} = \frac{I_{110}^2}{i_{\text{Sh},110}^2 + i_{\text{Th}}^2}. \tag{10}$$

Here, I_{110} is the current for 110 input. $i_{\text{Sh},110}^2$ and i_{Th}^2 are the shot noise and thermal noise current densities for 110 input, respectively, and can be calculated as

$$i_{\text{Sh},110}^2 = 2q\left(I_{\text{Dark}} + I_{110}\right) N_{\text{BW}} \tag{11}$$

$$i_{\text{Th}}^2 = \frac{4K\mathcal{T}}{R_{\text{TIA}}} N_{\text{BW}} \tag{12}$$

N_{BW} represents the noise bandwidth and equals $(\pi/2)\times$ system bandwidth. R_{TIA} is the load resistance of the detector or input resistance of the TIA, and $\mathcal{T}$ is the temperature.

Since the modulated signal contributes to the signal power and both modulated and unmodulated signal contribute to the shot noise, (10) can be written as

$$\text{SNR}_{110} = \frac{\left(\eta\mathcal{R}P_{\text{Mod},110}\right)^2}{q\pi \times \text{BW}\left(\eta\mathcal{R}P_{\text{Tot},110} + I_{\text{Dark}}\right) + \left(2\pi K\mathcal{T} \times \text{BW}\right)/R_{\text{TIA}}}. \tag{13}$$

Similarly, we can find the modulated and total output signal power and SNR for the 001 input case.

TABLE 1. Parameters of the buffer circuit for different capacitive load.

Inverter ratio	Delay ps	Power mW	Output voltage V_{RF} V	Footprint μm^2	Load capacitance C_{PS} fF
8:16:32	3.19	2.5	0.87	0.351	3.4
12:24:48	3.25	3.4	0.78	0.572	6
7:14:28	3.31	2.3	0.7	0.311	5

TABLE 2. Required input optical power, $P_{\text{In,PS}}$ (mW) to reach a specific BER. $V_\pi L_\pi$ = 50 Vμm.

$\Delta\phi$	L_{PS} μm	V_{RF} V	BER 10^{-4} $P_{In,PS}$ mW	BER 10^{-3} $P_{In,PS}$ mW	BER 10^{-2} $P_{In,PS}$ mW	BER 10^{-1} $P_{In,PS}$ mW
60^o	10	0.83	5.7	3.8	2.5	0.75
	12	0.7	7.7	5.1	3.3	0.9
90^o	15	0.83	2.75	1.8	1.3	0.4
120^o	20	0.83	2.3	1.7	1.1	0.5

Fig. 4(a) and (b) shows the contour plots of SNR_{110} and SNR_{001} with varying phase shifter length and input power for system bandwidth = 200 GHz, $R_{\text{TIA}} = 1.2$ KΩ, $\mathcal{T} = 300$ K, $\mathcal{R} = 0.31$ A/W, and $\eta = 0.9$. In the figure, each data point is simulated by changing V_{RF} to ensure $\Delta\phi = 180°$. SNR $\geq$ 20 dB is usually considered an acceptable level, which is shown by the red line. Although SNR analysis gives insight of the error performance of the system, we need to calculate and separately analyze the SNR for both 110 and 001 inputs. Using a single metric, the bit-error-ratio (BER), it is possible to combine the two SNRs, which simplifies the measurement of overall system performance.

2) BER OF THE INTEGRATED DEVICES

The BER of the system (details in supplementary section S4) is

$$\text{BER} = \frac{1}{2}\,\text{erfc}\left(\frac{1}{\sqrt{2}}\frac{I_{110} - I_{001}}{\sigma_{110} + \sigma_{001}}\right). \tag{14}$$

Here, $\sigma_{110/001}^2 = i_{\text{Sh},110/001}^2 + i_{\text{Th}}^2$. Table 2 summarizes the input optical power, $P_{\text{In,PS}}$ requirement of each phase shifter of Fig. 3(c) to reach a specific BER. Since loss in the phase shifter increases with its length, $L_{\text{PS}} \leq 20$ μm is considered. Additionally, $V_{\text{RF}} < 1$ V is considered, as the supply voltage of the driving circuit is VDD $\leq$ 1 V. Moreover, $\Delta\phi \geq 60°$ is assumed to ensure enough separation between adjacent current levels. From the table, it can be seen that as BER decreases, the required $P_{\text{In,PS}}$ increases since smaller BER requires a larger separation (ΔI) between I_{110} and I_{001}, which can be achieved by injecting more power at the input. Additionally, since ΔI increases with the increase of $\Delta\phi$ [shown in Fig. 3(b)], less $P_{\text{In,PS}}$ is required to achieve the same BER with increasing $\Delta\phi$ even with longer L_{PS}.

Output with a high BER can be corrected using system-level error correction methods. The highest BER that can

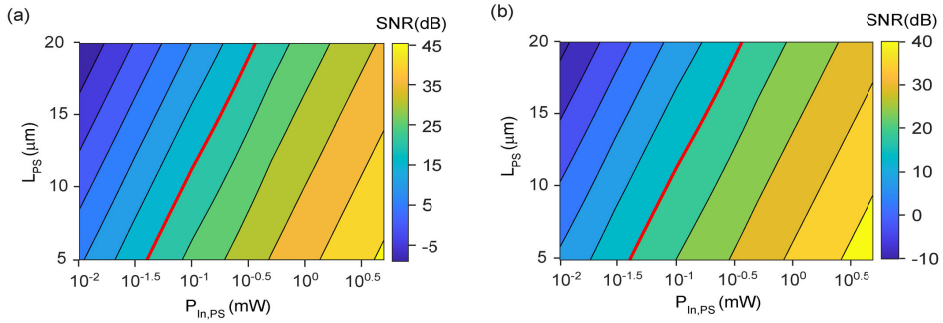

FIGURE 4. SNR of the integrated devices when the logic gate input is (a) 110 and (b) 001. $\Delta\phi = 180°$.

be corrected by a forward error correction (FEC) code and the hard-decision FEC threshold is 3.8×10^{-3} [22], [23], which means a data transmission accuracy of >99.62%. As a result, for the integrated plasmonic devices, the targeted BER is $\leq 10^{-3}$. From Table 2, we see that the lowest input optical power of the phase shifter is 1.7 mW for BER $= 10^{-3}$. However, for $P_{\text{In,PS}} = 1.7$ mW, the heat flux density, $Q_{\text{Flux}} = 4$ KW/cm^2, which is significantly higher than the heat removing capacity of the possible cooling methods. In fact, Q_{Flux} is within the target limit of 1–1.5 KW/cm^2 only when $P_{\text{In,PS}} \leq 0.5$ mW, which results in a BER of 10^{-1} that is too high for realistic error correction methods. Hence, the system, in its present state, will yield inaccurate outputs.

TABLE 3. Phase shifter configurations resulting in $Q_{\text{Flux}} \approx 1.5$ KW/cm^2 and BER $\leq 10^{-3}$. $V_\pi L_\pi = 25$ Vμm.

$\Delta\phi$	L_{PS} μm	V_{RF} V	$BER = 10^{-4}$ $P_{In,PS}$ mW	$BER = 10^{-4}$ Q_{Flux} KW/cm^2	$BER = 10^{-3}$ $P_{In,PS}$ mW	$BER = 10^{-3}$ Q_{Flux} KW/cm^2
90^o	7	0.9			0.55	1.8
120^o	10	0.83	0.5	1.75	0.4 P_T=5.2	1.4
	12	0.7			0.5	1.55
150^o	12	0.87	0.42	1.45	0.33	1.1
	15	0.7			0.47 P_T=5.5	1.43
180^o	15	0.83			0.4	1.28
	17	0.74			0.5	1.45

D. SOLUTION TO IMPROVE THE BER

1) BREAKTHROUGH IN THE PHASE SHIFTER

One possible solution to achieve a BER of $\leq 10^{-3}$ is to design a phase shifter with a smaller voltage–length product ($V_\pi L_\pi$). A phase shifter with smaller $V_\pi L_\pi$ will require smaller L_{PS} for the same applied RF voltage to achieve a specific phase shift, resulting in less power loss and less heating in the system. $V_\pi L_\pi$ is inversely proportional to the electrooptic coefficient of the OEO material used in the phase shifter. Therefore, discovering a suitable OEO material may result in a smaller $V_\pi L_\pi$. For example, preliminary research studies and experiments have shown that electrooptic coefficients of over 300 pmV^{-1} are achievable for OEO materials such as HD-BB-OH/YLD124 [24], whereas the electrooptic coefficient of the OEO considered in this work is 180 pmV^{-1}.

To assess the impact of reducing $V_\pi L_\pi$, we assume $V_\pi L_\pi$(new) $= 25$ Vμm and summarize our findings in Table 3. As $V_\pi L_\pi$ is reduced, more combinations of the phase shifter configuration (L_{PS}, V_{RF}, and $\Delta\phi$) are possible that fulfill the design specifications compared to those in Table 2. However, many combinations still lead to elevated heat flux densities. In Table 3, we have compiled the phase shifter configurations that result in $Q_{\text{Flux}} \approx 1.5$ KW/cm^2.

After analyzing Table 3, it is found that with $P_{\text{In,PS}} = 0.4$ mW, $L_{\text{PS}} = 10$ μm, $V_{\text{RF}} = 0.83$ V, $V_\pi L_\pi = 25$ Vμm, and correspondingly $\Delta\phi = 120°$, the integrated system can reach BER $= 10^{-3}$ generating a heat flux density, $Q_{\text{Flux}} = 1.4$ KW/cm^2. Using the proper cooling method, the average temperature, $\mathcal{T}$ in the plasmonic devices will be below 100 °C. The phase shifter, having $C_{\text{PS}} = 3.4$ fF, can be driven by a buffer circuit of 8:16:32, which is designed in Section II-E. Additionally, the table shows that with different phase shifter configurations, the system can even achieve a BER of 10^{-4} while all the design specs are fulfilled. In Table 3, we have also calculated the total device power (P_T) including the optical input power and electrical drive power for two representative cases. To find the optical input power, we consider a laser to fiber coupling efficiency of 70%, a fiber to Si photonic WG coupling efficiency of 83% [25], and a photonic to plasmonic mode conversion efficiency of 75% [26].

2) INCREASING V_{RF} TO >1 V

Another way to improve BER is to increase the output swing of the buffer circuit or the driving voltage of the phase shifter, V_{RF} to >1 V. The standard IMEC 3 nm technology intended for regular logic with the proposed buffer circuit cannot support $V_{\text{RF}} > 1$ V with VDD $= 1$ V. So, instead, we aim to use I/O devices, which are also developed for 3 nm node, or employ a stacked inverter circuit topology with higher VDD support [27]. The latter is listed as future work now. In Table 4, we compile the phase shifter configurations that result in BER $\leq 10^{-3}$ when $1 < V_{\text{RF}} < 1.5$ V and $V_\pi L_\pi = 50$ Vμm.

TABLE 4. Phase shifter configurations resulting in BER ≤ 10^{-3}. $V_\pi L_\pi$ = 50 Vμm and 1 < V_{RF} < 1.5 V.

$\Delta\phi$	L_{PS}	V_{RF}	$BER = 10^{-4}$		$BER = 10^{-3}$	
			$P_{In,PS}$	Q_{Flux}	$P_{In,PS}$	Q_{Flux}
	μm	V	mW	KW/cm^2	mW	KW/cm^2
120^o	12	1.4	0.63	1.96	0.45	1.4
	13	1.3			0.5	1.48
150^o	15	1.4	0.66	2	0.47	1.44
	17	1.22			0.64	1.8
180^o	17	1.47			0.55	1.6
	18	1.4			0.65	1.8

Using Table 4, we can see that a BER of 10^{-3} can be achieved with several phase shifter configurations that ensure $Q_{\text{Flux}} = 1$–1.5 KW/cm^2 and $\mathcal{T} < 100$ °C. With this solution, total consumed energy will increase due to the higher voltage required in the CMOS drivers; hence, additional trade-off analysis is needed.

IV. CONCLUSION

In conclusion, we have designed and modeled a plasmon-based optical integrated circuit consisting of plasmonic phase shifters, a plasmonic logic gate, a plasmonic photodetector, and Si-CMOS detector and driver circuits. The integrated circuit operates at 200 GHz clock frequency. We have holistically assessed the system-level performance of the integrated devices, considering plasmonic losses, operational speed, footprint, energy consumption, and device temperature. The phase shifter, featuring a $V_\pi L_\pi$ of 50 Vμm, relies on nonlinear organic material, requiring the device temperature to be maintained below 100 °C. To assess the system performance, we assume a phase shifter length of $\leq$20 μm, a driving voltage of $<$1 V, a phase difference between bit 0 and bit 1 of $\geq$60°, and a heat flux density of $\approx$1.5 KW/cm^2 ensuring $T < 100$ °C. We have found that to meet the design specifications with the existing phase shifter ($V_\pi L_\pi = 50$ Vμm), the integrated plasmonic devices achieve a BER of 10^{-1}. However, increasing the driving voltage of the phase shifter to 1.5 V or achieving a breakthrough in the phase shifter to reduce $V_\pi L_\pi$ to 25 Vμm allows the system to achieve a reasonable BER of 10^{-3} and 10^{-4}, respectively. The designed computing module has significant promise in error-tolerant streaming applications.

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