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Nanofabrication of sharp conductive diamond tip probe chips and their application in reverse tip sample scanning probe microscopy

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ABSTRACT

Recently, a new scanning probe microscopy (SPM) concept called reverse tip sample scanning probe microscopy (RTS SPM) was introduced. Here, a sample is mounted at the end of a cantilever beam and scans over a tip that is integrated into an array of hundreds of SPM tips, overcoming one of the major limitations of the SPM technique, namely, the time-consuming and experiment-interrupting manual tip exchange step. However, to fully exploit this novel approach, a chip with an array of densely packed, nanometer-sharp, and durable SPM tips is essential. Therefore, we have developed a fabrication process to integrate such an array of sharp, high aspect ratio, doped diamond tips – referred to as hedgehog full diamond tip (HFDT) – into so-called probe chips, facilitating high-resolution SPM measurements and enabling rapid and seamless sample movement from one tip to another within the RTS SPM framework. An array of pyramidally shaped, doped diamond tips is fabricated through consecutive molding and diamond deposition steps. A supporting membrane is formed by metal deposition and electroplating, followed by selective underetching of the silicon substrate to release the tip array membrane and enable probe chip assembly. Finally, a self-patterned dry etching step is employed to generate multiple nanoscopic sharp tips on top of the base diamond pyramids. In this work, we present our developed and optimized probe chip technology and demonstrate its high electrical conductivity, robustness under high tip load force, and excellent spatial resolution, rendering it highly suitable for diverse electrical SPM measurement modes.

1. Introduction

As semiconductor device structures continue to scale down to sub-10 nm dimensions, it becomes increasingly important for electrical characterization techniques to advance in tandem [1,2]. Specifically, these methods must not only deliver nanometric spatial resolution to match device scaling but also ensure reliability and efficiency compatible with current fabrication processes. Within this framework, electrical scanning probe microscopy (*E*-SPM) techniques have shown significant promise, with scanning spreading resistance microscopy (SSRM) standing out for its demonstrated capability to map doping profiles in state-of-the-art nanodevice architectures [3–5].

Despite its potential, SSRM has two major, interrelated limitations. First, its performance critically depends on the properties of the probe tip, which must possess an exceptionally sharp apex to achieve high spatial resolution, sufficient mechanical robustness to endure gigapascal-scale contact pressures, and high electrical conductivity to minimize parasitic resistance effects. To meet these requirements, highly boron-doped diamond (BDD) has become the material of choice for SSRM tip fabrication [6,7]. Over time, two principal BDD tip technologies have emerged: Coated diamond tips (CDTs) [8], which offer excellent electrical conductivity but suffer from mechanical fragility, and full diamond tips (FDTs) [9–11], which provide superior mechanical stability but at the expense of reduced conductivity. Furthermore, recent advancements have primarily focused on enhancing the sharpness and aspect ratio of both CDT and FDT designs. For CDTs, nanometer-scale apex radii have been achieved through a combination of focused ion beam (FIB) masking and subsequent plasma etching [12]. More notably, even sharper tips have been realized with FDTs through a self-patterned etching process, which produces ultra-sharp, high-aspect-ratio

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nanoscopic tips atop the pyramidal FDT structures, a configuration that is now referred to as hedgehog full diamond tip (HFDT) [13]. These improvements in tip sharpness have significantly advanced SSRM's resolution capabilities but have also exacerbated the technique's second major limitation, its inherently low throughput. Namely, sharper tips degrade more rapidly due to wear during measurements, necessitating frequent replacements to maintain data quality [14]. These replacements, being manually done and time-consuming, disrupt the measurement workflow and substantially reduce the overall efficiency of SSRM.

However, a promising solution for this has recently emerged in the form of reverse tip sample scanning probe microscopy (RTS SPM) [15]. This innovative approach inverts the conventional SPM configuration by having the sample mounted on a tipless cantilever [16], which scans over an array of fixed, integrated tips on an RTS probe chip. This reversed layout enables fast and seamless tip exchanges by simply moving the cantilever to an adjacent sharp tip, achieving up to fivefold higher throughput compared to the conventional SPM configuration [17]. In support of the new RTS approach, a robust and time-efficient nanofabrication process has been established for producing silicon-based probe chips via plasma-based dry etching [15]. These silicon tips were subsequently coated with BDD to create CDT probe chips, which have demonstrated compatibility across multiple SPM modes, including SSRM. However, these RTS-compatible CDT chips inherit the sharpness and aspect ratio limitations characteristic of coated diamond tips. To fully unlock SSRM's potential, achieving data quality comparable to conventional SSRM while harnessing the high-throughput advantages of RTS SSRM, a probe chip featuring a densely packed array of high aspect ratio nanometer-sharp tips is needed. While FIB-assisted tip sharpening can produce nanometer-scale apex radii, it remains impractical for densely packed tip arrays. Instead, a scalable self-patterning-based alternative available in standard SSRM, the ultra-sharp HFDT technology, known for its superior spatial resolution, offers a promising route. Yet critically, this technology has not been adapted for the RTS configuration.

In this paper, we therefore address the technological challenge of integrating the aforementioned FDTs into high-density tip arrays, followed by the dry etching-based tip sharpening process to realize HFDT tip array probe chips suitable for RTS SPM. Transferring the HFDT fabrication strategy to this new probe chip architecture was far from trivial and required multiple critical modifications to the nanofabrication process. We present here the optimized fabrication process in detail, with emphasis on these key adaptations, along with the resulting ultra-sharp diamond tips integrated into an RTS-compatible chip form. The morphological quality of the individual tips was characterized by scanning electron microscopy (SEM), while their functional performance was assessed through RTS SSRM measurements on a p-type doped silicon calibration sample and a GaAs nano-ridge waveguide structure. Finally, a comparative study with the reference CDT probe chip was made on a FinFET sample, demonstrating the added value of the HFDT probe chips for dopant profiling in nanoscale semiconductor devices.

2. Methods

As highlighted above, the HFDT probe chip fabrication builds upon and further expands the fabrication process for pyramidal-shaped full diamond tip (FDT) probes [11], including their conversion to HFDT probes via a final self-patterning etch step [13]. However, several key modifications had to be implemented to adapt the existing process and structural design to yield an array of tips that form an adequate probe chip, rather than just a single tip. In the following, we first describe the fabrication process in detail, followed by the design considerations that led to the final HFDT probe chip layout.

2.1. Fabrication process

Fig. 1 provides a schematic overview of the entire process, specifically tailored to the RTS configuration. First, arrays of 15 × 15 μm^2 squares are patterned into an SiO_2 hard mask layer on a 4-in. ⟨100⟩ Si wafer using conventional photolithography (tip patterning), followed by anisotropic KOH etching to create inverted pyramid molds in the silicon substrate (Fig. 1a) [18]. The SiO_2 mask is then removed, and a highly boron-doped microcrystalline diamond film (~1 μm thick) is grown on the wafer surface and into the molds using hot-filament chemical vapor deposition (HFCVD) (Fig. 1b). The details of this diamond deposition have been outlined in earlier work [11]. Next, an aluminum (Al) hard mask layer is sputtered onto the diamond film and patterned via a second lithography step (diamond patterning), followed by O_2 plasma etching to selectively remove diamond between the pyramidal mold areas (Fig. 1c). After the removal of the Al mask, a thin stack layer comprised of titanium-tungsten (TiW), copper (Cu), and titanium (Ti) is deposited. TiW acts as an adhesion layer, Cu serves as a seed layer for electroplating and Ti protects the Cu from oxidation. This is followed by a third lithography step (membrane patterning), which patterns the tip array and the surrounding supporting membrane area (Fig. 1d). With the protective Ti layer etched away, a several-micrometers-thick Ni layer is electroplated onto the Cu, forming the supporting membrane for the tip array (Fig. 1e). The diamond tip array and Ni membrane are then released by locally underetching the Si substrate in KOH (Fig. 1f). After this, the tip array film is peeled off and fixed onto a Si support substrate, thus creating the diamond tip array probe chip (Fig. 1g). The peel-off approach is described in detail elsewhere [19]. The final step (Fig. 1h) of the fabrication workflow is to further increase the performance of the obtained, already functional FDT probe chip by converting it into an HFDT one through a self-patterned dry etching step as reported in reference [13].

However, having an array of sharp tips on a probe chip is only one aspect of the fabrication process. The spatial arrangement of those tips is equally important to fully exploit the advantages of the RTS configuration. In the following, we outline the design modifications together with the underlying motivations, which ultimately lead to the optimized tip array layout used in the final HFDT probe chip.

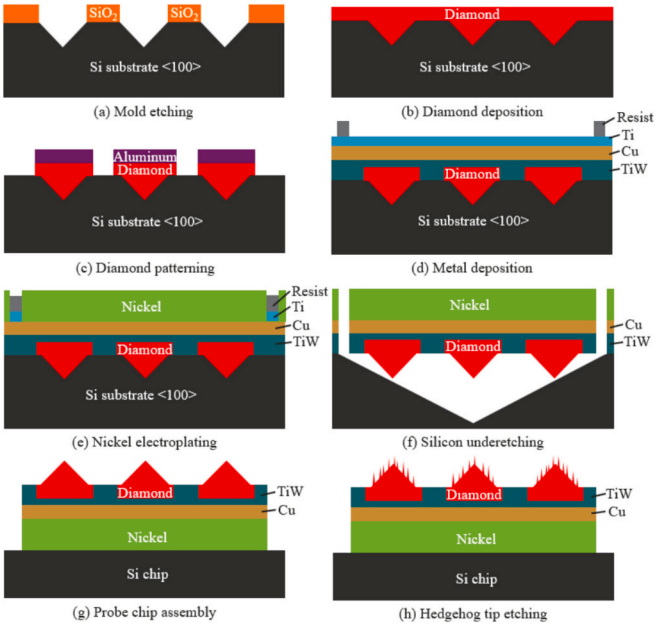

Fig. 1. Schematic overview of the different steps in the HFDT probe chip fabrication process.

2.2. HFDT probe chip design

In the RTS SPM setup, samples are mounted on commercially available tipless cantilevers approximately 50 µm in width, which imposes a minimum inter-tip spacing of 25 µm to avoid making lateral contact between the cantilever sides and adjacent tips. At the same time, the spacing should not be excessively large, to maximize the number of usable tips within the AFM piezo scan range, typically between 50 × 50 µm^2 and 100 × 100 µm^2. Additionally, the tips must exceed a height of 8 µm to prevent the front edge of the cantilever from colliding with the probe chip surface during scanning operation [15]. Taking these constraints into account, and while maintaining the overall fabrication process as described above, the optimized lithography mask design was developed during multiple iterations. Fig. 2 presents the evolution of these mask layouts alongside SEM images of the resulting probe chip prototypes, highlighting the differences between design generations.

The first cantilever design (Fig. 2a) was based on the well-established fabrication scheme of the standard FDT probes [11], with modifications to include multiple cantilevers of equal length, each carrying several tips. By scanning the sample cantilever and the tip cantilever perpendicular to each other, the issue of the cantilever's front edge hitting a neighboring tip is mitigated. Despite the relatively low tip density and the added mechanical complexity due to the combined spring constant contributions of both the sample and tip array cantilevers, this design was sufficient to serve as a probe chip for the initial proof-of-concept RTS SPM measurements.

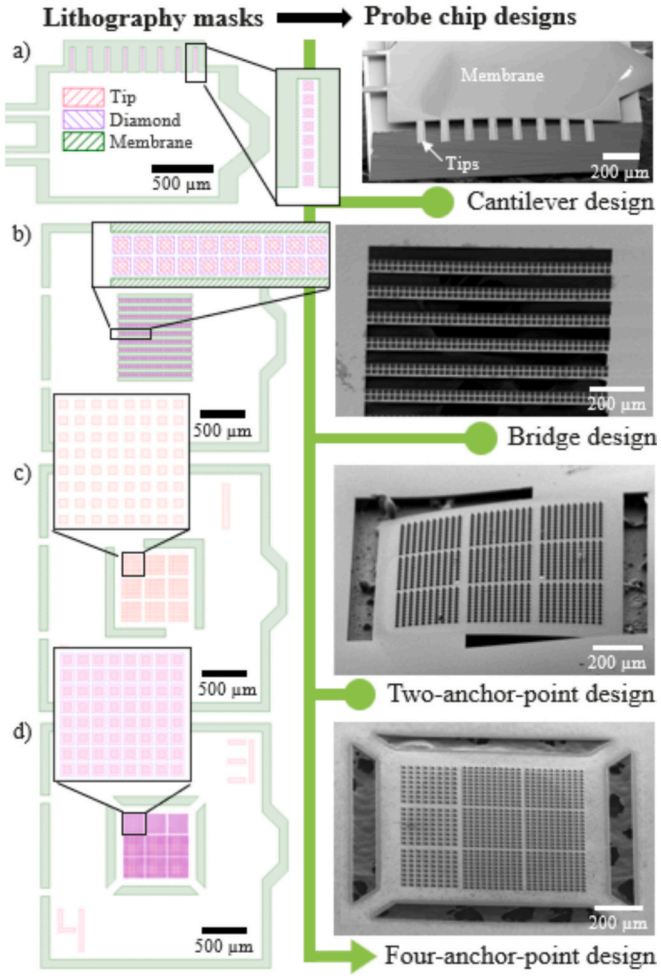

Fig. 2. Overview of the probe chip prototype design evolution, showing an overlay of the three lithography mask layouts used in the fabrication process, and SEM images of the resulting prototypes (right). The evolution includes: an initial cantilever design (a), a bridge design (b), a two-anchor-point design (c), and the final four-anchor-point design (d). Mask 1 (red) and mask 3 (green) are darkfield masks, where the colored regions represent transparent areas for tip and support membrane patterning. Mask 2 (purple) is a brightfield mask, with colored regions representing opaque areas for diamond patterning. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Following the proof-of-concept validation, the fabrication strategy shifted towards increasing the number of tips in the scan area. In the bridge design (Fig. 2b), lithography masks were designed to define double rows of diamond tips on narrow, elongated Ni beams, anchored at both ends to a larger supporting Ni membrane. Rectangular-shaped openings in this membrane, defined during the membrane patterning step (green mask), exposed the silicon substrate during the final KOH etching step, creating trenches to facilitate the peeling of the tip array beams from the wafer. It is worth noting, however, that occasional imperfections in metal etching and peel-off processes have in some cases led to significant losses in tip yield.

Therefore, to improve the tip array release, the design was modified to exploit the underetching behavior at convex corners during anisotropic KOH etching of Si ⟨100⟩ substrates [20]. This was achieved by introducing convex-corner-shaped edges in the Ni membrane at the upper-left and lower-right corners of the tip array, while maintaining anchor points to the support membrane at the upper-right and lower-left corners, resulting in the two-anchor-point design (Fig. 2c). By substantially increasing the KOH etching time, full underetching of the tip array was achieved, enabling an easy Ni membrane release from the substrate. This design also allowed for an increased tip density, as no additional clearance within the array was needed for peel-off. To simplify the process, the diamond patterning step was omitted in this prototype, resulting in the full diamond coverage across the entire chip area. However, the resulting tip array membrane, with only two anchored corners, exhibited significant bending due to interfacial stress in the Ni/Cu/TiW/diamond stack, rendering a large portion of the tips unsuitable for RTS SPM measurements.

Therefore, in the final design, the diamond patterning was included again, and a four-anchor-point configuration was implemented to retain membrane flatness (Fig. 2d). Trapezium-shaped openings were introduced on all four sides of the tip array, arranged such that the rectangular cavities created during KOH etching merged. This exposed the four convex corners of the membrane to etch attack, ensuring complete underetching of the tip array, while preserving anchor points at all four corners. This revised configuration effectively counteracts stress-induced bending, resulting in a flat, high-yield, and dense tip array ideally suited for application in RTS SPM measurements.

3. Results and discussion

Here, we present the results of the fabrication process described above, focusing on a comprehensive evaluation of the HFDT probe chips. This includes analysis of tip apex morphology, fabrication yield, and performance within the intended application scope of SSRM. Furthermore, we benchmark the newly developed diamond-tip probe chip technology against the existing CDT probe chip.

3.1. Tip morphology and fabrication yield

We begin with a visual inspection of the fabricated probe chips using SEM. As shown in Fig. 3a, a representative probe chip consists of a total of 792 tips, arranged into a 3 × 3 grid, comprising six blocks with 10 × 10 tip arrays and three blocks with 8 × 8 tip arrays. The 8 × 8 array, highlighted as an example in the SEM close-up in Fig. 3b, showcases a uniform tip-to-tip spacing of 30 µm, while the 10 × 10 arrays feature a slightly smaller tip spacing of 25 µm. Therefore, in both tip arrangements, the tip separation is kept at no less than 25 µm, ensuring rapid and reliable tip switching, while simultaneously preventing unwanted

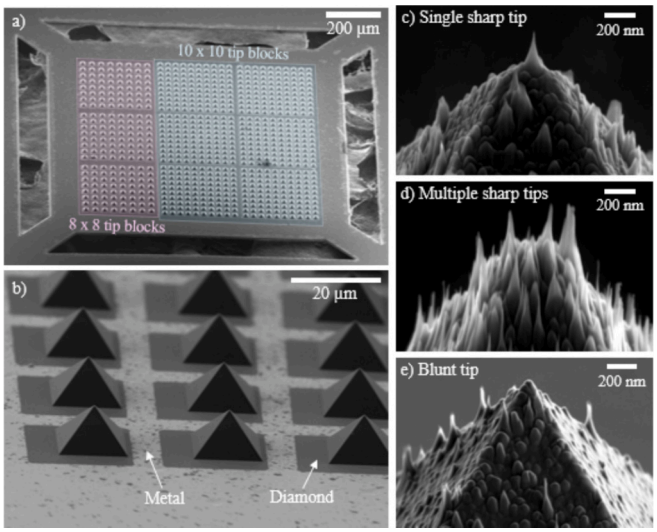

Fig. 3. SEM image of an array of diamond tips in a probe chip (a), a zoomed image of a selection of the pyramidal diamond tips (b) and high-resolution SEM images of the apex of a diamond pyramid with single sharp tip (c), multiple sharp tips (d) and blunt tip (e) configurations.

contact between the sample-cantilever edge and adjacent tips.

High-resolution SEM images shown in Figs. 3c–e highlight the diversity of apex geometries resulting from the final dry etching process: a single sharp tip (Fig. 3c), multiple sharp tips (Fig. 3d), and a blunt tip apex (Fig. 3e). This variability is due to a unique self-patterning feature of the dry etching step, wherein re-sputtered metal particles from the surrounding nickel membrane act as localized nanoscale etch masks, selectively determining the final apex configuration, as previously discussed in detail [13].

For the preferred single sharp tips, tip radii as small as 2.7 nm have been measured, although the yield for this tip morphology is only approximately 5 %. It should be emphasized, however, that this yield represents a conservative lower-bound estimate. SEM imaging of multi-tip HFDTs can sometimes be misleading due to imaging angles and perspective effects, which may wrongly suggest multiple simultaneous contact points. In practice, one apex often protrudes sufficiently to serve as the sole point of interaction with the sample surface. Indeed, SPM measurements using tips that appear to have multiple apexes in SEM often produce artifact-free, high-resolution images. Conversely, even blunt HFDT tips typically perform well in practice due to the polycrystalline diamond grain structure, where individual diamond grains can effectively act as discrete, sharp interaction points with the sample surface. The blunter tips may additionally be suitable for applications where tip stability over many scans is prioritized over resolution, such as in nano-milling or comparative studies across multiple samples. Altogether, the preliminary SEM analysis clearly confirms the exceptional sharpness and high aspect ratio of the nanoscopic tips, whether present in the apparent single-tip or multi-tip configurations on the FDT apex. However, to truly assess the quality of the newly developed HFDT probe chip, it is essential to test its performance within its target application, RTS SSRM, with respect to the above-discussed requirements for probe chip design as well as conductivity, wear resistance, and geometry of the tips that comprise it.

3.2. HFDT probe chip performance in RTS SSRM

All RTS SSRM measurements discussed in this section were conducted using a Bruker Dimension Icon-PT AFM system equipped with an SSRM application module, under ambient conditions. To primarily assess the electrical performance of the developed HFDT probe chip, RTS SSRM measurements were carried out on a p-type silicon staircase calibration sample composed of multiple layers with varying doping levels. These layers span a wide range of carrier concentrations, from 4 $\times$ 10^{16} to 5 $\times$ 10^{19} carriers/cm^3, providing a rigorous test for the SSRM dynamic range that could be achieved with the HFDT probe chip tips. This is especially critical in the highly doped regions, where measurements are most susceptible to parasitic tip resistance. As shown in the two-dimensional SSRM resistance map in Fig. 4a, clear electrical contrast is observed between the discrete layers across this full doping range. This contrast serves as strong evidence that the tips on the HFDT probe chip provide a satisfactory level of electrical conductivity. Furthermore, achieving good SSRM contrast requires applying sufficiently high forces at the tip-sample interface, generating pressures of around 10 GPa which are necessary to induce the phase transition of silicon beneath the tip apex into the metallic β-Sn phase [21,22]. These extreme conditions place significant demands on the mechanical robustness of the tips. However, as evidenced in the resistance map, no measurement instabilities or electrical contact failures were observed throughout the imaging process. This consistent performance suggests that the tip apex did not experience significant degradation, confirming its mechanical stability. This is also confirmed for another example, presented in Fig. 4b. Here, the focus shifted specifically to assessing the sharpness of the nanoscopic tips on the HFDT probe chip, by conducting measurements on a more complex, feature-rich GaAs nano-ridge waveguide structure [23]. This structure is composed of multiple sharp nano-heterointerfaces, all clearly resolved in the high-resolution SSRM resistance map, demonstrating an excellent tip sharpness.

However, the most effective way to assess the performance of this newly developed technology is through direct benchmarking against existing alternatives, specifically, RTS CDT probe chips. To this end, a finFET structure with a gate length of 28 nm was investigated using both CDT and HFDT probe chips. It is important to note that RTS SSRM results were obtained using randomly selected tips from each probe chip type, and that the results presented in the following accurately reflect the typical imaging quality achievable with both technologies. Fig. 5 presents the results of this comparative study, showing SEM images of representative tip apexes from each RTS probe chip, alongside corresponding 2D SSRM resistance maps of the finFET device. The comparison of the SSRM maps acquired with CDT (Fig. 5c) and HFDT (Fig. 5d) probe chips reveals a few notable differences. Measurements done with the CDT probe chip produce a visibly broadened representation of the source, drain, and gate metal contacts, deviating from their actual physical dimensions. In contrast, the HFDT probe chip delivers a much sharper, more accurate representation, with metal contacts clearly resolved and closely aligned with their real-world dimensions (e.g., a measured gate width of 27 nm). Moreover, the S/D *epi* doping is also resolved with nanometer-scale precision, offering valuable insights into

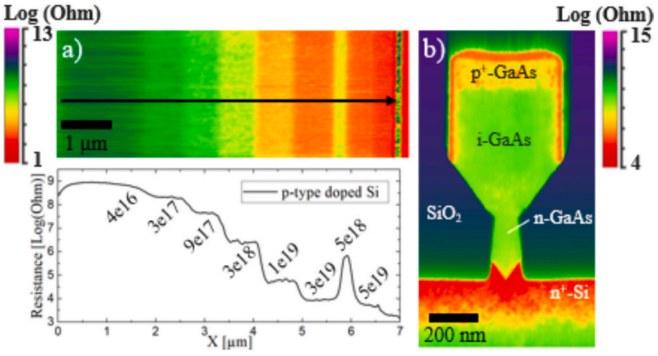

Fig. 4. a) 2D SSRM resistance map of a p-type doped Si staircase sample containing multiple layers with varying carrier concentrations; the measured resistance profile with the carrier concentration values for the different layers is shown underneath. b) 2D SSRM resistance map of the cross-section of a GaAs nano-ridge waveguide structure.

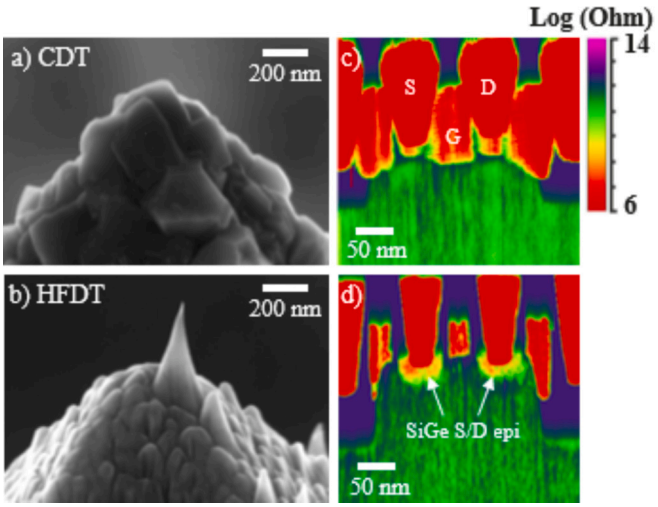

Fig. 5. SEM images of a CDT (a) and an HFDT (b) tip apex. SSRM resistance maps of a FinFET structure with a CDT (c) and an HFDT (d), measured in RTS configuration.

dopant diffusion, a crucial factor for accurate finFET device modelling and development [24,25].

The striking difference in performance between the two probe chip types is primarily due to the broader tip apex geometry of the CDT tips, which increases the tip-sample contact area and introduces feature-broadening in the resulting images. Additionally, the low aspect ratio of the CDT tips can cause adjacent diamond grains to simultaneously contact the sample surface, leading to multiple-tip artifacts. In contrast, the HFDT probes, with their high-aspect-ratio nanoscopic tips atop the FDT apex, effectively avoid these issues. This further reinforces our earlier observation that, even when SEM imaging suggests the presence of multiple apexes, a single dominant protruding tip typically governs the tip–sample interaction, ensuring artifact-free measurements. Overall, this comparison highlights the superior performance of HFDT probe chips, making their application in RTS SSRM a significant advancement for cutting-edge semiconductor device metrology.

4. Conclusions

In this work, we have demonstrated the successful development of a novel HFDT probe chip architecture tailored for RTS SPM applications. By adapting the established HFDT fabrication process, originally designed for conventional single-tip configurations, to dense tip arrays integrated into probe chips, we addressed key challenges related to tip sharpness and high-throughput measurement compatibility. SEM inspections confirmed the high morphological quality of the fabricated diamond tips, while RTS SSRM measurements validated their functionality. The HFDT probe chip tips exhibited good electrical conductivity, robustness under high tip load force, and excellent spatial resolution. Moreover, comparative studies against the pioneering RTS CDT probe chips on advanced semiconductor structures clearly highlighted the improved imaging capabilities provided by the HFDT probe chip technology. By bridging the gap between high-resolution electrical imaging and high-throughput operation, the newly developed HFDT probe chip platform provides a promising step forward for future nanoscale electrical characterization.

Declaration of generative AI and AI-assisted technologies in the writing process

During the preparation of this work the author(s) used ChatGPT in order to improve language and readability. After using this tool/service, the author(s) reviewed and edited the content as needed and take(s) full responsibility for the content of the publication.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Jinwan Cho and Sugil Gim report financial support was provided by Korea Institute for Advancement of Technology (KIAT). Thomas Hantschel has patent #EP 3702792 B1 issued to Imec. Thomas Hantschel and Antti Kanniainen have patent #US 11112427 B2 issued to Imec. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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