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Method to Study Potential-Induced Degradation of Perovskite Solar Cells and Modules in an Inert Environment

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The efficiency of perovskite solar cells (PSCs) is advancing rapidly, yet their sensitivity to ambient conditions poses challenges. An additional degradation mechanism, potential-induced degradation (PID), can emerge during field operation, but the understanding of PID within perovskite devices is limited. To exclude environmental stressors, this study is conducted in an inert environment at room temperature. PSCs and mini-modules are subjected to a 324 h PID stress test at −1000 V, revealing relative efficiency losses of around 29% and 24% for the PSCs and mini-modules, respectively, exposing subtle degradation differences. These degradation rates are notably lower than reported in the literature, suggesting possible additional degradation pathways arising from suboptimal encapsulation combined with ambient conditions. Subsequently, half of the stressed samples are subject to +1000 V for 523 h and recover to a reduced efficiency loss of 15% and 7.7% for the PSCs and module, respectively. In contrast, storing the stressed samples on the shelf increased the efficiency losses to 32% (PSCs) and 41% (module). Therefore, the post-PID rates differ significantly between both groups, whereas both effects of voltage recovery and progressed degradation are more pronounced in modules compared to cells. This study contributes to a robust method for PID research.

1. Introduction

Organic–inorganic halide perovskite solar cells (PSCs) were developed in 2012 after they were first used as sensitizers in dye-sensitized solar cells in 2009.[1] The efficiencies have been rapidly increasing from 9.7% in 2012 to 26.1% in 2023.[2,3] In the pursuit of commercialization, one of the critical objectives is the achievement of long-term stability and upscaling of the devices.[4–7] PSCs, similar to other photovoltaic (PV) technologies, encounter several stability challenges arising from various environmental stressors.[8,9] Furthermore, additional degradation mechanisms, such as potential-induced degradation (PID), can arise during field operation. PID is already intensively investigated within commercial silicon PV applications, and it stands out as a significant reliability concern.[10,11] However, understanding of PID in perovskite devices is limited.

PID is a system-level degradation mechanism due to a high electric potential difference between the solar cells and the grounded module's frame. The mechanism mainly occurs when the PV cells have a negative potential to the ground. Subsequently, positively charged sodium ions (Na^+) can migrate from the soda lime glass toward the PV cell and deteriorate its performance, ultimately leading to severe performance losses and, in some cases, catastrophic failure within a relatively short time frame.[10,12] Extensive research has already been conducted into this degradation mechanism within conventional silicon solar panels, and various mitigation strategies and recovery procedures have been suggested.[10,13–17] With the upscaling of PSCs and working toward the commercialization of the product, the investigation of this system-level degradation mechanism within perovskite

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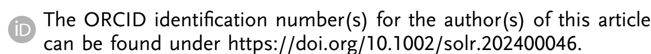
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devices gains increased significance. However, research studies on this phenomenon and its effects are relatively scarce for these next-generation solar cells. Only a few publications are available, and they show that PID can be very aggressive.[12,18–22] Nakka et al. suggested that an additional nickel oxide (NiO_x) layer between the hole transport layer (HTL) and indium tin oxide (ITO) layer suppresses the migration of sodium ions, hence mitigating PID to a certain degree.[22] Furthermore, some researchers have briefly investigated the possibility of recovering the PID-degraded devices and state that this is partially possible by inverting the bias voltage. Despite these improvements, some permanent degradation remains.[12,18,20,21]

The PID-stress tests from these publications have been conducted on encapsulated perovskite cells using epoxy resins in ambient conditions (i.e., 25 °C, and 20% relative humidity (RH)), or at elevated temperatures (i.e., 60 °C, and 20% RH). This applies to all referenced PID stress publications, except for Xu et al. who utilized glass–glass encapsulation employing a polymer film as the encapsulant and butyl rubber as the edge sealant.[20]

PSCs are known to be very sensitive to ambient exposure, such as moisture, oxygen, and temperature. Therefore, the encapsulation approach is used to minimize the ingress of moisture and oxygen. Moisture and oxygen can rapidly generate strong hydrogen bonds with the organic cations of perovskite like methylammonium (MA), weakening the original bonds between MA and Pb–I. Consequently, the formation of this hydrated intermediate decreases absorption significantly within the visible spectrum. Furthermore, decomposition occurs by deprotonating the organic cation, where the volatile hydrohalogenic acid (HI) could be formed.[5,23–25] MA-based perovskites have been found to be stable when they are exposed to oxygen in the dark.[24,26] However, combining oxygen and illumination could result in rapid degradation.[5,26,27] The oxygen can be absorbed and diffused through iodide vacancies. This process has been observed to occur within an hour after exposure. Afterward, a charged and highly reactive superoxide is formed due to trapping of electrons in the conduction band by the oxygen. Hence, an acid–base reaction with the A site cation is initiated, resulting in the creation of water, deprotonated A site gas, and lead iodide.[24,26–28] The oxygen and moisture species originating from the environment can be absorbed. However, even with encapsulated devices, oxygen could be released through the metal oxide layers that, in combination with illumination, can cause degradation.[5,28] Furthermore, perovskite PV is very sensitive to thermal stress whereby the perovskite absorber material, depending on its composition, easily decomposes.[5,26,27] Besides the perovskite film, the elevated temperature could also affect functional layers like the electron transport layers (ETL) or HTL by diffusion of some of their constituents.[5,23] Additionally, metal contacts can easily react with the decomposition products, resulting in instability.[24]

Encapsulating the perovskite devices with a cover glass is possible in two different ways: glass–glass laminated encapsulation using thermoplastic polymers,[20] and encapsulation using epoxy resins.[12,18,19,21–23,25,27] When encapsulation is performed using thermoplastic polymers, the approach requires high lamination temperatures (i.e., usually higher than 140 °C[23,29,30]), which is a significant drawback because these elevated temperatures can degrade the structure of the devices. Furthermore, within UV-curable encapsulation, the epoxy resin serves as an edge sealant, and the cover glass is affixed to the device. The curing process is accomplished with UV light at room temperature, presenting notable advantages over the polymer film encapsulation procedure.[23,25,31]

Unfortunately, this encapsulating approach using UV-curable epoxy resin possesses challenges and needs to be a foolproof method ensuring the sustained efficiency of the cells over time. Many commercially available epoxy resins are widely used for PSC encapsulation. Nevertheless, there are currently no UV-curable epoxy resins designed explicitly for perovskites. UV-curable epoxy resins are typically composed of monomers, initiators, stabilizers, and trace amounts of oxygen and moisture. It is important that these constituent materials do not react with the perovskite layer in the solar cell. In literature, it has been reported that a droplet of commercially available epoxy resin, applied on a metal electrode, can dissolve the active layer and, therefore, deactivate the perovskite.[23] Furthermore, hydroxyl-containing epoxy resins can form hydrogen bonds with water quickly and thus trap moisture, potentially leading to degradation of the perovskite. Nevertheless, when encapsulation is used, it has been shown to prevent the escape of volatile products during degradation at elevated temperatures, creating an equilibrium in the reversible chemical reaction.[24]

Due to the susceptibility of PSCs to environmental factors and the possibly introduced sensitivity when the devices are encapsulated, it can become challenging to investigate the influences of an external electric field, leading to PID. Unwanted exposure to ambient conditions using encapsulation may have some additive influence on the PID study, which may bias the results. Therefore, in this publication, a study is carried out that investigates the influences of PID, whereby the undesirable additional degradation factors (i.e., ambient conditions and encapsulation) are kept to a minimum by conducting all experiments in an inert environment at room temperature. Using this approach, this study tries to gain accurate insights into the degradation mechanism, possibly accelerating the search for PID mitigation strategies and recovery processes. To maximize the isolation of the PID effects on the perovskite devices, a customized PID-stress setup was created and placed in a nitrogen environment. The temperature influences could be minimized by conducting the experiments at room temperature.

To date, most reported PID stress tests in literature have focused on perovskite cell structures.[12,18–22] However, in practical applications, the PID mechanism is expected to impact module-design samples instead of single-cell-design samples. Therefore, examining potential differences in the degradation mechanism between these two sample designs is relevant for developing precise mitigation and recovery strategies. A perovskite solar module (PSM) comprises the same layers as a perovskite cell. However, it distinguishes itself by incorporating multiple perovskite cells interconnected in series through P1P2P3 laser scribes. Nevertheless, the P2 scribe brings the perovskite material into direct contact with the top metal contact, creating a new interface and possible degradation path. Additionally, the P3 scribe creates an opening for environmental exposure to the absorber if no measures are taken.[27] Furthermore, when solution processing techniques are being used, achieving uniform layers becomes challenging.[32]

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Consequently, in literature, it has been reported that PSMs exhibit distinct degradation compared to PSCs, posing difficulties in achieving comparable efficiencies within PSMs as observed in PSCs.[27,31,33,34]

Hence, this study incorporates an initial comparison to assess the susceptibility of PSCs versus PSMs. Given the relatively mild stress conditions and the absence of established testing standards for PID stress tests in perovskites, an extended duration of 324 h is used (i.e., around 14 days). Subsequently, the negative bias voltage was inverted to investigate voltage recovery for ≈523 h. As the devices were placed in a nitrogen environment, it is important to note that all samples were left unencapsulated.

2. Experimental Section

In this study, two distinct groups of samples are used: the first group consists of cell-design samples, while the second group comprises a mini-module design. All samples are fabricated using an identical p-*i*-n structure incorporating a triple-cation ($Cs_{0.05}FA_{0.85}MA_{0.10}PbI_{2.90}Br_{0.10}$) perovskite absorber layer of 550 nm. The front electrode comprises 150 nm indium tin oxide (ITO), a transparent conductive oxide. Furthermore, 15 nm of nickel oxide (NiO_x) is used as HTL, followed by a thin, subnanometer, self-assembling monolayer. A layer of 0.8 nm lithium fluoride is applied on top of the perovskite to achieve field-effect passivation, enhancing its overall performance.[35–37] Subsequently, a 60 nm C60 and 5 nm bathocuproine bilayer ETL is employed. Each sample is equipped with a copper rear electrode and intentionally left unencapsulated. Further details of the materials and the processing can be found in the supporting information.

The cell-design samples comprise 12 cells per substrate, each having an active area of 0.125 cm^2. In contrast, the module-design samples consist of four individual subcells with an active area of around 1 cm^2, connected in series through P1P2P3 laser scribing, with a total aperture area of 4 cm^2. Each group consists of two PID stressed samples and two reference samples (i.e., 24 stressed cells and 24 reference cells combined with two stressed modules and two reference modules). The reference samples were stored in the dark in the controlled nitrogen atmosphere and were not subjected to voltage stress. To minimize the environmental stressors, all devices were subject to inert conditions (i.e., <0.1 ppm O_2, <0.5 ppm H_2O) and room temperature (i.e., 25 °C).

To conduct a PID stress test, the application of an external electric field is required. In the absence of International Electrotechnical Commission (IEC) standards for defining test procedures and evaluating PID in perovskite devices, the experiments of this study are conducted based on the standard foil method described in IEC 62804-1, developed for silicon PV.[38] The PV cells and modules were short-circuited to avoid an external electric field across the device stack. 0 V was continuously applied to the exterior of the glass via a copper block. Furthermore, the short-circuited samples were connected to −1000 V during the PID stress test and to +1000 V during the recovery test. **Figure 1** illustrates a schematical representation of the electrical connections. The entire stress setup was connected and positioned in an inert environment. For this purpose, a dedicated sample holder was fabricated, illustrated in **Figure 2**. Here, a custom-made printed circuit board was developed to short-circuit the sample and apply a bias voltage. A 3D-printed cover securely holds all components, pressing a copper block onto the sample that can be connected to 0 V.

To capture significant degradation and approach stabilization as closely as possible, the negative bias voltage stress was applied for a duration of 324 h. Subsequently, one sample of each group was subjected to a positive bias voltage stress test for ≈523 h (i.e., the short-circuited sample was exposed to a high positive potential relative to the grounded glass), while the other samples were stored together with the reference samples.

To acquire insights into the degradation mechanism, intermediate light-JV measurements were taken on a regular basis in a nitrogen-filled glovebox using a Keithley 2602A source-measure unit and an Abet solar simulator. The measurements were carried out on all devices under one sun illumination, with

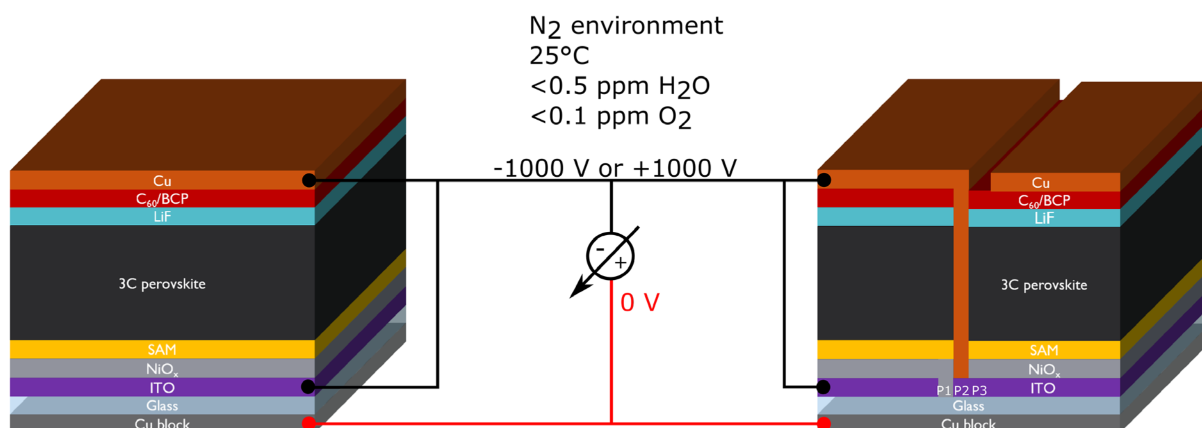

Figure 1. Schematical representation of the short-circuited perovskite PV stack. The left side illustrates the architecture of a cell, whereas the right side represents a graphical representation of a module with the P1P2P3 scribes. The copper block is always connected to 0 V in contrast to the short-circuited connections that are connected to −1000 or +1000 V.

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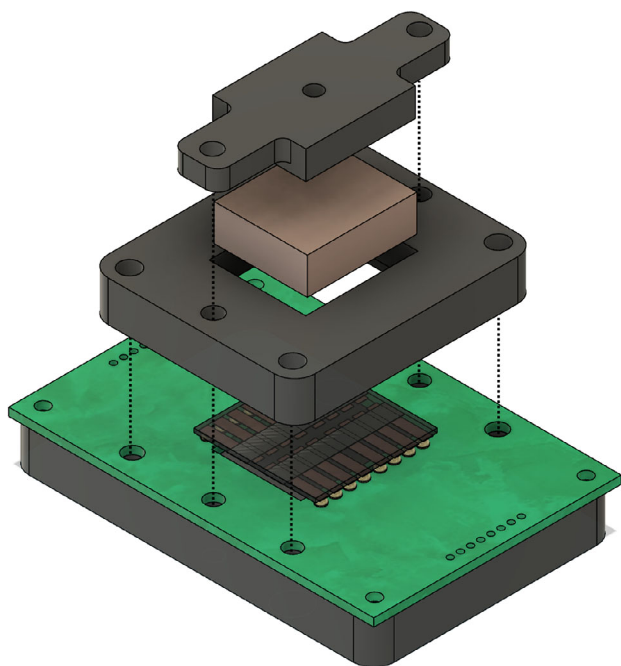

Figure 2. 3D representation of the custom-made sample holder for external voltage stress application of perovskite cell and module-design samples.

simulated 1000 W m^{-2} AM 1.5G illumination from a 450 W xenon lamp (Abet Sun 2000). A fan was used to control the temperature of the measured devices at 30 °C. The illumination intensity was calibrated with a Fraunhofer ISE's WPVS reference solar cell (Type: RS-ID-4). The JV sweeps were carried out between −0.2 and 1.3 V with a voltage step of 0.01 V and a delay time of 0.01 s (0.8 V s^{-1}). Additionally, external quantum efficiency (EQE) measurements were conducted at the beginning, at intermediate stages, and upon completion of the experiment, on the cell-design samples only. For this, wavelengths between 300 and 900 nm were used, with a stepsize of 5 nm.

Furthermore, EQE measurements were taken. These were performed with a Bentham PVE300 spectral response setup using halogen and Xenon lamps. A Si reference cell was used to calibrate the tool. Subsequently, EQE spectra were recorded between 300 and 900 nm wavelengths with a step of 5 nm, and an area of 0.7 mm^2.

3. Results and Discussion

During the pilot testing phase, PID stress tests were performed on encapsulated devices to develop and evaluate the custom-built PID stress setup. Glass–glass encapsulations were applied to module and cell-design samples, employing a polymer film with butyl rubber as the edge sealant and glass–glass encapsulation using UV-curable epoxy resin, respectively. The PID stress test was conducted under ambient conditions at room temperature, revealing that the encapsulation did not completely prevent the ingress of ambient chemicals. As these pilot PID stress tests advanced, the perovskite material became transparent or exhibited significant yellowing. These two effects might be attributed to the formation of hydrogen bonds due to moisture exposure and the decomposition resulting in the formation of Pb–I ascribed to the combined influence of oxygen and light, respectively (see Figure S1 and S2, Supporting Information). Similar effects during PID stress tests were reported by Purohit et al.[19] Given the difficulty in achieving proper encapsulation, subsequent PID stress tests were carried out in an inert environment to prevent the need for packaging.

Figure 3 illustrates the loss in power conversion efficiency (PCE) as a function of stress duration for both the cell-design and module-design samples (i.e., Figure 3a,b, respectively). The vertical black line after 324 h indicates that the negative bias voltage stress was stopped and the bias voltage was inverted (i.e., 0 V at the glass, and +1000 V at the short-circuited devices). Here, one stressed cell sample and one stressed module sample were excluded from voltage stress and stored on the shelf with the reference samples. Additionally, it is to be mentioned that outliers in the cell-design samples were removed at each point.

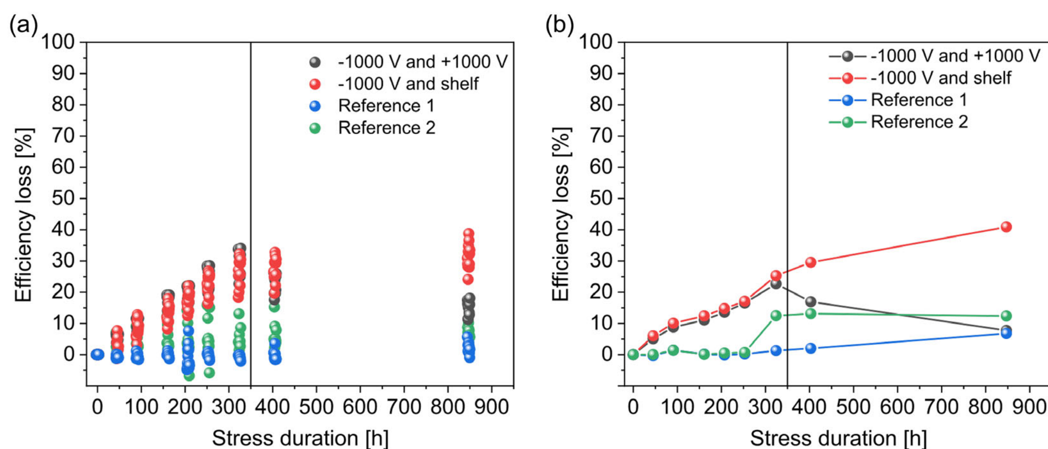

Figure 3. a) Relative efficiency loss as a function of stress duration for cell-design samples and b) module-design samples.

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The PCE loss graph of the cell-design samples in Figure 3a illustrates that the control group maintained a stable efficiency, with an average efficiency difference of −0.78% and 5.1%. However, the stressed samples exhibited a notable decline in PCE after 324 h, with an average relative loss of 30% and 28%. The decline in efficiency can be attributed to the migration of sodium ions from the front cover glass under the influence of the external electric field, as established in previous studies.[12,21] Additionally, Nakka et al. stated that the sodium ions interact with the negatively charged halides in the perovskite, forming a weak sodium-halide bond.[21] Upon further analysis of the data, it became evident that both stressed samples exhibited the same degradation trend. This clearly illustrates the high degree of reproducibility in the applied degradation.

It is to be noted that the rate of degradation is significantly lower compared to those reported in existing literature.[12,18,19,21,22] Nakka et al.[22] reported a relative efficiency loss of 32% after 96 h of PID stress and 49% after 135 h, using the same stress conditions (i.e., room temperature, 1000 V potential difference) and a similar three-cation perovskite stack with a nickel oxide HTL. However, it is important to highlight that this comparison involves PSCs with different active areas. Nakka et al. used samples comprising an active area of 1.2 cm^2, whereas the 24 cells in this study had an active area of 0.125 cm^2. An optical examination revealed no differences (e.g., yellowing or transparency of the perovskite, as also observed in ref. [19]) in the samples, indicating that the pilot tests were heavily affected by suboptimal encapsulation, complicating the analysis of the PID mechanism. Therefore, it is hypothesized that the ambient conditions, coupled with encapsulation, could introduce additional degradation pathways, which potentially become worse by the external electric field.

Figure 3b provides the experimental data on mini-modules. The control samples present stability over time, showing no signs of degradation on the shelf. Nevertheless, a slight loss in PCE was noticeable after 324 h for sample "Reference 2". This loss is hypothesized to be attributed to defects in the perovskite module. After the jump in PCE loss, this characteristic remains constant for the rest of the experiment. On the contrary, the stressed samples show immediate degradation, which continues until the end of the stress test at 324 h. It can be seen that both stressed modules exhibit the same trend in degradation. At the end of the 324 h of negative bias voltage stress, both stressed modules suffered a significant loss in PCE of 23% and 25%.

After concluding the PID stress test at 324 h, a recovery test was started by applying a positive bias of +1000 V to the stressed samples. In each group, one stressed sample was removed from the setup and stored with the reference samples. Figure 3a,b clearly illustrates that the PCEs of the samples that were subject to a positive bias voltage (i.e., the black curve in both Figure 3a,b) significantly improve. On the contrary, the stored degraded samples did not demonstrate any recovery. Moreover, the PCE even deteriorated. For the cell-design samples, the PCE losses went from an average of 30% and 28% at 324 h toward 15% and 32%, respectively. In contrast, the PCE loss of the module-design samples went from 23% and 25% after 324 h of PID stress toward 7.7% and 41%, respectively. It is hypothesized that the application of a positive bias voltage will drive the sodium ions out of the perovskite sample, and back toward the glass substrate.[12,21] However, some degradation remains visible.

It has been shown in the literature that ion migration can cause damage to the perovskite lattice, therefore creating additional defects in the perovskite film, which could deteriorate its performance.[39–42] Hence, it is assumed that the sodium ion migration inside the perovskite film, due to the negative bias voltage stress, can cause similar, permanent damage. Moreover, the presence of sodium halide bonds might persist. Nevertheless, microstructural analysis would be necessary to confirm this.

Overall, these results, which were obtained using a stress setup placed in a controlled nitrogen environment and performed at room temperature, show that the PID stress can be applied very accurately. Furthermore, it is apparent that reversing the bias voltage decreases the losses in PCE significantly and recovers the perovskite device to a certain degree. No spontaneous recovery occurs when the degraded samples are stored in the dark. In contrast, the degradation even progresses. It was observed that the poststress characteristics of the module-design samples are significantly more pronounced compared to the cell-design samples (i.e., the progressive degradation when the sample was not subjected to a positive bias voltage, as well as the recovery in efficiency when a positive bias voltage was applied).

To retrieve more insights into the effects of the degradation, it is necessary to take a closer look into the behavior of the other characteristics of the perovskite devices. Therefore, the effects over time on JV curves and EQE measurements are discussed in the following sections.

3.1. *I–V* Measurements

Figure 4 illustrates the JV graphs of the four samples that experienced 324 h of negative bias voltage stress. In Figure 4, parts (a) and (c) depict data from samples of the cell and module-design that underwent the additional positive bias voltage for 523 h subsequent to the PID stress (i.e., between 324 and 847 h of the total experiment). Furthermore, parts (b) and (d) display the performance of the cell and module-design samples subjected solely to the 324 h of PID stress, respectively. All JV graphs contain the measurement at the start and end of the PID stress test (i.e., 0 and 324 h) and after 523 h of a positive bias voltage (i.e., 847 h). As previously mentioned, a cell sample consists of 12 individual perovskite cells. Therefore, the illustrated graphs represent only one of the 12 cells per sample.

During the 324 h of the PID stress, the decrease in PCE could be primarily attributed to a decrease in short-circuit current (J_{SC}) for all four samples. Additionally, a decrease in fill factor (FF) and open-circuit voltage (V_{OC}) was noticeable, albeit to a lesser extent compared to the reduction in J_{SC}.

Figure 4a,c indicates a significant increase in J_{SC} and V_{OC} after a positive bias voltage. However, a slight decrease in FF is still noticeable. It is apparent that the V_{OC} of both devices recovered approximately the same value, compared to the initial measurements (i.e., a normalized value of 98%). Nevertheless, the recovery of J_{SC} exhibits significant differences for cells and modules. It is hypothesized that these variations in recovery can be attributed to the lower rate of the PID mechanism in the module-design

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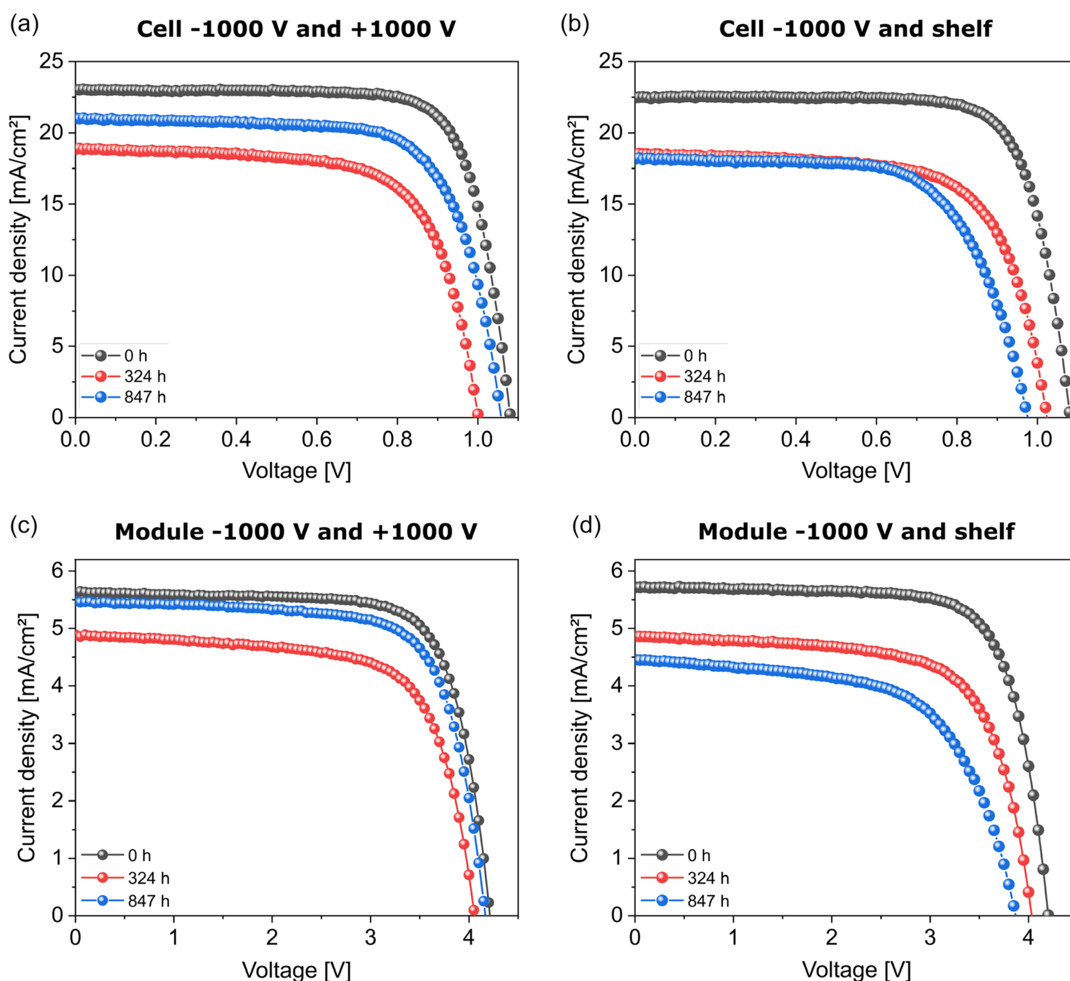

Figure 4. Light JV characteristics for a,c) a cell and mini-module, respectively, exhibiting negative and positive bias voltage, and b,d) a cell and mini-module, respectively, only subject to negative bias and afterward is stored.

samples compared to the cell-design samples. Consequently, the effects of sodium migration would be less pronounced, rendering recovery more feasible.

However, the same trends could not be observed in the stressed samples stored together with the reference samples. Here, two different effects seem to be present. In Figure 4b, a decrease in FF and V_{OC} is observed, while J_{SC} remains relatively constant. The series resistance and maximum power point seem to be affected. On the contrary, Figure 4d exhibits a more substantial decrease in J_{SC} compared to its cell's counterpart. However, similar to the impact observed on the cells, it is apparent that both FF and V_{OC} are now affected to a greater extent.

These experiments show that applying a positive bias voltage across the devices recovers the JV characteristics to a certain extent. However, some irreversible damage remains, mainly observable in the FF. The J_{SC} and FF at the module level seem to have degraded more significantly than those in the degraded cell. The presumed difference in degradation rate between both cell-design and module-design samples, coupled with the variance in JV characteristics observed in the samples not subjected to a positive bias voltage, suggests the possibility of a different PID mechanism between both types of samples.

3.2. EQE Measurements

Figure 5a,b illustrates the EQE graphs of stressed cell-design samples, with Figure 5a being the sample subjected to a positive bias voltage. The measurements were not taken from the module-design samples since the tools used in this experiment are not suited for this purpose. As depicted in the graphs, there is a noticeable uniform downward shift of the EQE curve after PID stress, consistent with the reports of other groups.[12,21,22] A decline in EQE output of around 10% was visible after 324 h, which agrees with the observed decrease in J_{SC}. When no positive bias voltage was applied after the PID stress, the EQE curve increased with ≈2% absolute value. This finding could be counter-intuitive since the JV results from the previous section indicate that the J_{SC} slightly decreased during the 523 h on the shelf. However, the EQE measurements in this experiment were performed without bias irradiance. According to

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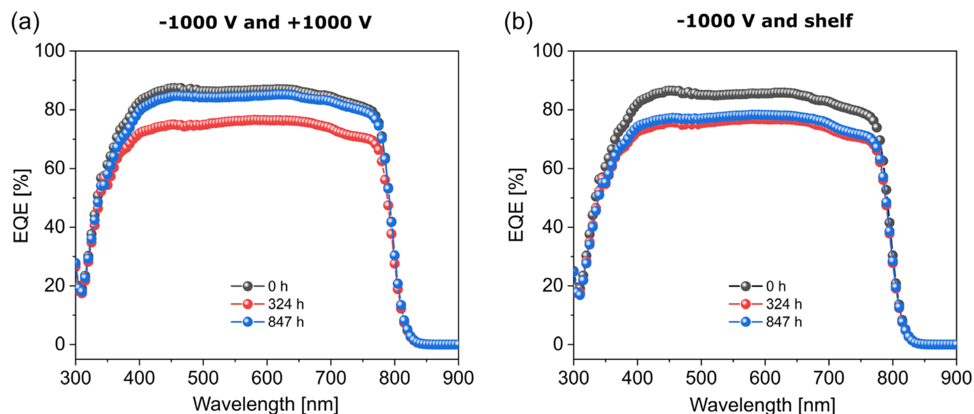

Figure 5. a) EQE graphs over time of a cell-design sample exhibiting negative and positive bias voltage stress and b) a cell-design sample only subject to negative bias voltage and stored on the shelf.

the literature, overestimation of the J_{SC} could occur due to processes that vary non-linearly with light intensity.[43,44] Moreover, there is a difference in area, with the EQE area being 0.7 mm^2, while the active area of the cell is 0.125 cm^2. Consequently, inhomogeneous damage across the cell could lead to a difference in the results.

3.3. Comparison Cells and Modules

From the previous sections, it became clear that both stressed cell and module-design samples have been experiencing PID and that a positive bias voltage has been able to recover the electrical characteristics of the PSC and module to a large extent. However, a difference in architecture exists between cells and modules, so the electrical operation deviates, potentially rendering additional degradation pathways. Hence, whether the same effects would develop due to high-voltage stress is yet to be determined. As a first perspective at whether there is a difference present in the degradation processes between the two designs or not, the PCE results from Figure 3 illustrate a brief discrepancy in the degradation velocity between both. However, the more detailed JV graphs suggested that equivalent degradation mechanisms and effects manifest when applying a negatively biased voltage.

The most significant differences between cells and modules can be found in the poststress characteristics when a positively biased voltage is applied or when the stressed samples are stored. To investigate whether all cells and modules behave similarly, the evolution of the JV characteristics is illustrated as a function of percentage degradation. **Figure 6** depicts the J_{SC}, V_{OC}, and FF of the cells and modules as a function of relative efficiency loss for both negatively and positively biased voltage stress (i.e., Figure 6a–f, respectively).

Figure 6a–c illustrates the JV characteristics as a function efficiency loss, measured at 161, 253, and 324 h of PID stress for all stressed samples. Upon initial examination, it can be observed that all data points are tightly clustered and exhibit a consistent trend. This observation is apparent for all three different parameters. Furthermore, it can be seen that the module data closely aligns with the cell data. Notably, the cells extend further along the *x*-axis due to the greater degree of degradation in the cells during the PID stress test.

As mentioned before, subsequent to the PID stress, the voltage across the stack had been inverted for two out of four stressed samples; hence, a positive bias voltage had been applied, whereas two other samples were stored together with the reference samples. Figure 6d–f shows the JV characteristics as a function of efficiency loss, measured at 324, 403, and 847 h of the experiment (i.e., 0, 79, and 523 h of positive bias voltage stress). The data in the graphs reveal that applying a positively biased voltage has a significant, positive influence on the recovery of the JV parameters. Nevertheless, it is worth noting that storing the stressed samples after PID stress would negatively affect the parameters. From these graphs, it can be concluded that the post-stress effects are much more present or have a more pronounced influence at the module level, which can be seen by the most extreme points on the *x*-axis. The parameters of the modules were significantly closer to the initial values after applying 523 h of a positive bias voltage. Furthermore, it has been illustrated that when the samples are stored after degradation, the three JV parameters of the module-design sample become worse than the parameters of the cells. It is to be noted that when the samples have been subjected to 324 h of PID stress, the degradation of the modules is slightly lower than that of the cells. Furthermore, the positive bias voltage stress returns the module-design samples much closer to their initial values. The delayed visibility of PID in their parameters may imply that the migration of Na^+ ions has not had sufficient time to damage the structure of the modules, causing the influence of a positive bias voltage to be more significant. This hypothesis can be reinforced by the results of the module placed in a dark environment after PID stress. Here, it can be observed that the PID increased even though no more stress was applied. The possibility of a delayed impact of PID on module-design samples should be borne in mind when conducting future PID experiments. The results in each graph of Figure 6 are relatively close together for all individual cells and modules. Additionally, the results of the modules align with the trends observed in the cells. However, the poststress characteristics, both with the application of a positive bias voltage and without any bias voltage, exhibit significantly more pronounced effects in the modules compared to the cells.

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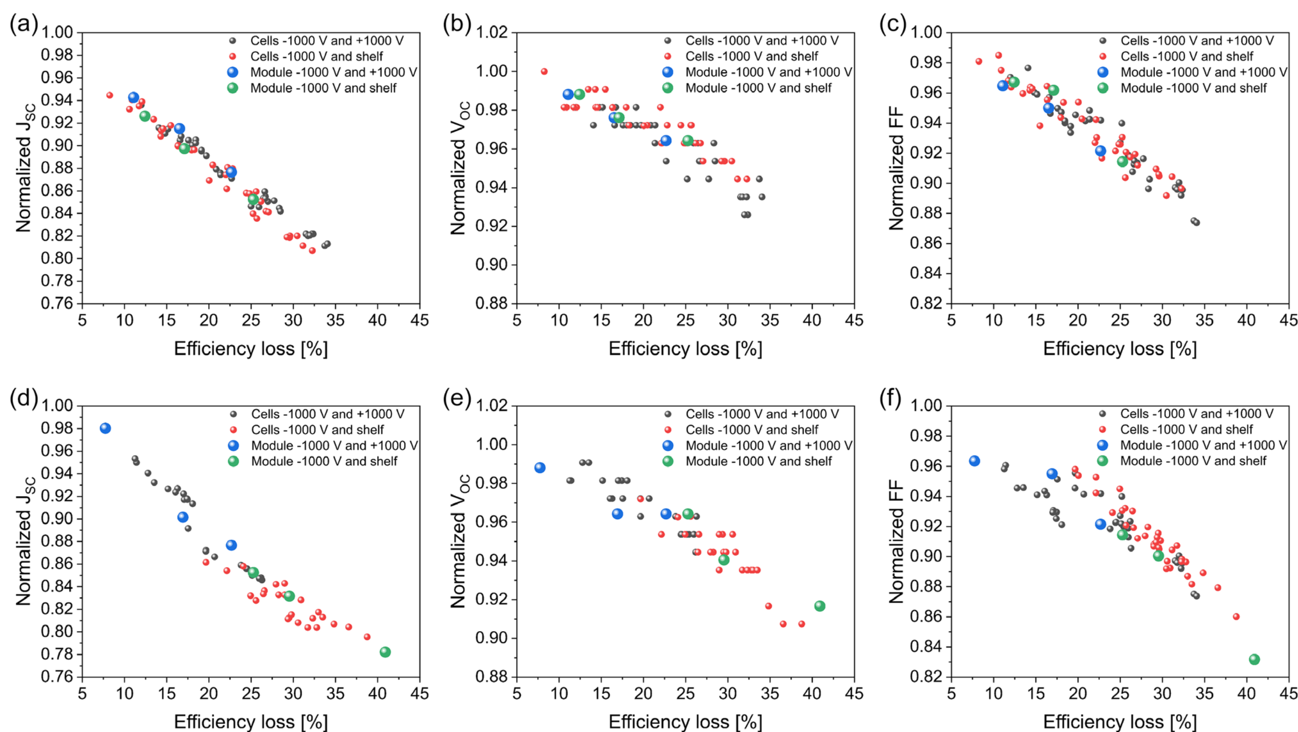

Figure 6. a–c) J_{SC}, V_{OC}, and FF as a function of relative efficiency loss at 161, 253, and 324 h of negative bias voltage stress, respectively. d–f) J_{SC}, V_{OC}, and FF as a function of relative efficiency loss at 0, 79, and 523 h of positive bias voltage stress, respectively. Here, no bias voltage was applied for two out of four samples.

4. Conclusion

Perovskite PV devices are promising candidates for the next generation of PV technologies. However, they are susceptible to environmental stressors, and deployment in the field could introduce additional degradation such as PID. Even though encapsulation could isolate the perovskite devices from oxygen and moisture, the currently used epoxy resins are not always appropriate for the perovskite layer and complete isolation can not be fully guaranteed. Moreover, it can be relevant to investigate the degradation mechanism in module-type samples, given their application in practical installations.

This study assesses PID in inert conditions without encapsulation, effectively excluding degradation mechanisms attributed to unwanted external stress factors. Furthermore, a comparison of PID susceptibility between perovskite cells and modules is presented.

The results presented in this article reveal that both PSCs and PSMs demonstrate similar behavior during the 324 h of negative bias voltage stress, with the observation that the degradation rate within the PSMs is lower. It was observed that the degradation mechanism mainly affected the J_{SC} and reduced the V_{OC} and FF, nevertheless, to a lesser extent. Notably, the degradation rate during this study is significantly lower compared to other studies presented so far, while using similar architectures and stress conditions. This suggests that this method of operating in a nitrogen environment without encapsulation could be ideal for accurately investigating the PID mechanism while excluding environmental stressors.

Throughout the 523 h positive bias voltage stress, there was a noticeable increase in the efficiency for both cells and modules. However, full recovery was not obtained. Additionally, the stressed modules exhibit distinct behavior compared to the stressed cells, both with or without positive bias voltage stress. The recovery of the module is notably higher compared to the recovery of the cells. Nevertheless, further research is required to investigate whether this discrepancy is due to the modules not being initially degraded to the same degree as the cells, owing to their distinct degradation rates, or if a different mechanism is influencing the outcomes. Furthermore, comparing the degraded cell and module-design samples without positive bias voltage stress, it can be seen that the degradation progresses to a significantly greater extent in the module-design sample. Additionally, it is evident from the JV graphs that the V_{OC}, J_{SC}, and FF decreased within the modules, whereas the J_{SC} was not significantly affected at the cell level. Hence, whether exactly the same degradation mechanisms are occurring is still being determined.

However, further research with more samples and extensive microstructural analysis is needed to make it more statistically relevant and to provide deeper insights. Further research, including microstructural analysis, must clarify the underlying physics. This analysis is imperative to elucidate the factors contributing to the difficulty of achieving full recovery and the divergent responses observed in cell and module-design samples following PID stress testing. It needs to be investigated whether these effects are genuinely different degradation mechanisms resulting from architectural differences (i.e., P1P2P3 scribing,

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differences in area). Furthermore, due to the sensitivity of perovskite, it is suggested to gradually include other stress factors (i.e., moisture, oxygen. temperature, light, encapsulation, etc.) to understand the different effects accurately and ultimately engineer effective mitigation strategies.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

inert environment, methods, modules, potential-induced degradation, recovery, unencapsulated

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