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CFET channel stack fabrication by wafer-to-wafer bonding and BESOI donor dismounting

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ABSTRACT

We focus on the fabrication of a Complementary Field Effect Transistor (CFET) stack with two distinct four-periods Si/SiGe epitaxial superlattices isolated from one another by a thin thermal SiO_2 layer. The structure is built using oxide-oxide wafer-to-wafer direct bonding and a Bond and Etch Back SOI (BESOI) approach to transfer the donor stack onto the receiver wafer. Key process steps of this fabrication flow are described including the superlattice epitaxial growth, the formation of the thermal oxide bonding layer, the molecular hydrophilic bonding and finally the donor wafer dismounting with extensive physical characterizations performed at each step. This process flow yields defect-free CFET channel stacks provided that the thermal oxide growth is well controlled and limited to a thickness of about 15 nm on top of each superlattice (i.e. a MDI thickness of at most 30 nm), a value compatible with the specifications of future CFET devices.

1. Introduction

The complementary field effect transistor (CFET) architecture is positioned as the best solution to be deployed around 2030 at the 14 Å More Moore technology node [1]. Major integrated device manufacturers and research and technology organizations such as CEA-Leti and IMEC are actively developing this complex technology involving novel process bricks, many breakthroughs and new equipment capabilities [2], [3], [4], [5].

In the CFET architecture, N- and P-MOS devices are placed on top of one another, thus completely removing areas consumed by N-P spacings in planar architectures. This results in a maximization of the effective channel width and, hence, the drive current. Such devices can be fabricated using either a monolithic or a sequential approach [6]. In the first option, N- and P-MOS transistors are built on the same wafer. Meanwhile, with the sequential approach, P-MOS and N-MOS Si/SiGe stacks are fabricated independently [2]. Flexibility is then larger in terms of individual layer thickness, maximum Ge concentrations allowed and crystalline orientation, to name a few. The Middle-Dielectric-Isolation (MDI) layer is directly built-in during the sequential CFET fabrication flow, avoiding the use of sacrificial SiGe stacks as in the monolithic approach. Finally, the use of various types of dielectrics (such as SiO_2, SiN or SiCN) is also facilitated, a feature which will be beneficial for device integration and eventually for the minimization of parasitics between N- and P-MOS transistors.

A high-quality wafer-to-wafer bonding of the two tiers at the MDI interface without any degradation of the integrity of the two Si/SiGe superlattices is essential for sequential CFET integration. The resulting stacks should be robust against downstream processes, e.g., the bonding interface should notably be resistant to the multiple wet cleanings or etchings used later on.

Wafer dismounting is the last key step of this sequential flow. A Bond and Etch Back SOI (BESOI) or a Smart Cut™ approach could be used to that end [7]. The first method involves the use of a silicon-on-insulator (SOI) substrate for the donor wafer, with the buried oxide being a convenient etch stop layer in order to have a soft landing on the first active SiGe layer met upon dismounting. Meanwhile, the second approach implies to implant the fracturing species in the donor wafer

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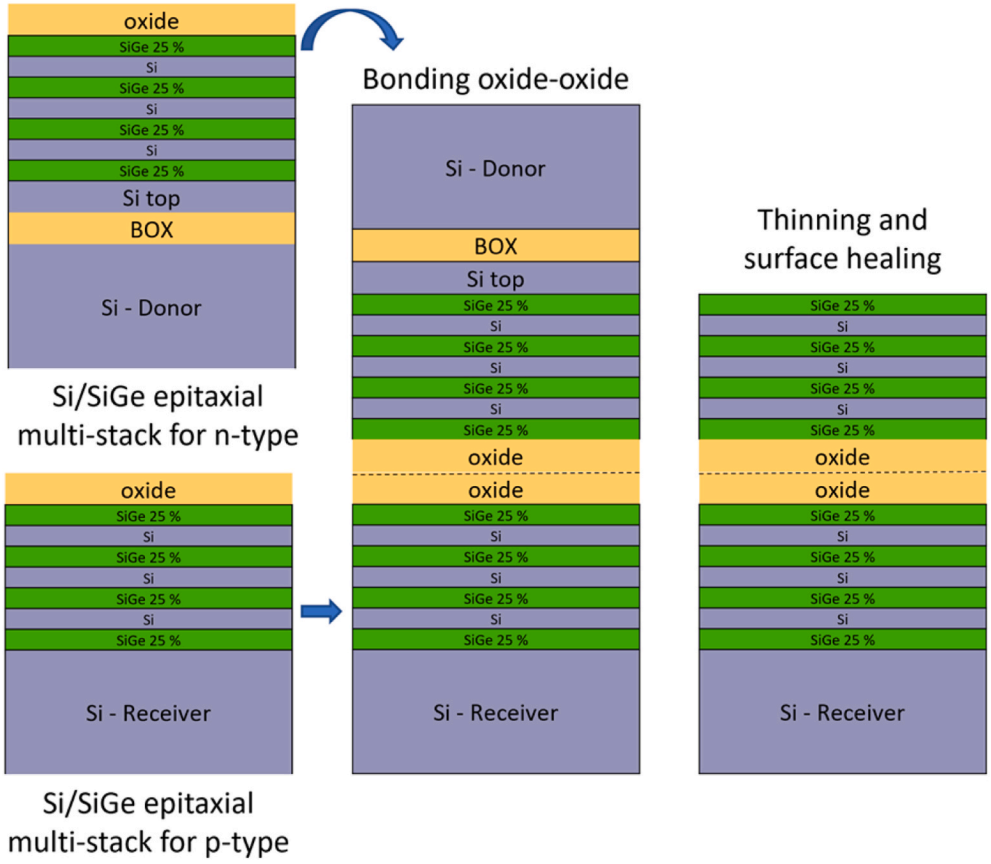

Fig. 1. CFET channel stack fabrication using a layer transfer approach and BESOI donor wafer dismounting.

through (i) the Si/SiGe superlattice, without degrading its structural and electrical integrity and (ii) a fraction of the MDI layer, without impacting the quality of the bonding interface. This method is thus much more challenging. In the current paper, we will therefore focus solely on the use of a BESOI route.

2. Fabrication process flow

The overall process flow, implemented at CEA-Leti, is depicted in Fig. 1. Si/SiGe superlattices were epitaxially grown on the receiver bulk Si wafer and the donor SOI wafer. Oxide layers were subsequently fabricated thanks to the thermal oxidation of the silicon layers sitting on top of those superlattices. The thickness of Si overlayers was such that it yielded half the targeted MDI thickness. The two wafers were then bonded using a direct bonding technique with a specific surface preparation and a controlled bonding atmosphere. A batch annealing was then performed at 500 °C to strengthen the bonding interface. A specific attention was paid to the overall thermal budget for layer transfer (e.g., that of the thermal oxidation for MDI formation then that for the post bonding annealing) to preserve the structural integrity of the Si/SiGe multilayers.

3. Si/SiGe superlattice epitaxy

3.1. Process description and setup

The SiGe/Si donor and receiver superlattices were epitaxially grown at 650 °C, 20 Torr on 300 mm bulk Si or SOI substrates in a reduced-pressure chemical vapor deposition (RPCVD) reactor from Applied Materials. Those superlattices consisted in four $Si_{0.75}Ge_{0.25}$ layers and three Si spacer layers, each 9 nm thick, capped with sacrificial Si layers of variable thicknesses which were fully oxidized to form the bonding oxide layer and finally the MDI (Fig. 2a).

3.2. Characterization

Fig. 2b shows a cross-sectional Transmission Electron Microscopy (TEM) image with well-defined interfaces between Si and SiGe layers. The extracted individual layer thicknesses were close to the targeted value of 9 nm as confirmed by the Energy Dispersive X-ray spectroscopy (EDX) profile shown in Fig. 2d. The latter also confirms the presence of sharp Ge concentration gradients at the different interfaces, identical individual layer thicknesses and the reaching of the targeted germanium content (25%).

Si and Ge depth profiles were determined thanks to time-of-flight secondary ion mass spectrometry (ToF-SIMS) in a ToF-SIMS 5 instrument from ION TOF GmBH. For secondary ions analysis, the Bismuth LMIG gun was tuned to deliver primary Bi_3^+ cluster ions energized at 25 kV and with a current of 0.6 pA. The analysis area of 75 × 75 μm^2 was described in 128x128 pixels for negative polarity secondary ions. Depth analyses were carried out with 500eV Cs^+ primary sputtering ions with a 30 nA current and a raster size of 300x300 μm^2. The composition profiles of the SiGe/Si stack are similar in different areas of the wafer. Indeed, as shown in Fig. 2c ToF-SIMS Ge depth profiles can be superimposed at the center, at mid-radius and at the edges of both bulk Si receiver and SOI donor wafers. Interfaces are otherwise chemically sharp (Si on SiGe) to very sharp (SiGe on Si). Individual thicknesses, thickness uniformities and interface sharpness were confirmed by X-Ray Reflectivity (XRR) measurements (Fig. 2e and Table I). Individual layer thicknesses were lower close to the wafer edges than at centers. The

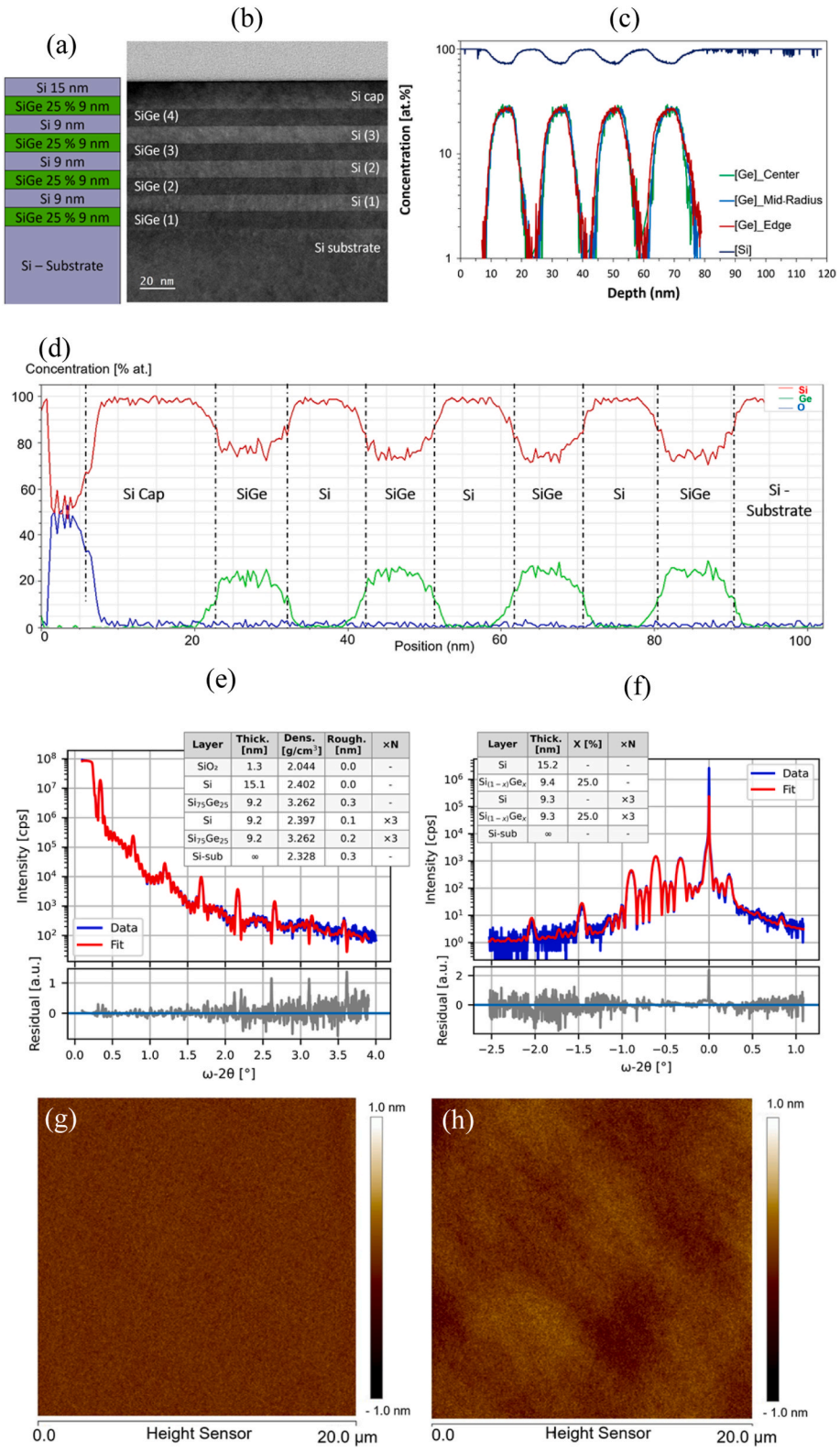

Fig. 2. (a) Schematic cross-section of the epitaxial stack on a bulk Si donor wafer, (b) cross sectional TEM image, (c) ToF-SIMS depth profiles of $[Ge]^-$ and [Si] signals at the center (green line), mid-radius (blue line) and the edge (red line) of the wafer, (d) EDX profile, (e) measured and modelled XRR profiles with the residuals highlighting the goodness of fit, (f) HRXRD ω-2Θ scan around the (004) Bragg peak (in blue) and its superlattice model fit (in red) and AFM 20 × 20 µm^2 images of the top SiGe surface after epitaxy on (g) Si bulk and (h) SOI substrate. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

Table 1
Individual thicknesses of the topmost four layers of a Si/SiGe superlattice grown on bulk Si for different positions over the wafer, from center (0 mm) to the edge (140 mm) and interface sharpnesses at the wafer center as extracted from XRR measurements.

X-pos	Thickness (nm)			
	SiGe0.25	Si-ch	SiGe0.25	Si-cap
0	9.1	9.2	9.1	15.5
35	9.2	9.2	9.1	15.5
70	9.4	9.5	9.3	16.1
105	9.4	9.6	9.2	16.0
140	8.6	8.7	8.3	14.6
Average	**9.1**	**9.3**	**9**	**15.5**
Rel. Std. Dev.	**3.6 %**	**3.7 %**	**4.7 %**	**3.6 %**
Interface sharpness center	2.86 Å	1.16 Å	2.03 Å	

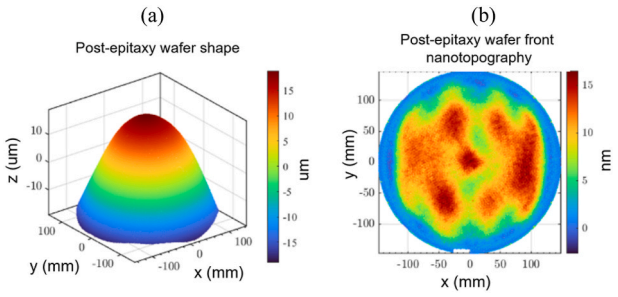

Fig. 3. (a) Wafer shape after growth on a bulk Si donor, measured in a free hanging position. A slight umbrella shape is found ranging from −20 to +20 µm. (b) Nanotopography map of the same wafer as in (a), with significant variations ranging from 0 to ~15 nm (from center to wafer edges).

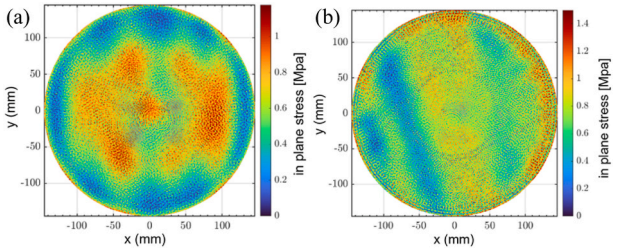

Fig. 4. In-plane stress distribution after the growth of superlattices on (a) bulk Si (same wafer as in Fig. 3) and (b) a SOI substrate. Stress distribution in both wafers largely reflects the nanotopography distribution on the front surface, except at the very edges, where the stress is higher.

presence of well-resolved XRR thickness fringes up to high incidence angles confirmed the high quality of those stacks. Surface haze maps measured using a KLA Surfscan® SP5 tool showed that surfaces were smooth. Finally, a Ge concentration close to the targeted value of 25% and individual layer thicknesses very similar to that in XRR were deduced from careful fittings of High-Resolution X-Ray Diffraction (HRXRD) omega-2theta scans (Fig. 2f). Those data were extracted by fitting the measured curve with the Bruker JV RADS software, with a superlattice model for the simulation of buried layers. Surfaces of the SiGe/Si donor and receiver superlattices were smooth and featureless, with a Root Mean Square roughness lower than 0.1 nm. This was confirmed by AFM measurements performed over 20 × 20 µm^2 areas on both Si bulk and SOI substrates, as shown in Fig. 2g and h.

Nanotopography and wafer shapes (while holding them in a gravity-neutralised position) just after epitaxy were determined thanks to dual sided Fizeau interferometry in a PWG (Patterned Wafer Geometry) tool from KLA. Fig. 3a for instance shows that a bulk Si wafer with a SiGe/Si superlattice on top has an inverted bowl shape, with its front side bulging upwards. The nanotopography on its front side is shown in Fig. 3b, with up to ~15 nm variations. The nanotopography taper close to wafer edges, indicating some growth nonuniformity.

For a given stack of thickness t the (both bonded or unbonded-) wafer shape could be remapped onto a mesh and gradients of the shape could be computed to derive the effective strain in the wafer as

$$\epsilon_{xx} = \frac{-t}{2}\frac{d^2z}{dx^2}, \text{and } \epsilon_{yy} = \frac{-t}{2}\frac{d^2z}{dy^2},$$

which can be multiplied by the bulk material's elastic modulus E to obtain the in-plane stress distribution ($E\epsilon_{xx}$ and $E\epsilon_{yy}$) in the stack. The averaged in-plane stress (and not that in individual layers) is shown in Fig. 4 for the wafer probed in Fig. 3. While the stress distribution resembles the front side nanotopography (Fig. 3b) in the central region, it is higher at the very edges, possibly due to a sharper curvature originating from the thickness non-uniformity of as-grown layers.

4. Middle dielectric isolation by thermal oxide growth

4.1. Process description and setup

The MDI layer is formed thanks to the thermal oxidation of the Si cap layers on donor and receiver wafers. Oxidation has to be well controlled not to partially consume the first SiGe layers under the Si caps which would degrade the superlattice integrity. The thermal wet oxidation was performed at 700 °C in a vertical batch furnace for several hours. Two SiO_2 thicknesses, 20 nm and 36 nm, were evaluated, starting from 10 nm and 15 nm thick Si caps, respectively, and considering a theoretical ratio of 0.44 between consumed silicon and resulting SiO_2 thicknesses.

4.2. Characterization

Spectroscopic Ellipsometry (SE) and High-Resolution Transmission Electron Microscopy (HRTEM) were used to characterize the grown oxide. For samples on which 20 nm of SiO_2 were grown by a partial oxidation of 10 nm thick Si caps, the grown oxide exhibited a good wafer uniformity with a total thickness variation below ±0.5 nm. The oxide thickness was otherwise very close to the targeted value (Fig. 5b). Thicknesses determined from TEM cross-sections were, taking into account error bars, fully in agreement with the ellipsometry values (Fig. 5c). The surface morphology after oxidation remained of excellent quality, with a low RMS roughness (lower than 0.13 nm), as evidenced by AFM scans over 20 × 20 µm^2 areas on both Si bulk and SOI substrates (Fig. 5d and e).

The cross-sectional TEM image of the bulk Si receiver after such a thermal oxidation confirms the excellent crystalline quality of the SiGe/Si superlattice (Fig. 6a), with interfaces and individual layer thicknesses that were not altered by the oxidation process. This image also highlights the presence of a 1 nm thick Si layer beneath the SiO_2 cap that was not oxidized, confirming that the oxidation was partial. The EDX profile in Fig. 6b shows that the superlattice was not altered by the oxidation process, with the same Ge and Si concentration profiles than just after epitaxy. This result was confirmed thanks to a HRXRD omega-2theta scan (Fig. 6c), with individual layer thicknesses and Ge concentrations matching post epitaxy measurements. This measurement shows also the presence of a thin Si top layer that was not oxidized. A different superlattice model, more suitable for this stack was used for curve fitting. These results are confirmed by Fig. 6d ToF-SIMS profiles at the center and mid-radius of such an oxidized stack. The $^{18}O^-$, $^{30}Si^-$ and Ge_2^- signals are once again superimposable: Ge^{2-} profiles are still sharp, whereas the $^{30}Si^-$ in-depth distribution confirms the presence of an

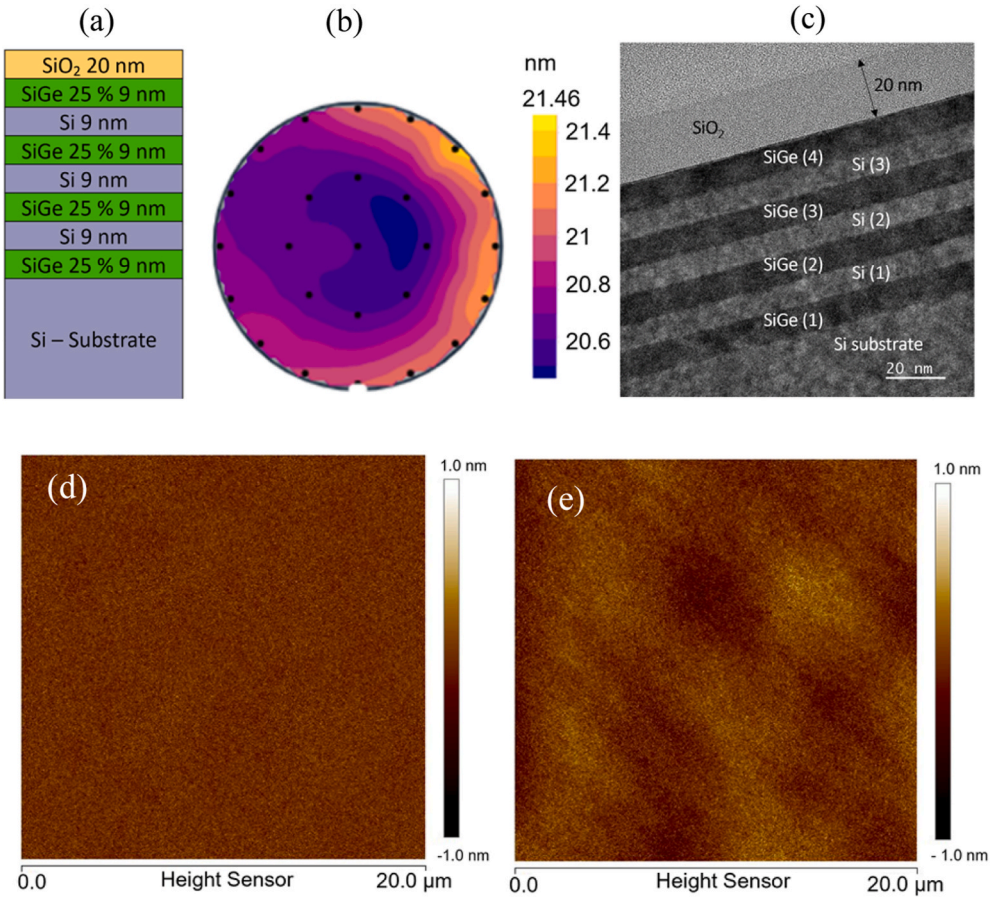

Fig. 5. (a) Schematic cross-section, (b) wafer map of the SiO_2 thickness from Spectroscopic Ellipsometry (SE), (c) cross-sectional TEM image of the SiGe/Si superlattice and $20 \times 20\ \mu m^2$ AFM images of the oxide surface on (d) Si bulk and (e) SOI substrate after low temperature thermal oxidation.

unoxidized ~1 nm thick Si top layer.

A second series of wafers was fabricated with 36 nm thick SiO_2 layers grown by oxidizing 15 nm thick silicon caps. Under these conditions, a complete oxidation of the silicon caps was anticipated. As a result, the resulting oxide exhibited significant deviations from targeted specifications (Fig. 7a).

- the final oxide thickness was substantially higher than expected (40 nm vs 36 nm);
- at the wafer edge, the measured oxide thickness reached up to 60 nm.

These observations were confirmed by Energy Dispersive X-ray Spectroscopy EDX (Fig. 7b). The TEM/EDX cross section analysis further revealed (Fig. 7b and c).

- a 2 nm downward displacement of the top SiGe layer into the underlying Si layer;
- a reduction of the top SiGe layer thickness down to 3 nm, together with an increased germanium concentration of up to 40%. This Ge condensation effect has already been reported in the literature [8], [9].

In regions at the wafer edge where such a thick oxide was present, specific crystalline defects were observed (Fig. 8). These defects consisted of faceted Ge-rich inclusions within the silicon spacer layer beneath the first SiGe layer.

These findings highlight the critical importance of precisely controlling the oxidation process to avoid even a partial oxidation of the first SiGe layer, as uncontrolled oxidation leads to a rapid degradation of the superlattice structural integrity and to a defective oxide/semiconductor interface [10]. To mitigate this issue, under-oxidation of the Si cap is necessary, with the preservation of a thin silicon layer (at least 1 nm, possibly a few nm) between the first SiGe layer and the thermal oxide formed on top.

PWG showed that thermal oxide growth changed the wafer surface topography. Changes in front side nanotopography on (a) bulk Si and (b) SOI wafers are shown in Fig. 9. Nanotopography changes after thermal oxidation closely mirror the in-plane stress pattern measured by PWG on as-grown Si/SiGe superlattice wafers. Regions that exhibited higher in-plane stress prior to oxidation showed a more pronounced upward or downward surface displacement after oxide growth. Consequently, the oxidation-driven modification of the wafer topography was not uniform. It was instead modulated by the initial stress field inherited from the epitaxial stack growth.

5. Wafer-to-wafer direct bonding

5.1. Process description and setup

The donor and receiver wafers were chemically cleaned to obtain optimal surface states and a defect free interface upon oxide-oxide direct bonding. Standard DiO_3 and RCA cleanings removed organic and particular contamination. Ethalonamine was used prior to bonding in an EVG850LT bonding tool in order to increase the adherence energy and

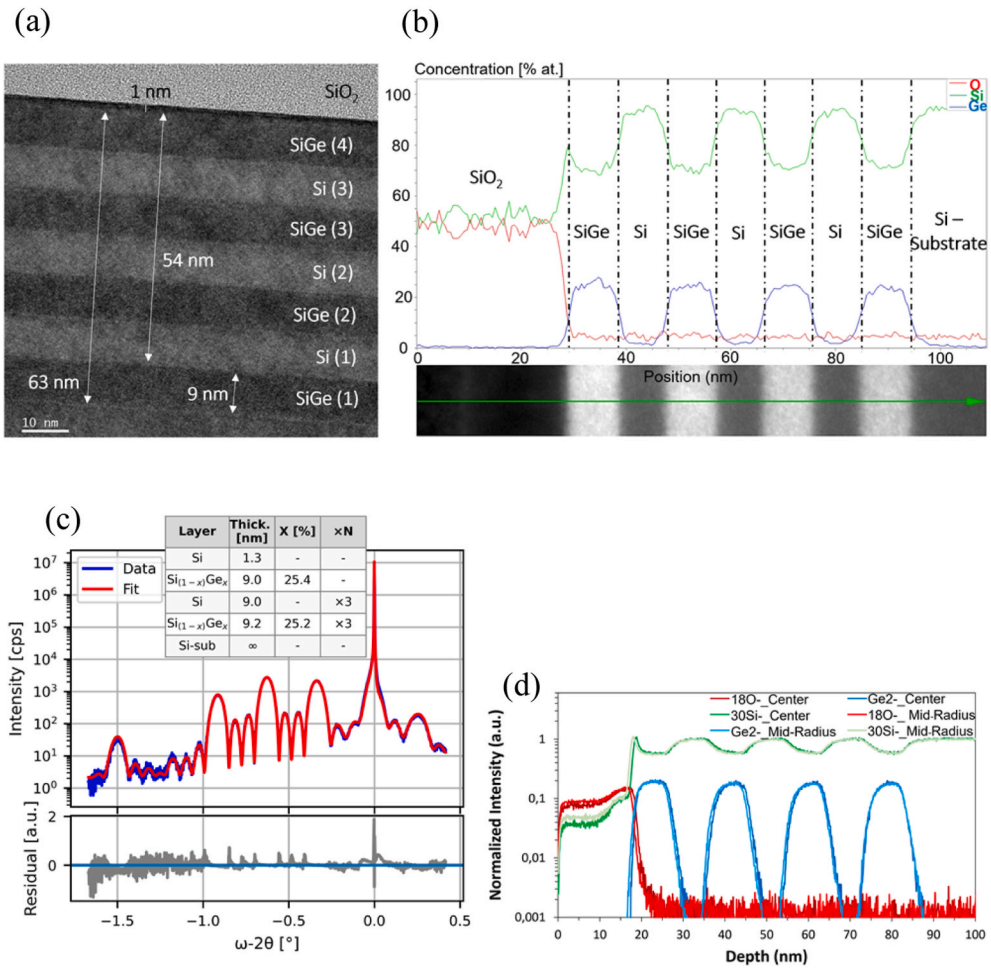

Fig. 6. (a) Cross sectional TEM image, (b) EDX profile, (c) HRXRD ω-2Θ scan around the (004) Bragg peak (in blue) and its superlattice model fit (in red) of the bulk Si receiver and (d) ToF-SIMS depth profiles of Ge_2^-, $^{30}Si^-$ and O^- signals at the center and the mid-radius of the wafer, after under-oxidation. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

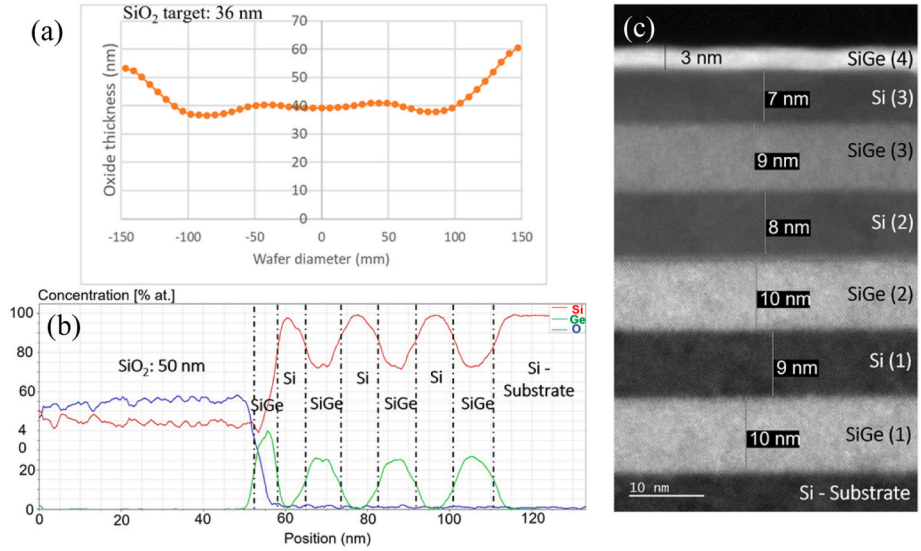

Fig. 7. (a) Oxide thickness along the wafer diameter from SE, (b) EDX profile and (c) cross sectional High Angle Annular Dark Field (HAADF) STEM image of the superlattice donor after over-oxidation.

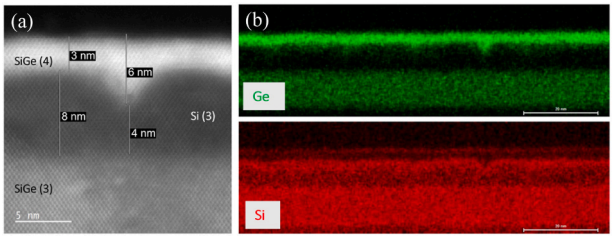

Fig. 8. (a) Cross-sectional HAADF STEM zoom on a crystalline defect in the superlattice after over-oxidation and (b) chemical analysis of the defective area.

avoid defectivity [11]. Moreover, humid helium at 40% RH was used as the bonding atmosphere to get rid of edge bonding voids while keeping a good adhesion energy [12]. The superlattice donors and receivers were then aligned and bonded together. After bonding, a batch annealing was performed at 500 °C to consolidate the bonding interface.

5.2. Characterization

The bonding interface was characterized using Scanning Acoustic Microscopy (SAM), TEM and EDX. The SAM image (Fig. 10a) showed that bonding was homogeneous and void-free across the entire wafer. A good strengthening thanks to ethalonamine was achieved, without any trace of an interface in cross-sectional TEM (Fig. 10b). The EDX profile (Fig. 10c) indicated that the superlattice structure remained intact, with sharp Si/SiGe transitions identical to those observed prior to bonding.

The direct bonding process, combined with optimized chemical cleaning and annealing, thus produced a high-quality interface between the superlattice donor and receiver wafers. The controlled bonding of oxide-oxide layers yielded a 40 nm thick MDI layer without altering the superlattice structure.

6. Donor wafer dismounting

6.1. Process description and setup

P-MOS/N-MOS Si/SiGe superlattices with a 40 nm thick SiO_2 MDI were finally obtained by dismounting the SOI donor substrate with the BESOI approach. Following the bonding step, the donor wafer underwent successive silicon grindings and wet etchings to obtain in the end the final CFET structure (Fig. 11a). The buried oxide (BOX) layer of the SOI donor wafer served as an etch-stop layer for substrate removal, with a subsequent chemical etching selectively stopping at the first SiGe layer of the N-MOS superlattice sitting on top.

6.2. Characterization

Spectroscopic Ellipsometry measurements were performed on the upper Si/SiGe stack. The measured overall thickness matched the targeted value of 63 nm across most of the wafer but decreased towards the wafer edges (Fig. 11b and c), in line with measurements at the epitaxy stage. An excellent wafer-to-wafer reproducibility was nevertheless demonstrated in this study. This reproducibility was shown using wafer shapes, measured on all the wafers post dismounting. The mean of shapes of the four wafers with 40 nm MDI, post dismounting, are shown in Fig. 12a. The standard deviation of these four wafers measured are shown in Fig. 12b, with less than ~1.3% variations.

SiO_2-MDI thickness was also precisely monitored using spectroscopic ellipsometry (Fig. 13). Measurements showed a very good control of the MDI thickness across the entire wafer within the target specifications and with an excellent wafer to wafer reproducibility, as well.

TEM imaging of the final fabricated structure showed once again the presence of sharp, defect-free Si/SiGe interfaces, while EDX mapping confirmed the expected chemical composition modulation between Si and $Si_{0.75}Ge_{0.25}$ layers (Fig. 14b). Fig. 14c HRXRD reciprocal space mapping (RSM) showed periodic peaks at different Qx positions due to the fact that donor and receiver substrates were different. After bonding, the atomic column of the top and bottom stacks were not aligned (because of tilt and twist), hence the two sets of superlattice peaks in the RSM. Fig. 14c map was also typical of a superior crystalline quality stack, with distinct satellite peaks associated to each superlattice, indicating a successful preservation of their periodic structures throughout the fabrication process. However, lateral peak broadening for upper compared to lower stacks may indicate a difference in terms of crystalline quality between the two superlattices. These results validate the effectiveness of our wafer-bonding approach in maintaining high-quality superlattice integrity in complex stacked architectures. EDX and ToF-SIMS profiles shown in Fig. 14d and e also highlight that the final stack is indeed made of high-quality superlattices with the expected composition and periodicity, without any significant germanium and silicon interdiffusion between layers.

The final inspection of the SiGe top layer surface was performed using optical profilometry and atomic force microscopy (AFM) (Fig. 15a and b). This analysis revealed the presence of lines most likely associated to the presence of misfit dislocations in the CFET stack. Those findings were subsequently confirmed by electron channeling contrast imaging (ECCI) performed in a Scanning Electron Microscope (SEM) using an insertable backscattered electron detector (Fig. 15c). The misfit dislocations likely extended through the entire channel stack, as the top SiGe layer imaged in AFM and optical profilometry was actually the first epitaxially grown layer on the donor SOI stack.

To elucidate the origin of dislocations observed in the SiGe top layer,

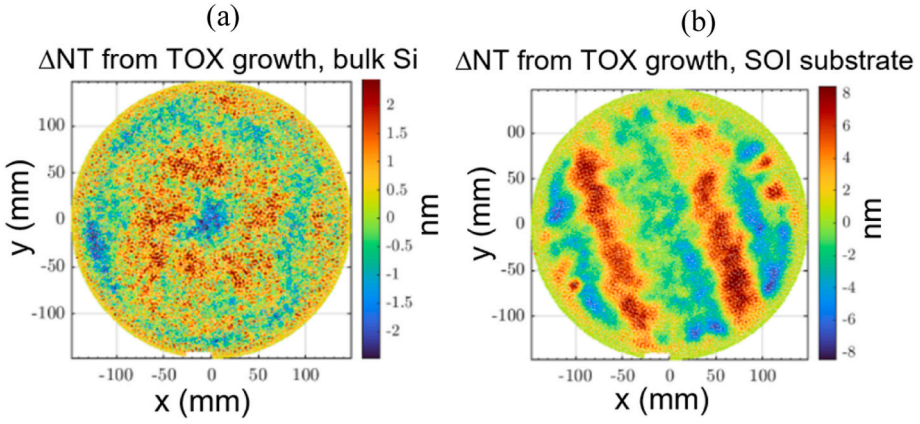

Fig. 9. Nanotopography changes on the front sides of wafers after oxide layer growth on (a) bulk Si and (b) SOI substrates (comparison with nanotopography after superlattice growth).

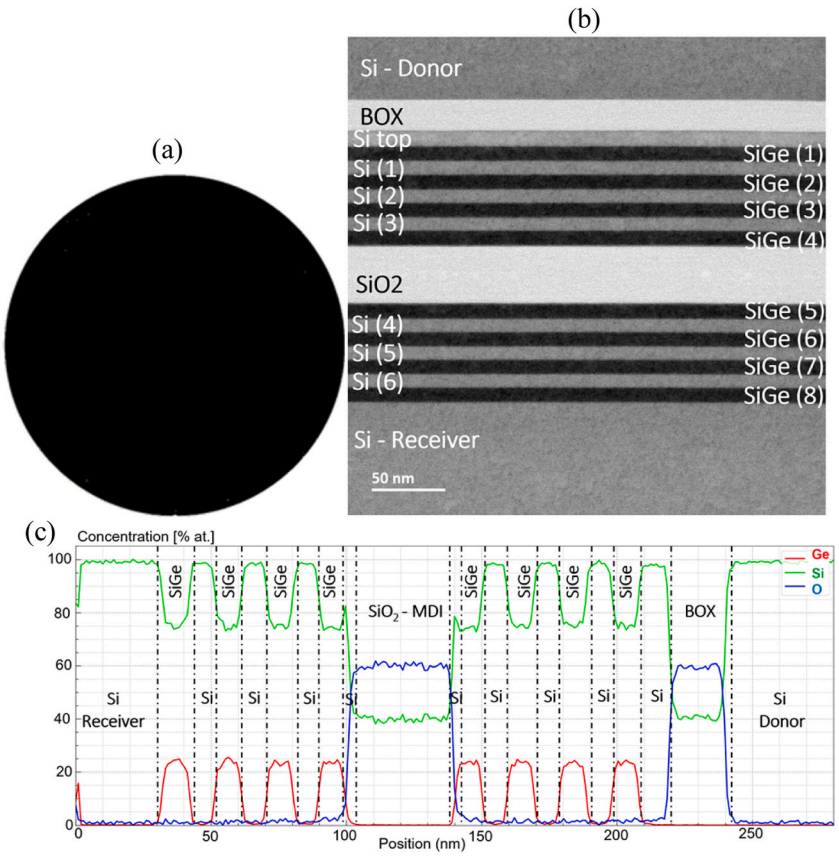

Fig. 10. (a) SAM image of the bonding oxide-oxide interface, (b) Cross-sectional TEM image and (c) EDX profile of the donor and receiver stacks after bonding.

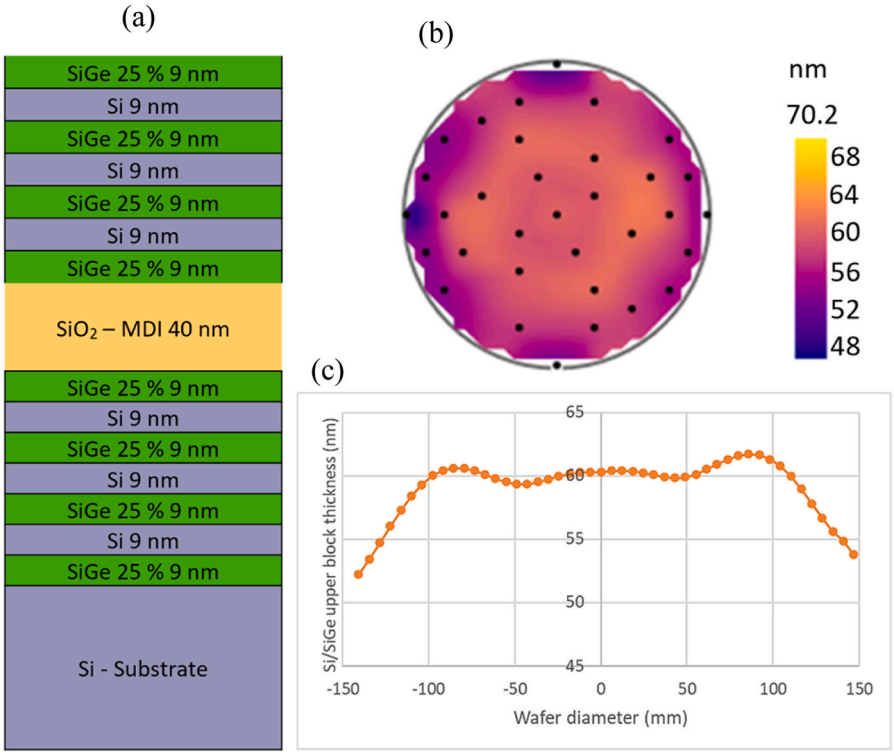

Fig. 11. (a) Schematic cross-section of the final SiGe/Si CFET structure, (b) wafer map and (c) wafer diameter scan of the Si/SiGe upper stack overall thickness at process end.

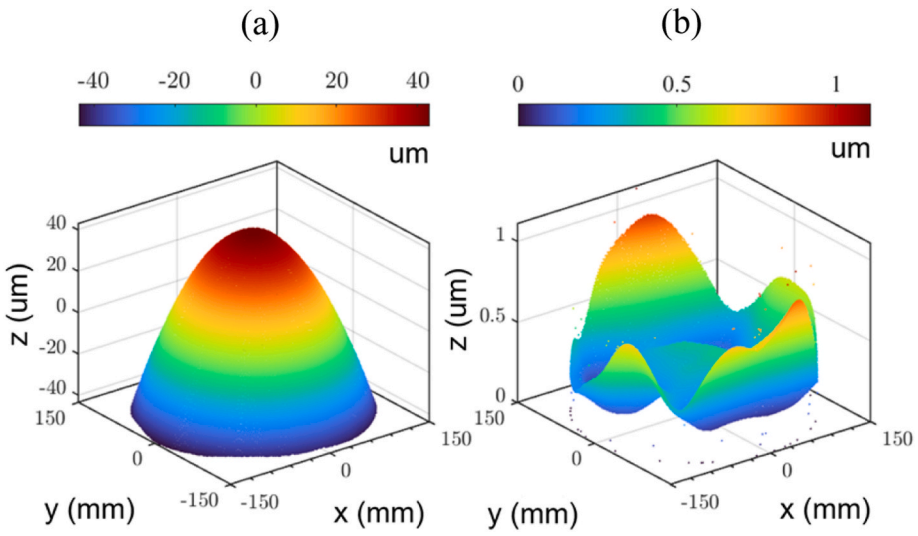

Fig. 12. (a) Mean of the shapes of four wafers after dismounting, each with 40 nm MDI. (b) Standard deviation over the four measurements shown in panel (a).

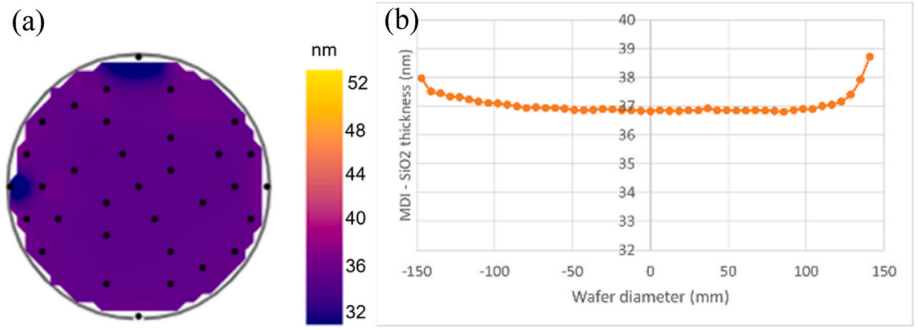

Fig. 13. (a) Wafer map and (b) wafer diameter measurement of the SiO_2-MDI thickness at process end.

which were not detected just after epitaxy nor post-oxidation (Figs. 2 and 5), we conducted two complementary experiments. The first one consisted in performing the thermal oxidation followed by a selective oxide removal on a SOI substrate with the same targeted epitaxial stack as on the donor wafer and conducting the same surface inspection. The second was to perform a N_2 annealing, instead of an oxidation, with the same thermal budget as that for 20 nm thermal oxide growth. Both experiments consistently revealed the presence of misfit dislocations (Fig. 16) when using a thermal budget equivalent to that for 20 nm thermal oxide growth, suggesting that the oxidation process itself was the root cause of these defects. Surface light point defect (LPD) maps confirmed that misfit dislocations were present over large wafer areas, although the haze values were not significantly higher than that of as-grown stacks. After oxidation, misfit dislocations were detected for Si/SiGe superlattices grown on SOI as well as on bulk Si. The presence of misfit dislocations was also reflected in RSMs, with a widening of individual peaks compared to that on as-grown superlattices. These findings, likely due to a plastic relaxation of the compressive strain in the SiGe/Si superlattices, corroborate our earlier observations of surface defects on the final CFET stack (Fig. 15).

We thus conducted a systematic study to determine the maximum allowable thermal budget (and thus the maximum thermal oxide achievable) before dislocation formation. Our findings showed that 15 nm of thermally grown oxide (and thus an overall MDI thickness of 30 nm) was the upper limit (Fig. 17). Above this thickness, dislocations started to form. This threshold corresponded then to a critical thermal budget for our $Si/Si_{0.75}Ge_{0.25}$ structure.

The selected oxidation temperature (700 °C) was the only one enabling thermal oxidation with a still acceptable process duration (a few hours, still). Given the scope of that study with numerous process steps used, we did not screen other oxidation temperatures.

7. Conclusions

This study successfully demonstrates the fabrication of an innovative P-MOS/N-MOS CFET structure featuring three active silicon layers in the top and bottom stacks separated by SiGe sacrificial layers, achieved through a novel combination of wafer bonding and BESOI donor wafer dismounting. The process features high-quality dielectric isolation through controlled thermal oxidation of a top Si layer on each SiGe/Si superlattice, providing excellent resistance to downstream processing steps, particularly against HF-based chemical treatments. However, results reveal an inherent limitation related to the thermal budget of the silicon oxidation limiting to a maximum Middle Dielectric Isolation (MDI) thickness of approximately 30 nm (15 nm on each side) to maintain superlattice integrity. Such a constraint is however in conformity with current CFET integration roadmaps featuring thin MDI to limit parasitic capacitance between N and P devices. Future work will explore

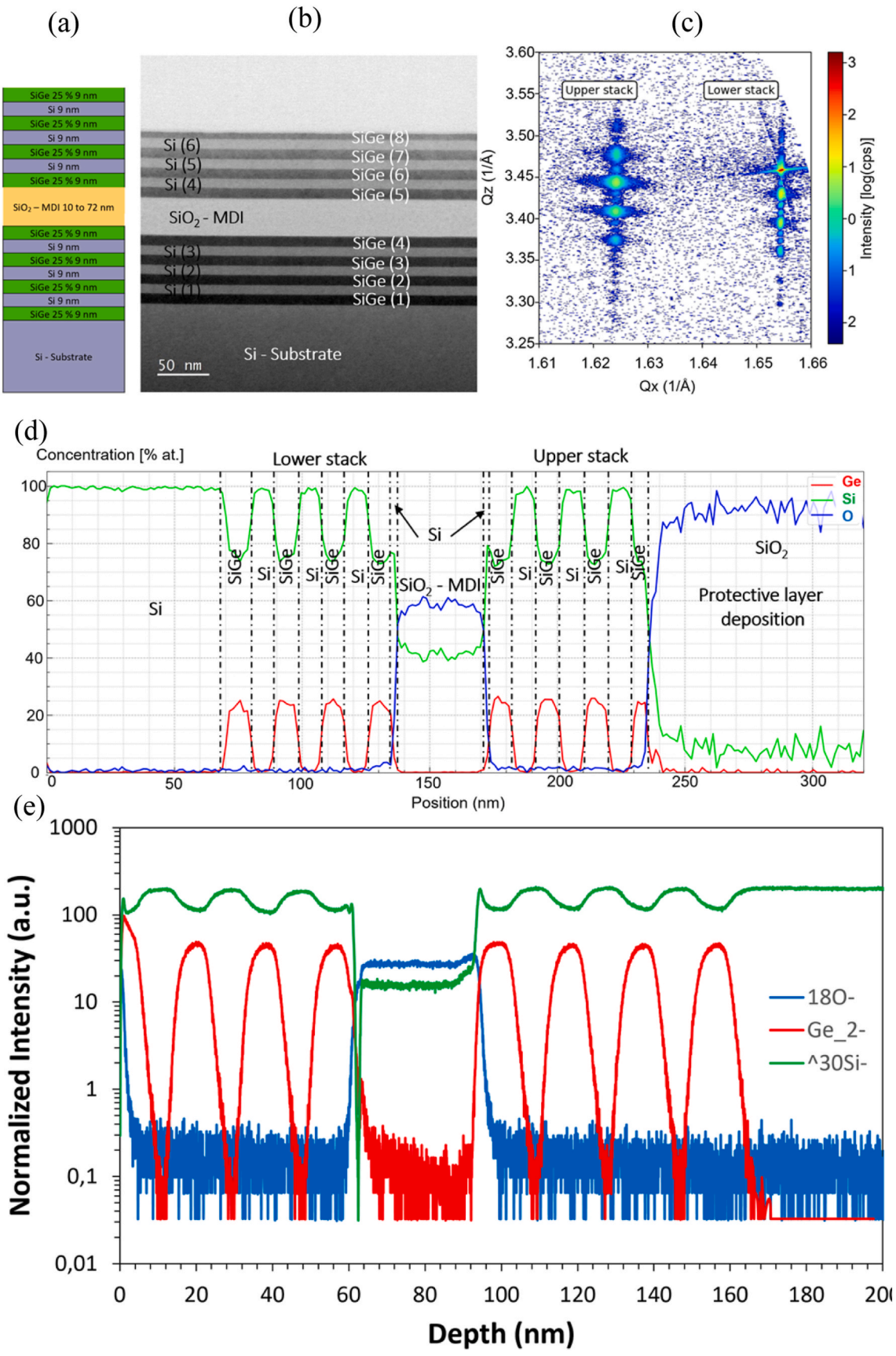

Fig. 14. (a) Schematics of the final CFET structure with a 40 nm thick MDI after the removal of the donor wafer, (b) cross-sectional TEM image of the resulting stack, (c) HRXRD-RSM around the (113) Bragg reflection with well-defined periodic peaks at different Q_X positions for top and bottom superlattices, (d) EDX profiles of the Si, Ge and O concentrations and (e) ToF-SIMS depth profiles of Ge_2^-, $^{30}Si^-$ and O^- signals.

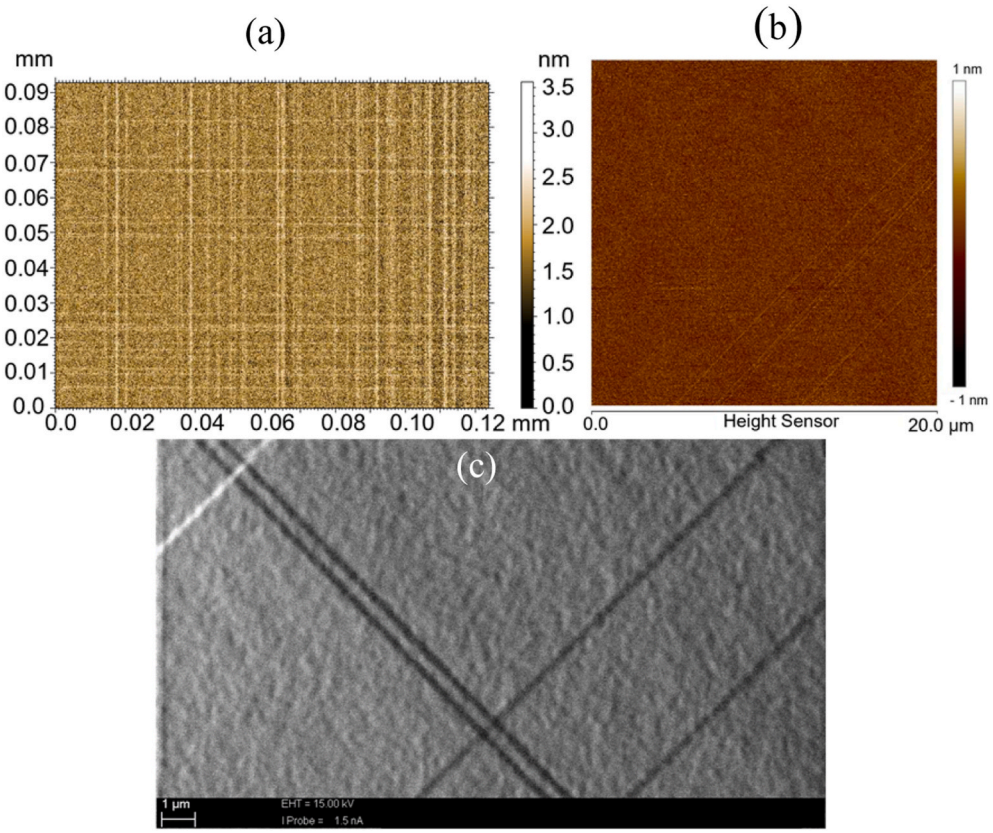

Fig. 15. (a) $90 \times 120\,\mu m^2$ optical profilometer image and (b) $20 \times 20\,\mu m^2$ AFM image of the top SiGe surface of a CFET stack with a 40 nm thick MDI showing the presence of lines most likely stemming from the propagation of the theading arms of 60° misfit dislocations on {111} planes. (c) ECCI imaging of dislocations in the CFET stack. The sides of the optical profilometer image are along the <110> directions while the sides of AFM and ECCI images are along the <100> direction.

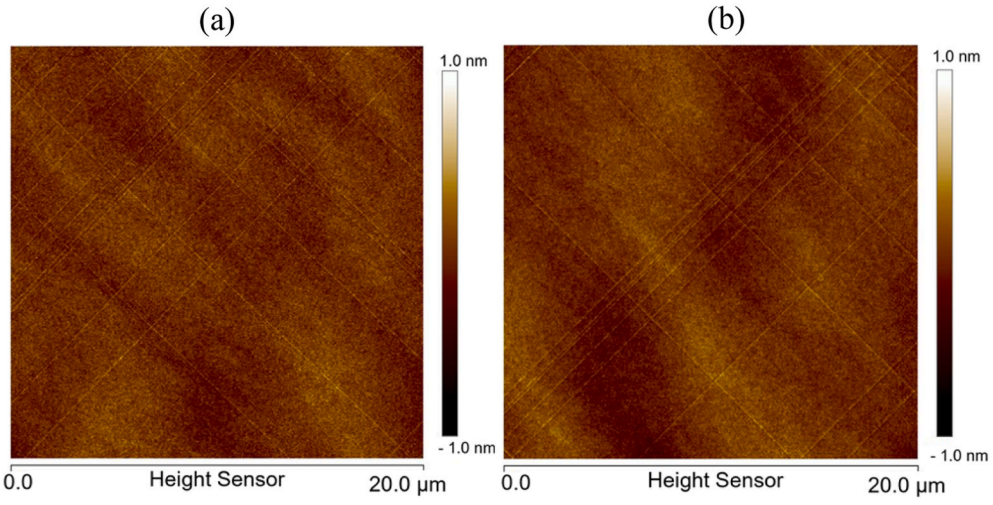

Fig. 16. $20 \times 20\,\mu m^2$ AFM images (a) after 20 nm thermal oxidation then oxide removal and (b) after a N_2 annealing without oxidation but with a thermal budget equivalent to that used for thermal oxidation revealing the presence of dislocation lines on the top SiGe (a) or Si (b) surface for the Si/SiGe stack grown on SOI. The sides of the AFM images are along the <100> directions.

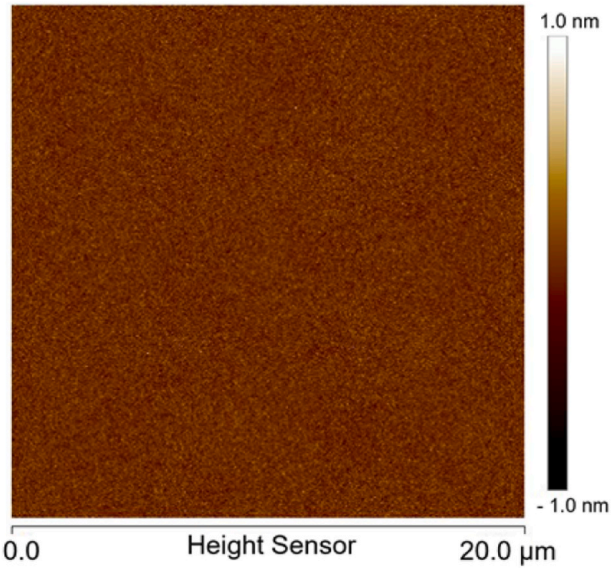

Fig. 17. $20 \times 20\,\mu m^2$ AFM image showing the lack of dislocation lines on the top SiGe surface when forming a 15 nm thick thermal oxide layer on a 4 periods (SiGe 25% 9 nm/Si 9 nm) superlattice grown on Si bulk. The sides of the AFM image are along the <100> directions.

different crystalline orientations for the PMOS component to fully exploit the unique potential of this wafer-to-wafer bonding approach [13]. This advancement represents a significant step forward in CFET technology, combining innovative fabrication techniques with precise thermal budget management to enable high-performance device fabrication.

CRediT authorship contribution statement

P. Tchoulfian: Formal analysis, Supervision, Writing – original draft, Writing – review & editing. **D. Barge:** Conceptualization, Formal analysis. **J.M. Hartmann:** Formal analysis, Resources, Writing – review & editing. **S. Kerdilès:** Resources. **V. Larrey:** Resources. **F. Fournel:** Resources, Writing – review & editing. **V. Loup:** Resources. **P. Hauchecorne:** Resources. **A.M. Papon:** Formal analysis, Writing – review & editing. **A. Thouvard:** Formal analysis, Writing – review & editing. **J. Richy:** Formal analysis, Writing – review & editing. **Y. Mazel:** Formal analysis. **N. Gauthier:** Formal analysis, Writing – review & editing. **A. Fraczkiewicz:** Formal analysis. **G. Pares:** Conceptualization, Supervision, Writing – review & editing. **D. Schippers:** Formal analysis. **U. Jain:** Formal analysis, Writing – review & editing. **S. Brems:** Formal analysis. **R. Loo:** Writing – review & editing. **B.T. Chan:** Supervision.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

Data will be made available on request.

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