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Recess metrology challenges for 3D device architectures in advanced technology nodes

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ABSTRACT

The introduction of new three-dimensional (3D) architectures in future logic and memory devices present new challenges for process metrology and control. Where there is a need to recess only one material type out of a superlattice (SL) layer stack, such structures all have in common the fact that the recess is hidden in the stack. Currently, process control in this field heavily relies on expensive, slow, and destructive metrology such as Transmission Electron Microscopy (TEM).

In this work, we use the high voltage Scanning Electron Microscope (SEM) technique in combination with the Elluminator® improved Back-Scattered electrons (BSE) technology for better imaging efficiency to demonstrate the ability to measure cavity recess from top-down SEM images.

We present case studies both in logic and memory domains. In Horizontal Gate-All-Around (H-GAA) Nanosheet and Forksheet logic devices, the SiGe layer is recessed in a Si/SiGe SL stack. In 3-Dimensional memory devices, we present results on Poly-Si recess metrology in Poly-Si/SiO_2 SL stack, Molybdenum (Mo) recess metrology in a Mo/aSi SL stack, and TiN recess metrology in a 3DSCM stack used for memory word line.

For the evaluation of the proposed recess metrology technique, several wafers with modulated recess amounts were measured using SEM technology at several high voltage landing energies (LE).

BSE signal and advanced image analysis algorithms were used to build a prediction model and quantify the recessed amounts using an edge-based analysis. TEM metrology was used to validate the measurement based on the top-down high LE SEM images.

We demonstrate that by using high voltage LE, in combination with enhanced BSE efficiency and advanced image analysis algorithms, we can investigate hidden layers in the stack, identify the recessed material edge, and measure accurately the cavities of interest, thus ultimately providing an inline, non-destructive, and statistically representative metrology solution for such advanced technology nodes.

This new application will help chip manufacturers to characterize their processes faster and provide an HVM monitoring and control solution.

Keywords: eBeam, back-scattered electrons, recess metrology, SEM, three-dimensional architecture, GAA, Nanosheet, Forksheet, NAND, SCM, memory

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1. INTRODUCTION

In recent years, we have seen an ever-increasing implementation of complex three-dimensional (3D) architectures for both logic and memory devices in the industry's advanced technology roadmaps [1]. Up to the 5nm technology node, Moore's law was mostly focusing on the 2D dimensional scaling. However, the scaling for new transistor structures at advanced technology nodes below 5 nm is now moving into the third dimension, to further support the standard cell size reduction by the fin depopulation approach.

We are now seeing more and more of these 3D complex structural innovations, such as Horizontal Gate-all-around (HGAA), Nanosheet and Forksheet FETs, and Complementary FET (CFET) aimed to enable further density scaling.

The memory roadmaps are also presenting an ever-increasing complexity due to the adoption of 3D architectures as in the case of 3DNAND [2] and 3D Storage Class Memory (SCM), looking for increased bit density and access time performance.

However, several challenges need to be addressed in the manufacturing flow of these novel 3D architectures, specifically in metrology and inspection.

The usual parameters monitored in a manufacturing flow (CD, LER/LWR, and surface defects), are not sufficient anymore to fully characterize the process when we face complex 3D structures (figure 1a). It becomes critical to measure and control what is hidden deep in the 3D structure. Parameters such as lateral recess, overlay in a multi-layer stack, buried defects, and material composition of the 3D stack become as important as the standard parameters (figure 1b), if not more.

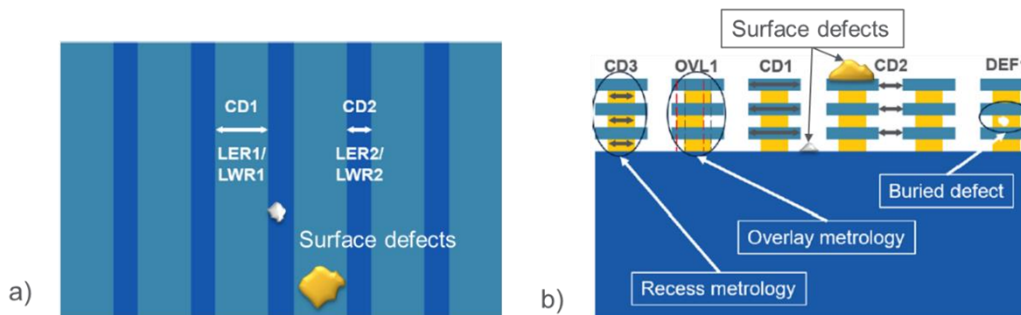

Figure 1. 3D structure like HGAA: a) Critical parameters usually measured from a top-down view; b) cross-section showing additional parameters of interest for 3D features.

2. METHODOLOGY

To address these challenges, we have used the technology that can enable the penetration of the 3D structures in the Z-axis namely the Scanning Electron Microscopy (SEM).

In an SEM instrument, we shine a primary electron beam onto the wafer. Secondary Electrons (SE) carrying the surface information are generated by the first tens of nanometers of the wafer, while Back-Scattered Electrons (BSE) carrying information on the deeper layers are emitted by the deeper part of the wafer.[3]

To properly characterize 3D architectures along the Z-axis direction, we need high BSE efficiency, as they carry information from the inner part of the structure.

To increase the efficiency of those back-scattered electrons, we have used high electron landing energies while utilizing the Elluminator® technology [4], which captures 95% of back-scattered electrons (BSE), thus enabling the "see-through" capability needed for the characterization of the hidden features of 3D architectures.

Figure 2 shows the comparison of the reference top-down SEM image collected at standard 600V landing energy (fig. 2a) vs the BSE SEM images collected at increasing higher landing energies (fig. 2b).

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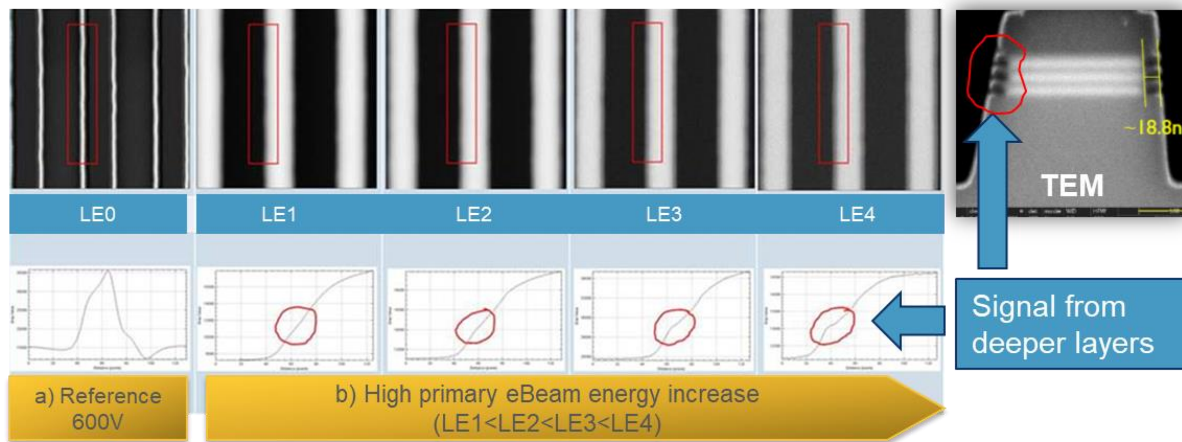

Figure 2. High LE BSE SEM: a) reference 600V LE top-down SEM image; b) High LE BSE SEM top-down images at increasing LE (LE1<LE2<LE3<LE4)

As observed in the grey level profile of the BSE signal, the higher the landing energy the stronger the signal coming from the region of the recessed layers.

The methodology used in this work starts from high LE BSE SEM imaging and analysis (supported by Monte Carlo simulations for optimal working point selection), defines the optimal metrology algorithm, measures the recess, and validates the results by TEM.

Advanced image analysis algorithms have been used to build a prediction model and quantify the recessed amounts using an edge-based analysis.

On top of this high resolution "see-through" capability, this approach has also the advantage of being fast, enabling massive data collection for better statistical analysis, being non-destructive, and providing an on-device measurement solution.

3. CASE STUDIES

Our focus is to measure the lateral recess of a specific layer in a complex material stack. We explore here various types of applications to assess the feasibility of the proposed approach.

In terms of logic, we study horizontal Gate-All-Around (GAA) Nanosheet and Forksheet structures in which the SiGe in the superlattice (SL) multilayer stack is recessed. Besides the challenge of "seeing through" the entire stack, we also investigated the impact of having the signal of interest buried under opaque layers. We specifically focused on lateral recess.

In terms of memory, we looked at Poly-Si recess in a Poly-Si/SiO_2 SL stack for 3DNAND, as well as Molybdenum metal recess in a Mo/aSi SL stack for 3DNAND application. In both cases, we also looked at the signal coming from long lines. Finally, we looked at a case where a tiny portion of TiN metal is recessed in word line metal for 3DSCM application.

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4. LOGIC 3D ARCHITECTURES

4.1 Horizontal Gate-All-Around (H-GAA) Nanosheet

HGAA devices are complex 3D architectures where, at some point in the flow, a source/drain isolation from the gate is needed by means of a dielectric inner spacer [5] (Figure 3a). One of the critical steps in the HGAA flow is to control the SiGe cavity recess, as this must be kept in a very narrow range of 5-10nm maximum [6] (Figure 3b).

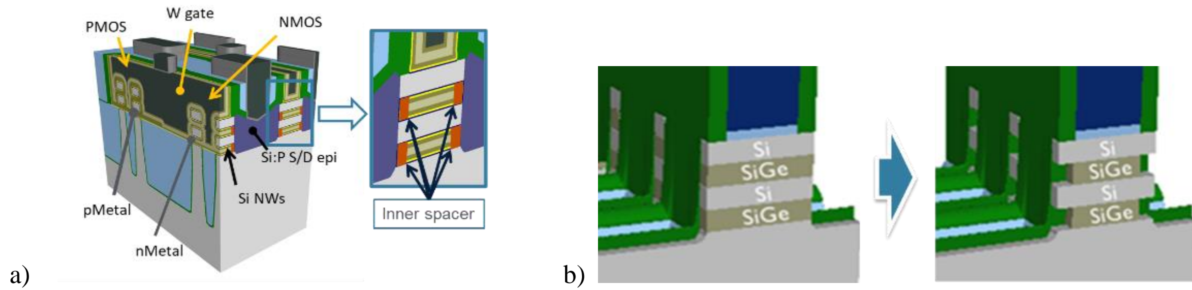

Figure 3. a) Horizontal Gate-All-Around (HGAA): 3D architecture and inner spacer isolation (Source: imec); b) Horizontal Gate-All-Around (HGAA): Inner cavity formation by SiGe layers lateral recess (Source: imec)

We inspected a set of samples covering a range of SiGe recess amounts from 0 nm (no recess) up to nominal 20 nm SiGe recess. (Figure 4a). The analysis focused only on the three central lines of a 5-Fin array area and then averaged the measured recess of the three central fins to provide a better statistic (Figure 4b).

We conducted experiments at several high landing energy values to optimize the SEM working point selection.

To evaluate the correlation with the SiGe cavity recess determined by TEM, we have compared the average SEM cavity recess with the average recess determined by TEM by measuring the individual cavities (Figure 4c).

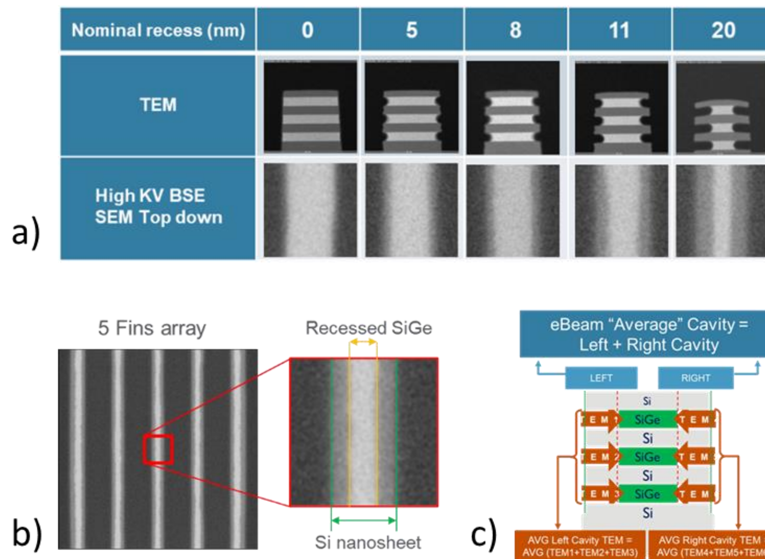

Figure 4. a) HGAA samples: SiGe recess amount range: 0-20 nm. Comparison between TEM and Top-down high LE BSE SEM image; b) 5-Fin array. Recessed SiGe and Si nanosheet CD measured; c) Cavity recess measurement validation by TEM: average SEM cavity recess vs average TEM cavity recess

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The first step in the process has been to tune the algorithm on a large recess amount range of ~17 nm.

The eBeam SiGe cavity recess metrology demonstrated a very good correlation with TEM results (Figure 5a). We then measured a single wafer at the target recess value to validate the algorithm and we correlated the measured average eBeam recess to the TEM on the same TEM location (Figure 5b).

A strong correlation (close to 1) has been obtained as well when measuring cavity recess below 8 nm, thus confirming the good performance of the eBeam high LE and high BSE efficiency detection approach to detect and measure SiGe cavity recess close to the target.

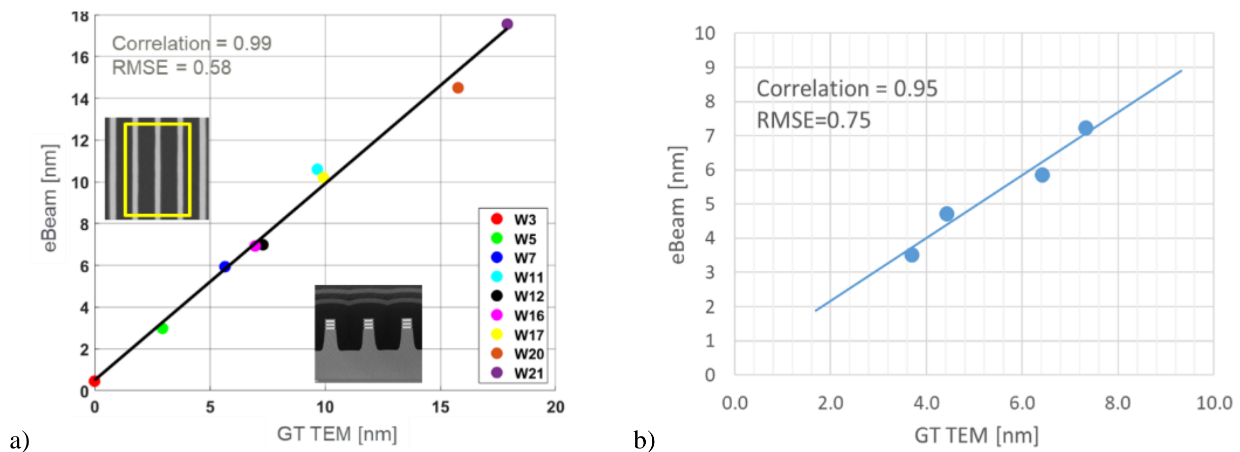

Figure 5. HGAA nanosheet cavity recess measurement: a) correlation graph between eBeam average cavity measurement and average TEM at large recess amount range; b) correlation graph on the target cavity recess amount

4.2 Horizontal Gate-All-Around (H-GAA) Forksheet

Forksheet is a GAA device designed to further enable dimensional scaling beyond the H-GAA nanosheet devices [7]. In this design, two nanosheet FETs, nFET and pFET, are close to each other on one device. A dielectric wall isolates the two regions (Figure 6a).

Even though such a test vehicle (in which the top SiGe layer is thicker than the others) is not representative of a real device stack, it is still an interesting case to validate our approach. Our interest is to extend the cavity recess metrology to an individual cavity sensitivity, especially when there is a non-uniformity in layer thickness and/or cavity recess at each individual layer in the SL stack.

We have inspected samples having several cavity recess depths at two different steps in the flow (hard mask (HM) is present or not on top of the SL stack). Our goal was to evaluate the capability of the proposed technique to "see-through" opaque materials such as the top hard mask (HM) layer. (Figure 6b). We then focused our analysis on the samples with HM as they are more challenging in terms of SiGe cavity recess determination.

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a) b)

Figure 6. HGAA Forksheet: a) test structure; b) Samples with and without HM at different cavity recess

Again, several landing energies have been tested to select the best imaging condition with the best signal-to-noise ratio (SNR) (Figure 7a). It is confirmed that the SiGe cavity recess signal is still visible on the Forksheet structures even in presence of the HM layer, as can be seen by the "knee" on the BSE GL profiles (Figure 7b).

Accurate measurements on several parameters like dielectric wall CD, SiGe + Wall CD, and Left/Right Recess have been performed for a comprehensive characterization of the Forksheet structure (Figure 7c).

a) b) c)

Figure 7. HGAA Forksheet: a) BSE images taken at two landing energies; b) BSE signal profiles showing a "knee" in correspondence of the SiGe recessed edge; c) CD parameters of cavity recess, dielectric wall, and dielectric wall + SiGe residual layer

As we highlighted before, this approach has the benefit to perform on-device measurement with high precision and accuracy providing fast local (within die) and global (across wafer) variation of the average cavity recess. In the specific case of the Forksheet samples, we have noticed an across wafer and within die variation of a similar order of magnitude, information which is otherwise not achievable by the limited TEM data sampling approach. (Figure 8). Measurement precision of <0.2 nm (3σ) has been achieved on this data set.

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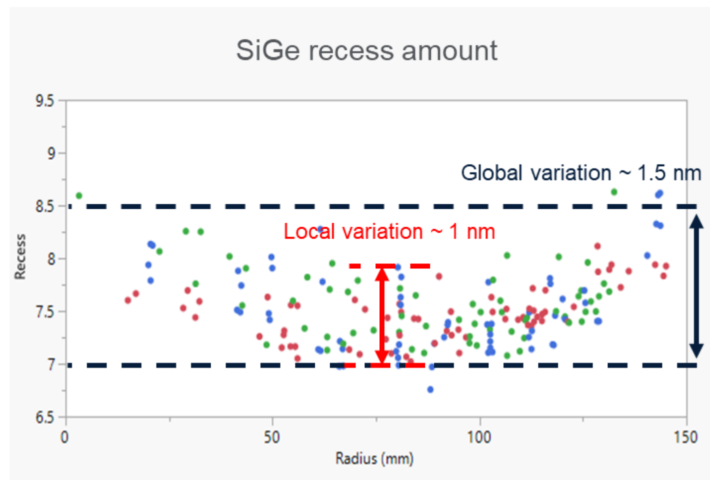

Figure 8. HGAA Forksheet: Wafer radius plot showing across the wafer and within the same die variation information

This is very important information when cavity recess is uniform across the several layers in the SL stack, hence the average cavity recess determined by the eBeam technique is representative of the recess at individual cavities and is sufficient for process monitoring and control.

However, when non-uniformity is observed across the Z-axis (among the different SiGe layers), this approach is limited, and a different way to determine the individual recess amount for each cavity is needed.

In the specific case of the Forksheet samples, we notice that the recess amount of the thicker top SiGe layer is higher compared to the mid and bottom SiGe layers (Figure 9a). Hence, in this case, the averaging of the individual layers is not an accurate measurement.

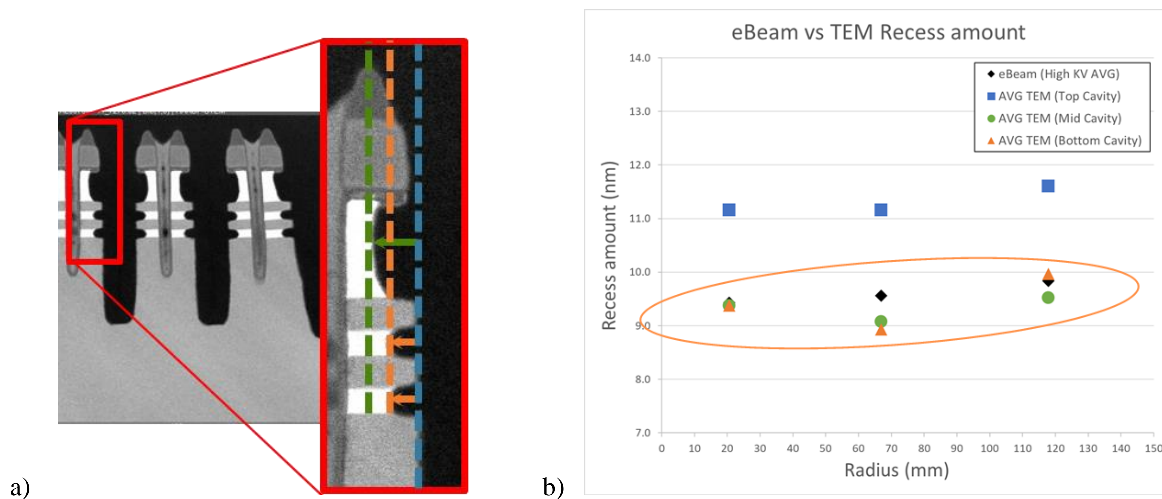

Figure 9. HGAA Forksheet: a) TEM cross-section showing the top SiGe layer recess (green) is higher compared to the mid and bottom layers (orange); b) HGAA Forksheet: Radial plot of individual cavities (TEM) vs eBeam average measurement.

In fact, the top SiGe layer signal is masked by the signal coming from the mid/bottom layers, being the eBeam measurement is based on a top-down image.

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If we discount the top layer contribution, the correlation with TEM is still confirmed. Figure 9b shows a radial plot of the measurement taken on the same Forksheet structure, across the wafer. It compares the TEM individual cavities vs the eBeam measurement, showing the good matching between mid/bottom TEM and eBeam measurements.

The results in Figure 9b validate the conclusion that multi-cavity average measurement is not the ultimate solution when it comes to characterizing through-depth cavity recess uniformity.

5. MEMORY 3D ARCHITECTURES

5.1 Poly-Si lateral recess in 3DNAND Memory

Moving to a different case study, we looked at a test sample relevant for 3D NAND and other memories.

In this case, the multi-layer stack is composed of 3 pairs of alternating PolySi and SiO_2 layers, where the PolySi is the recessed material (Figure 10a).

We define the "Line CD" as the CD of the oxide layers while the "Core CD" is the CD of the PolySi recessed layer (Figure 10b).

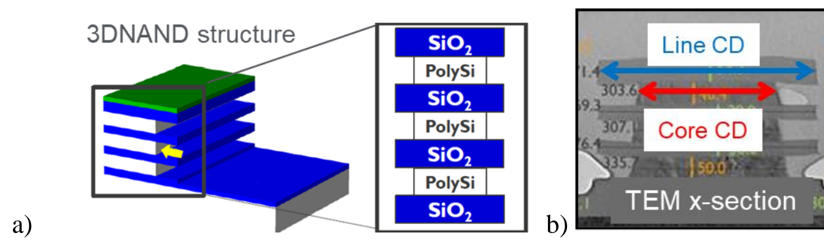

Figure 10. 3DNAND Memory. a) schematic of the 3DNAND test material; b) TEM cross-section (SiO2 layer = Line, PolySi layers = Core)

The selection of the best imaging condition and the appropriate LE for this stack was investigated by using Monte Carlo simulations, where the minimum LE required is the one capable to penetrate the full multilayer stack with marginal loss of primary electrons (Figure 11a). Moreover, the electronic yield of the two materials is so different that such a combination provides a very strong eBeam BSE contrast for the PolySi, as compared to the SiO_2 material (Figure 11b).

Due to the high SNR of the eBeam BSE signal for this material combination, there is a possibility to identify a core CD roughness information, at least qualitatively (Figure 11c).

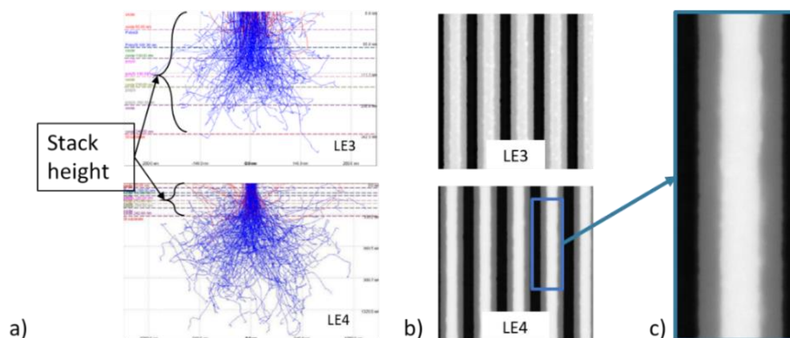

Figure 11. 3DNAND Memory. a) Monte Carlo simulations; b) BSE images at two landing energies; c) Zoom-in on Core CD roughness qualitative information

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The one side recess CD is determined by integrated arithmetic, subtracting the Core CD from the Line CD, and then dividing the total recess (both sides) by two (Figure 12a). The high SNR of both the Line and Core CD resulted in a recess CD having a precision of less than 1 nm (3sigma) and a good agreement with TEM data (Figure 12b).

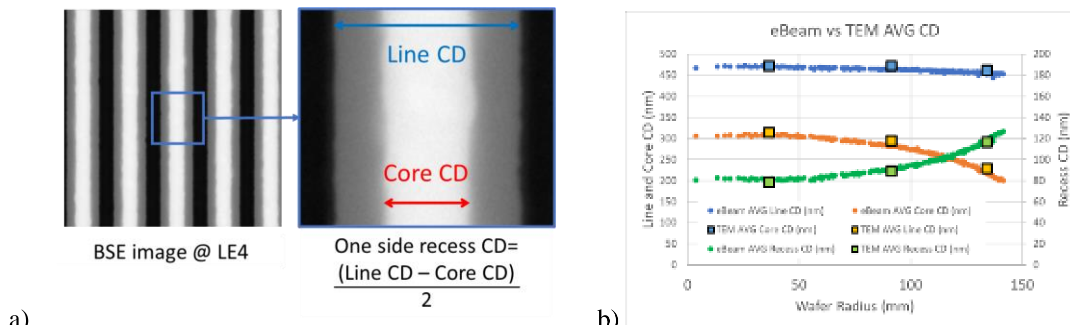

Figure 12. 3DNAND Memory. a) Recess amount by simple arithmetic; b) wafer radius plot of eBeam vs TEM recess amount

5.2 Molybdenum metal lateral recess in 3DNAND Memory

To further extend the evaluation of this technique across the different material selections, we have tested our approach also on another 3DNAND multi-layer stack which includes metal layers.

We have explored the case of Molybdenum recess in an amorphous Si/Molybdenum (aSi/Mo) multilayer stack.

In this specific case, each Mo metal layer in the multi-layer stack has a different thickness, with decreasing layer thickness as we move bottom-up in the stack (Figure 13). The a-Si layer thickness though remains constant for all layers.

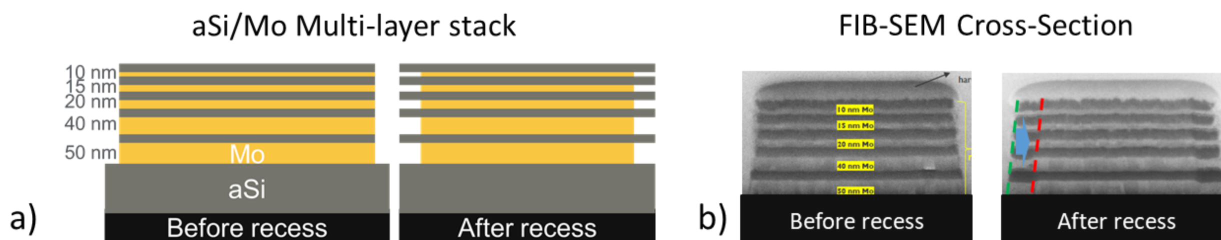

Figure 13. 3DNAND Memory. a) aSi/Mo multilayer stack schematic; b) FIB cross-section

In figure 14a, we show the comparison of the GL profiles for the SE and BSE signal images at three different LE (LE1<LE2<LE3).

We have used the SE signal to determine the a-Si edge, representing the outer CD. In addition, the BSE signal was used to determine the Mo edge, representing the inner CD (Figure 14b). We have then evaluated the impact of each LE on the SNR of the inner CD signal. As in the previous cases, the higher landing energy provides a sharper BSE Mo edge signal. As for the PolySi case, we can generate statistically relevant analysis by inline CD measurements. Good precision results (0.3 nm @ 3σ) were achieved thanks to the high yield of the metal layer (Figure 14c).

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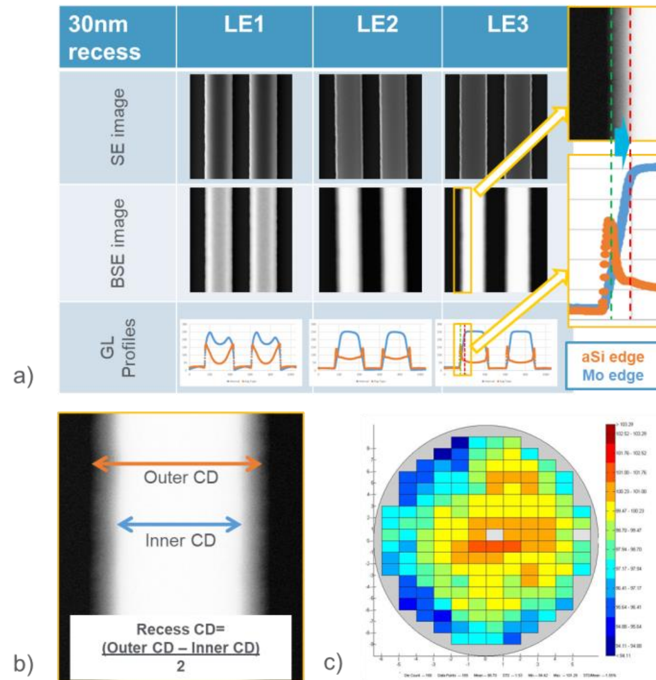

Figure 14. 3DNAND Memory. a) SE and BSE signal comparison; b) Recess CD definition; c) Recess amount full wafer map

As the SNR is high and so is the sensitivity to the metal layers, we were able to observe a non-uniformity of the metal recess through the multilayer stack along the recessed edge (Figure 15a). This non-uniformity, defined as the "shelving effect", has been later confirmed by the TEM analysis, where the TEM cross-section highlights a recess depth variation as a function of the Mo layer thickness (Figure 15b).

We can conclude then that the technique is indeed sensitive to across-stack recess depth variation, even though at present we cannot measure such non-uniformity.

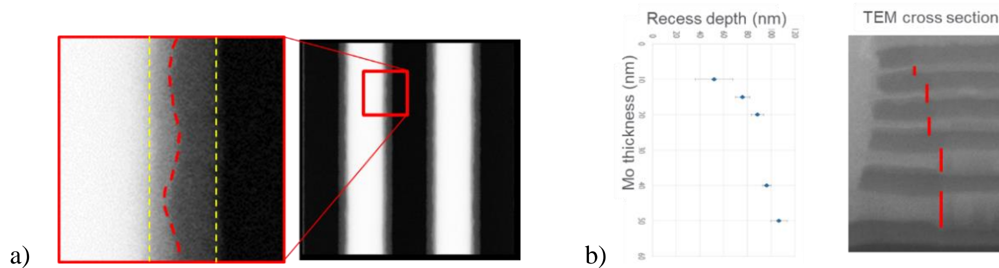

Figure 15. 3DNAND Memory. a) Mo layers "shelving effect"; b) Recess depth as a function of the Mo thickness. TEM cross-section showing the recess depth variability across the stack

5.3 TiN metal lateral recess in 3DSCM (Storage Class Memory)

We have tested the proposed approach in the case in which the recessed material is a metal layer, by looking at the TiN metal layer recess in 3D storage class memory. The recess of the TiN metal is more challenging from what we have seen so far, being confined in a small region (Figure 16a). Two different stacks have been tested with different materials and thicknesses to evaluate the impact of the materials/stack and thickness on the BSE signal (Figure 16b).

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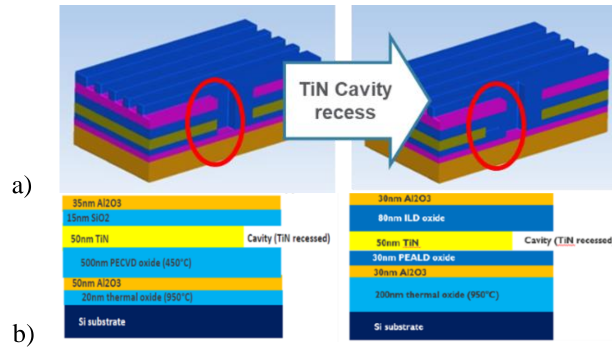

Figure 16. 3DSCM Memory. a) TiN cavity recess schematic; b) Material/stack samples selection

We looked at three different structures, having different densities of metal lines pattern and different surrounding environments (Figure 17a). As in previous cases, we have run experiments at three different LE to evaluate the SNR for each pattern density. The higher LE is again providing the best SNR and it has been selected for the analysis of the structures.

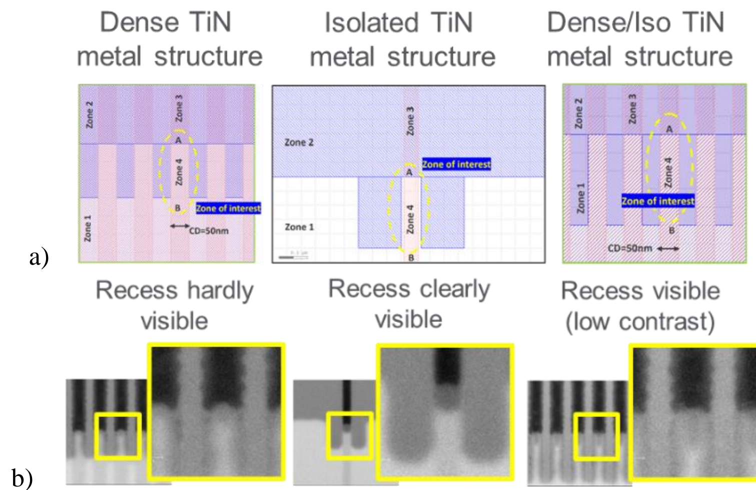

Figure 17. 3DSCM Memory. a) Three different structures with different pattern density; b) BSE image with different SNR response

Figure 17b shows the BSE images for the dense pattern structure (left), the iso pattern structure (center), and the dense/iso pattern structure (right).

On the dense pattern structure, the recess is hardly visible, probably due to the small amount of the TiN recess or to the surrounding environment, which might have an impact on the BSE yield of the recessed region. The recess in the dense/iso pattern structure is barely visible and the contrast is low, not sufficient for reliable recess metrology.

On the contrary, the iso pattern structure presents a clear signal of the TiN recess with a reasonable SNR, so we have focused on this structure for TiN recess analysis.

The impact of the material stack and thickness on top of the metal layer on the TiN recess signal is negligible when comparing the two different stacks and the corresponding GL profiles (Figure 18).

The stack below the metal layer though has an indirect negative impact on the evaluation of the cavity recess depth.

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Looking at the second stack, we observe a tapered profile which increases the mismatch between the cavity depth determined by TEM and the top-down eBeam measurement.

It is important then, when evaluating the process performance of the TiN recess, to notice the difference between the TEM-based recess evaluation and the high LE BSE eBeam-based measurement.

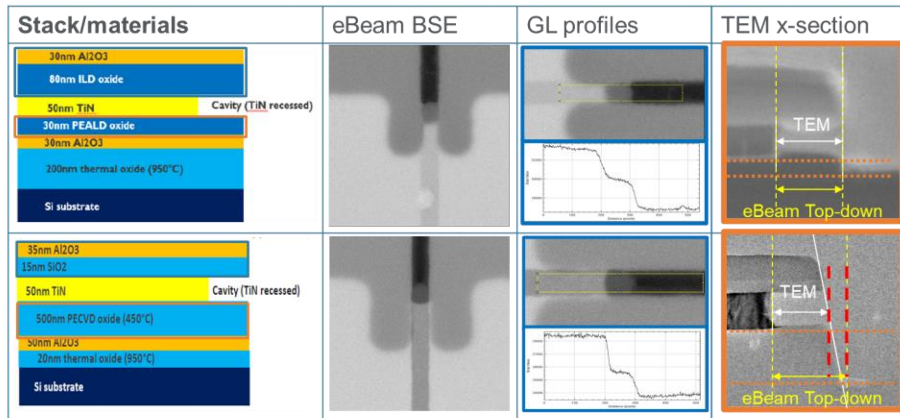

Figure 18. 3DSCM Memory. Two stacks comparison on BSE signal and impact on the eBeam vs TEM correlation

The definition of the recessed cavity dimension can be misled by the different reference edges from the top-down SEM and the TEM. Also, there is an extra complicating factor when it comes to the lack of straight fronts of the recess (Figure 19a). The recess amount will be different depending on where the TEM cut is performed. The eBeam approach does not suffer from this problem, as multiple cavity recess CDs can be measured on the same recess, providing additional information on the recess morphology (Figure 19b).

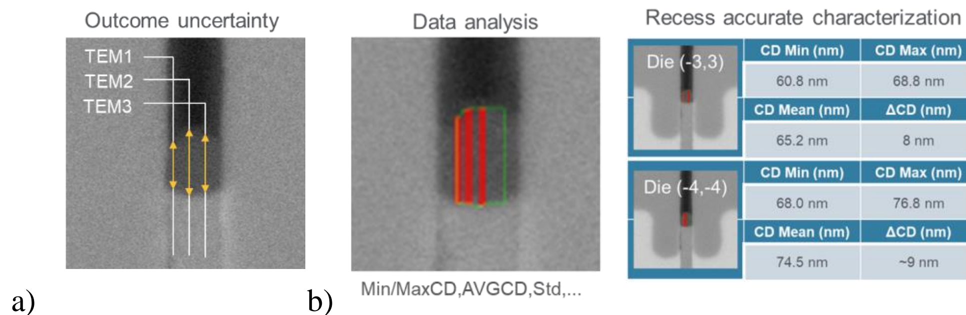

Figure 19. 3DSCM Memory. a) TEM outcome uncertainty due to irregular cavity recess one plane cross-section; b) eBeam full characterization through the accurate cavity measurements

6. CONCLUSIONS

As the industry is trending toward 3D architectures for multiple technologies, the critical parameters to be monitored and controlled are no longer those provided by top-down 2D metrology.

We investigated here high voltage SEM in combination with the Elluminator® technology which captures 95% of back-scattered electrons (BSE), thus enabling the “see-through” capability.

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We have presented several case studies both in logic and memory domains, where we have demonstrated good cavity recess metrology capability with good correlation to TEM (HGAA SiGe cavity recess) and good metrology precision < 1nm (3σ). In some cases, recessed CD line roughness resolution (PolySi and Mo in 3DNAND) could also be detected.

Such a technique can provide added value, thanks to its non-destructive, fast, and accurate performance.

The proposed approach is intended for application in HVM process monitoring and control, thanks to its high throughput, statistically representative data set, and on-device measurement capability.

Last, we have identified limitations when it comes to the multi-cavity average measurement, and we acknowledge that work still needs to be done to achieve a proper solution for individual cavity recess metrology.

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