A Compact Current-Reusing 6-mW 66–92 GHz Frequency Quadrupler With 5% Peak Power Added Efficiency and >36 dBc Harmonic Rejection in 22-nm FDSOI CMOS

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***Abstract*—This letter presents a frequency quadrupler with 32% fractional bandwidth (66–92 GHz) and 5% peak power-added efficiency (PAE), capable of operating with an input power of 0 dBm. The quadrupler consisting of two cascaded frequency doublers uses a multiport driven push-push complementary architecture for the first stage to generate differential signals for the second doubler with high fundamental harmonic rejection. The second doubler based on the nMOS-based push-push architecture uses gain enhancement to achieve a maximum conversion gain of –4 dB for the quadrupler. The quadrupler with an output saturation power (P_{sat}) of –2.6 dBm achieves first- to third-harmonic rejections of more than 36 dBc across the 3-dB bandwidth. The compact quadrupler has a core area of 0.09 mm^2, while consuming a DC power of 6.2 mW from a 0.8 V supply with an input power of 0 dBm at 20 GHz.**

***Index Terms*—CMOS, complementary, doublers, frequency multipliers, high efficiency, high-fractional bandwidth, high-harmonic rejection, LO generation, mm-wave, multiport doubler, push-push, quadruplers.**

I. Introduction

High-data rate systems for communication and sensing in the mm-wave bands need local oscillator signals with good output power, power-added efficiency (PAE), and bandwidth. Voltage-controlled oscillators (VCOs) with wide tuning ranges typically suffer from high-phase noise. Thus, VCOs followed by frequency multipliers are a common way to synthesize high-frequency signals.

Furthermore, frequency multipliers capable of operating with low-input power provide integration with the low-frequency signal generator without the need to use intermediate power-hungry power amplifiers (PAs). However, there are tradeoffs between conversion gain, fractional bandwidth, power efficiency, and harmonic rejection. To achieve a high-fractional bandwidth, [1] uses multiturn transformers with cascaded push-pull cascode stages. However, the bandwidth may not be sufficient for some applications, such as down-conversion of D-band RF signals with wide channel spacing to a fixed intermediate frequency (IF). To achieve a high power efficiency, [2] generates the first and third-harmonics (THRs) with phase and amplitude control and then uses a square law mixer to generate the fourth harmonic. The architecture results in a high-undesired THR power at the output, while also requiring a high-input power of 13 dBm. To achieve a compact design, [3] uses a phase-controlled push-push quadrupler, but the input power required is 9 dBm. The architecture also suffers from a low-conversion gain. To achieve a high conversion gain and harmonic rejection, [4] generates In-phase and Quadrature signals for both doublers generating fully differential signals. However, the fractional bandwidth is low. To increase the conversion gain, [5] uses cascode with inductive peaking. The design needs a high-supply voltage, and has low power-efficiency. To achieve high power efficiency, [6] uses a complementary MOS-based design, but the passive elements and the need to balance the amplitude limit the 3-dB bandwidth to only 5%.

In this work, a frequency quadrupler with high PAE, high-harmonic rejection, and the ability to operate with low-input power is demonstrated. The quadrupler consists of two cascaded frequency doublers. The first doubler uses a complementary multiport driven push-push stage to achieve quadrupler operation with low-input power, while also achieving high-fundamental harmonic rejection and low input resistance. The second doubler is a conventional nMOS-only push-push stage with gain enhancement, to achieve a high conversion gain and PAE for the quadrupler. The impedance matching between the doublers is designed to obtain a high fractional bandwidth. The design details and measurement results are provided in Sections II and III, respectively.

II. Circuit Implementation

The architecture of the proposed frequency quadrupler is shown in Fig. 1(a). The frequency quadrupler in Fig. 1(a) uses a combination of pMOS multiport (MP pMOS) and nMOS multiport (MP nMOS) driven stages for the first doubler. The second frequency doubler (FD2) is based on a conventional nMOS-based push-push architecture. The design of the first doubler is described in detail in the following section, followed by design of the interstage matching, the second doubler, and overall performance of the quadrupler.

A. First Doubler

The first doubler should be able to generate large output voltage swings at $2f_0$ with the desired input power, while achieving good fundamental harmonic rejection, input matching, and PAE. There are a few popular doubler architectures that satisfy the above criteria. The most common type of frequency doubler is the conventional push-push doubler (Conv. PP), shown in Fig. 1(b). Although the topology has a high conversion gain, the input matching of 50 Ω to the high gate impedance of the doubler results in a high insertion loss. MP nMOS architecture [7], shown in Fig. 1(c), is driven differentially at the gate and source and therefore has a low input real impedance that can be matched to 50 Ω with low insertion loss. However, the power gain is low. Furthermore, MP pMOS and MP nMOS stages can be combined to give a MP CMOS doubler, as shown in Fig. 1(a). The three architectures are compared with respect to conversion gain, harmonic rejection, and PAE for an input power of 0 dBm.

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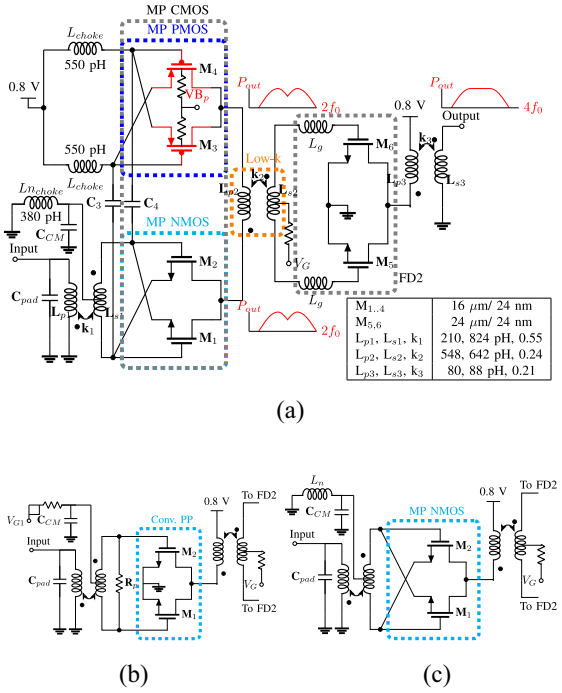


Fig. 1. (a) Circuit diagram of proposed MP CMOS-based frequency quadrupler. (b) Conventional PP frequency doubler. (c) MP nMOS frequency doubler.

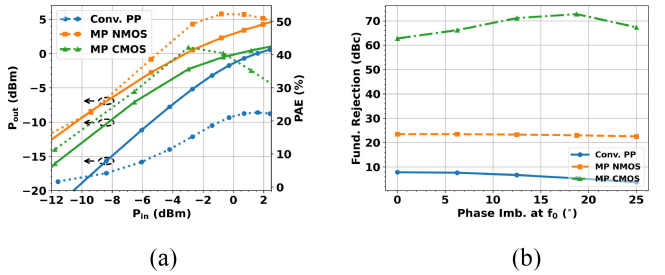


Fig. 2. (a) Output power (P_{out}) and the PAE at 40 GHz with sweep of input power, P_{in} at 20 GHz with ideal input and output match. (b) Output power at fundamental frequency (f_0) for a differential amplitude imbalance of 3 dB with sweep of phase imbalance at f_0.

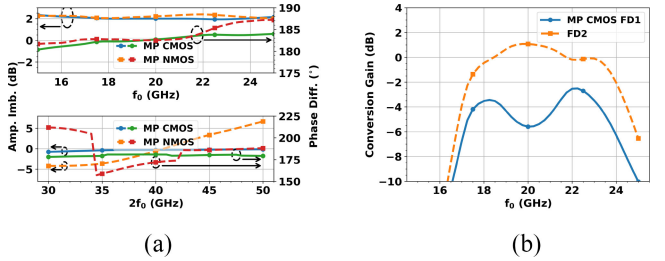


Fig. 3. (a) Differential input and output amplitude ratios and corresponding phase differences for the quadruplers with MP nMOS (dashed lines) and MP CMOS (continuous lines), (b) Conversion gain of the first doubler showing peaks at the edges of the bandwidth. The conversion gain of the second doubler (axis referred to f_0) is also added to illustrate the bandwidth enhancement technique for the quadrupler. The "FD2" conversion gain includes the loss of the interstage and output matching network.

For a fair comparison, the real part of the input impedance of the Conv. PP doubler is kept the same as MP nMOS doubler (290 Ω) by loading the differential gates with a shunt resistor (R_p) to make the insertion loss of the input matching irrelevant to the comparison. The Conv. PP nMOS transistors are biased for maximum PAE. The optimum load impedance for the best gain is obtained by running a loadpull-analysis. To obtain a good bandwidth at the output, the load impedance is chosen on the Q = 3 contour with the best gain. All architectures achieve near-rail-to-rail voltage swings with 0 dBm input power. The power gain and PAE with an ideal input and output match are compared for the different doubler types, as shown in Fig. 2(a). The gain and the PAE of the multiport architectures are higher than those of the Conv. PP doubler, due to differential swings at gate and source and Class-C operation. The MP nMOS architecture gives the best conversion gain and power efficiency. However, the MP CMOS doubler has the ability to generate differential signals without using a single-to-differential interstage transformer. Such a transformer typically produces a phase and amplitude imbalance in the differential outputs, which could produce undesired harmonics at the quadrupler output. A harmonic filter solves the problem, but lowers the bandwidth.

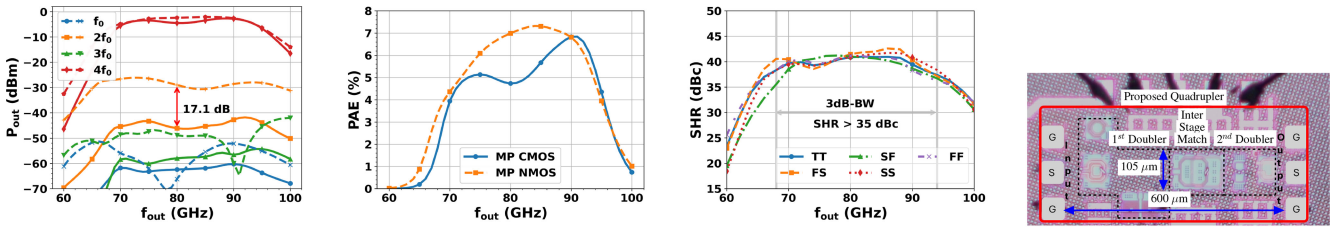
Furthermore, the conversion gain of the multiport architecture is resilient to phase and amplitude mismatch in the differential inputs. Fig. 2(b) shows the relative power rejection of f_0 at the output when the input amplitude mismatch is 3 dB and the phase difference is varied. MP CMOS doubler achieves the highest f_0 rejection due to the differential nature of the outputs, resulting in a low $3f_0$ power at the quadrupler output, which arises from the mixing of f_0 with $4f_0$ harmonic at the output.

The proposed architecture consists of MP nMOS and MP pMOS doublers connected through the primary winding of the interstage transformer to reuse the current for good power efficiency as shown in Fig. 1(a). The sizes of the transistors are chosen to generate enough swings at $2f_0$ to saturate the second doubler with 0 dBm input power. The gate length of the transistors is higher than the minimum for the technology for the best PAE, given the input power. The gate biases for nMOS and pMOS are kept at 0 V and 0.8 V, respectively, to obtain high power efficiency by operating in Class-C. In the FD-SOI process, the body bias of the flip-well transistors can be chosen to get the best performance. The gain of the first doubler improves by 0.7 dB when VB_p is changed from 0.8 V to 0 V by decreasing the threshold of the pMOS transistors without affecting the bandwidth.

In a typical frequency doubler, the second harmonic feedback from the drain to gate of the transistor causes a decrease in the conversion gain [1]. It is typically solved by having a filter at the center tap of the input transformer at the second harmonic [7]. In the proposed quadrupler, the sizes of pMOS and nMOS in the first doubler are kept the same to cancel the second-harmonic feedback from the output to the input. Thus, the center tap of the input transformer can be used to obtain good amplitude and phase matching at f_0 by connecting to a capacitor (C_{CM}). The amplitude error and phase difference of the inputs are well controlled in both the quadruplers as shown in Fig. 3(a). Fig. 3(a) also shows the phase and amplitude imbalance at the outputs of the MP doublers. The MP CMOS doubler shows very little imbalance in the phase and amplitude at $2f_0$ when the sizes of nMOS and pMOS transistors are the same, compared to the MP nMOS doubler. Thus, the MP CMOS-based quadrupler achieves a higher $2f_0$ rejection at the quadrupler output.

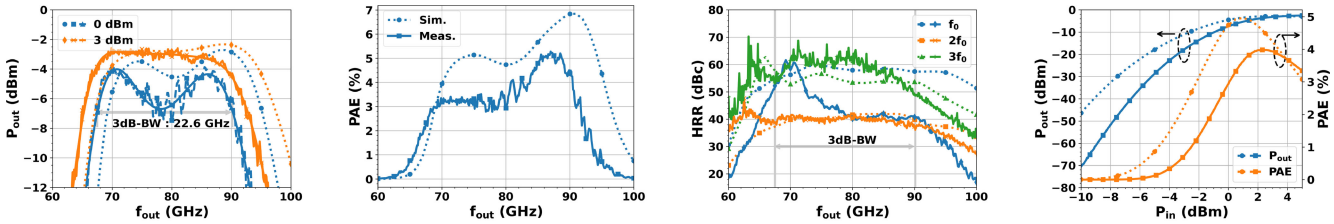
B. Quadrupler Design and Performance

The interstage matching between the doublers is chosen to obtain a higher gain at the edges of the frequency band compared to the center frequency as shown in Fig. 3(b) using a low-k (0.24) transformer [8] and the load-pull data of the first doubler. The conversion gain of the second doubler with output matching, can then focus on increasing



(a) (b) (c) (d)

Fig. 4. (a) Output harmonic powers comparison for quadruplers with MP nMOS first doubler (dashed lines) and MP CMOS first doubler (continuous lines). (b) PAE comparison for the two architectures. (c) Simulated SHR of MP CMOS quadrupler across corners. (d) Chip Micrograph.



(a) (b) (c) (d)

Fig. 5. (a) Measured output fourth-harmonic power, along with the fitted and the simulation results with sweep of frequency when input power is 0 dBm and 3 dBm. (b) PAE with sweep of frequency when input power is 0 dBm. (c) Harmonic power rejection with sweep of frequency when input power is 0 dBm. (d) Fourth harmonic power and PAE at 80 GHz with sweep of the input power. Solid line: Measured, Dotted line: Simulation results.

the gain at the center frequency. Thus, a good 3-dB bandwidth for the frequency quadrupler is achieved.

The second doubler based on a conventional nMOS-based push-push architecture, gives a good conversion gain. The sizes and gate bias of the transistors are chosen for the best PAE when the first doubler gets an input power of 0 dBm at f_0. A gate inductor (L_g) of 55 pH is used to further enhance the conversion gain at the center frequency by 1.4 dB, while maintaining good bandwidth. The inductor boosts the V_{gs} swing at $2f_0$ through inductive-peaking by resonating with C_{gs}. A higher value of the inductor decreases the conversion gain by boosting the common-mode feedback signal through C_{gd} at $4f_0$, which generates an out-of-phase drain current.

The output harmonic powers and the PAE of the proposed MP CMOS-based frequency quadrupler are shown in Fig. 4, and compared with the MP nMOS-based quadrupler to highlight the advantages of the architecture. The output power at $4f_0$, and the PAE are slightly better for the MP nMOS-based quadrupler. However, both architectures achieve 5% PAE. The DC power consumption with an input power of 0 dBm at 20 GHz is 7.5 mW. The first doubler consumes 1.1 mW, while the second doubler consumes 6.4 mW. The 3-dB fractional bandwidth of the MP nMOS-based quadrupler is 31% compared to 33% for the MP CMOS-based quadrupler. Both architectures achieve $3f_0$ and f_0 rejections better than 45 dBc. But the $2f_0$ power rejection is at least 12 dB better for the MP CMOS-based quadrupler across the 3-dB bandwidth, due to the balanced outputs of the first doubler. Thus, the MP CMOS-based quadrupler is superior in harmonic rejection while achieving good conversion gain and PAE. Furthermore, Fig. 4(c) shows that the $2f_0$ power rejection across process corners is greater than 35 dBc. The measurement results for the MP CMOS-based quadrupler are presented in Section III.

III. Measurements

The chip micrograph of Fig. 4(d) shows the proposed quadrupler fabricated in a 22-nm CMOS FDSOI process. The chip size is 1 mm^2 with a core area of 0.09 mm^2 excluding the pads. The frequency quadrupler is characterized using Keysight PNA-X network analyzer, N5247B and Keysight frequency extenders, N5293AX03. The harmonic powers and DC power consumptions are measured across frequency with a sweep of input power at f_0.

Fig. 5(a) shows the $4f_0$ power with a sweep of the input frequency when the input powers are 0 dBm and 3 dBm. A peak gain of –4 dB at the edges of the frequency band is observed, showing the effects of bandwidth enhancement due to interstage matching. A lower gain is observed compared to the simulations, possibly due to the lower gain of the first doubler biased in Class C, which has also resulted in a higher in-band ripple of +/–1.3 dB for the input power of 0 dBm. With a higher input power, the ripple disappears as the second doubler goes into saturation. The measured 3-dB bandwidth with an input power of 0 dBm is 22.6 GHz, a fractional bandwidth of 28.6%. The 3-dB BW is 26.4 GHz (33%) when the output power is saturated. Fig. 5(b) shows that the PAE reaches a peak of 5% for the input power of 0 dBm at 86 GHz. Fig. 5(c) shows the rejection of unwanted harmonics. The quadrupler shows a second-harmonic rejection (SHR) of greater than 36 dBc across the wide bandwidth, thanks to the differential nature of the outputs of the first doubler. The first-(FRR) and THR rejections are greater than 39 dBc and 46 dBc, respectively. The measured DC power consumption with 0-dBm input power at the center frequency is 6.2 mW, and varies between 3.3 mW and 11.4 mW in the 3-dB bandwidth. Fig. 5(d) shows the fourth-harmonic power and the PAE with a sweep of the input power at 80 GHz. The PAE peaks at 4% when the input power is 2.4 dBm at 80 GHz. The measured output saturation power is –2.6 dBm.

Table I compares the proposed frequency quadrupler with the state-of-the-art. This work achieves a similar PAE compared to [1], while also achieving a higher bandwidth. Compared to [2], a work with higher power efficiency and bandwidth, the harmonic rejection in this work is better than 36 dBc for all the lower harmonics. Furthermore, this work works with a low-input power of 0 dBm and consumes low DC power. Compared to [3], a work with similar power consumption and area, this work achieves better gain, bandwidth,

TABLE I
PERFORMANCE COMPARISON OF FREQUENCY QUADRUPLERS

Ref	This work	[1]	[2]	[3]	[4]
Frequency† (GHz)	**65.6-92**	70-86	62-92	66-75	71-81
3dB-BW†(%)	**33**	21	39	13	13
Technology	**22-nm FD-SOI**	28-nm CMOS	40-nm CMOS	40-nm CMOS	22-nm FDSOI
Topology	**Multi-port CMOS PP + PP**	x4 push-push	Odd harm recycling	Phase controlled PP	Bal. push-push
Peak P_{out}@P_{in} (dBm)	**-4@0**	-3@0	11@13	-0.2@9	3.1@0
Peak CG (dB)	**-4**	-3	-2	-9.2	3.1
VDD (V)	**0.8**	1	0.9	-	0.8
PDC (mW)	**6.2**[1]	20	101	11	70
FRR (dBc)	**>39**	60	45	45	35
SHR (dBc)	**>36**	40	45	30	35
THR (dBc)	**>46**	-	26	-	-
Peak η[2](%)	**5.2**	5	10	5 (2.5[*])	2.9
Area (mm^2)	**0.09**	0.03	0.26	0.1	0.38

† At saturation.
[1] At center frequency, 0 dBm input power.
[2] $\eta = P_{out}/(P_{in}+P_{DC})$.
[*] Without buffer.

and SHR. Compared to [4] which achieves a higher gain, the proposed design has higher bandwidth, compact area, and peak power efficiency.

IV. CONCLUSION

A compact frequency quadrupler with low-DC power consumption, wide fractional bandwidth, and the ability to operate with 0-dBm input power in the E-band was presented. This work employs a CMOS-based multiport driven frequency doubler, in conjunction with bandwidth enhancement techniques to achieve a high PAE (5.2% peak), harmonic rejection (>36 dBc), and fractional bandwidth (28.6%) without using buffers or explicit harmonic filters. Thus, the techniques presented in this work can enable power-efficient fourth-harmonic generation for low-power E-band mm-wave systems.

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REFERENCES

[1] P. Ricco, G. Avitabile, and D. Manstretta, "A compact 70–86 GHz bandwidth frequency quadrupler with transformer-based harmonic reflectors in 28nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, 2023, pp. 169–172, doi: 10.1109/RFIC54547.2023.10186198.

[2] Z. Lin, Y. Shen, Y. Ding, and S. Hu, "19.2 A 12.4% Efficiency, 11dBm Psat, Odd-harmonics-recycling, 62-to-92GHz CMOS frequency quadrupler using an amplitude-phase coordinating technique," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2024, pp. 350–352, doi: 10.1109/ISSCC49657.2024.10454527.

[3] K. Lee, K. Kim, G. Shin, and H.-J. Song, "65.6–75.2-GHz phase-controlled push–push frequency quadrupler with 8.3% DC-to-RF efficiency in 40-nm CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 6, pp. 579–582, Jun. 2021, doi: 10.1109/LMWC.2021.3068179.

[4] S. Vehring, Y. Ding, P. Scholz, and F. Gerfers, "A 3.1-dBm E-Band Truly Balanced Frequency quadrupler in 22-nm FDSOI CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 12, pp. 1165–1168, Dec. 2020, doi: 10.1109/LMWC.2020.3028053.

[5] Z. Sun, H.-Y. Li, J.-X. Xu, L. Gao, and X. Y. Zhang, "A 52–65 GHz frequency quadrupler with low conversion loss and high harmonic rejection ratio in 28-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 8, pp. 2784–2788, Aug. 2023, doi: 10.1109/TCSII.2023.3245653.

[6] J. Yoo and S. Hong, "Highly efficient differential frequency doubler with output resistance boosting feedback," *IEEE J. Solid-State Circuits*, vol. 59, no. 2, pp. 414–423, Feb. 2024, doi: 10.1109/JSSC.2023.3289512.

[7] S. Li, T. Chi, T.-Y. Huang, M.-Y. Huang, D. Jung, and H. Wang, "A bufferless wideband frequency doubler in 45-nm CMOS-SOI with transistor multiport waveform shaping achieving 25% drain efficiency and 46–89 GHzinstantaneous bandwidth," *IEEE Solid-State Circuits Lett.*, vol. 2, pp. 25–28, 2019, doi: 10.1109/LSSC.2019.2918943.

[8] M. Vigilante and P. Reynaert, "On the design of wideband transformer-based fourth order matching networks for *E* -band receivers in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2071–2082, Aug. 2017, doi: 10.1109/JSSC.2017.2690864.