A 56 Gb/s Zero-IF D-Band Beamforming Transmitter in 22 nm FD-SOI

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***Abstract*—This article presents a 4-way transmitter (TX) array suitable for beamforming operation at D-band. The transmitter is implemented using zero-IF architecture with LO beamforming. The signal path comprises an I/Q baseband (BB) section, direct up-conversion, and a power amplifier chain, supporting a wideband operation from 118 to 147 GHz. A 5-stage 2-way power amplifier chain provides a saturation output power up to 11 dBm. The probing measurement results demonstrate up to 64 quadrature amplitude modulation (64QAM) [30 Gb/s at −25 dB rms-error vector magnitude (EVM)] and achieve a data rate of 56 Gb/s with a −17 dB rms-EVM at an output power of 3 dBm using 16QAM modulation. The LO chain contains a 14–16 GHz buffer, a cascade of two frequency triplers for LO generation at D-band using an external LO reference. A tunable matching network with 6-bit capacitor-band control is implemented in the buffer stage together with a polarity switch to achieve full range phase control. An efficient I/Q generation scheme is implemented by exploiting the last tripler before the I/Q mixer: two *LC* buffers after 1st tripler generates ±15° phase offset. This results into ±45° phase offset after the 2nd tripler. The benefits of our sub-harmonic I/Q generation are: 1) no I/Q hybrid operating in D-Band is needed; 2) the limited ±15° phase offset required allows an easy *LC* tuned buffer implementation with limited amplitude variation across phase range; and 3) this amplitude variation is removed by 2nd tripler and LO buffers that operate at saturation level. This LO beamforming scheme ensures a phase resolution of 0.1° in measurement. A single TX channel draws 232 mW from a 0.8 V supply and has an area of 1.17 × 0.3 mm² in a 22 nm fully depleted silicon on insulator (FD-SOI) process. The 4-way beamformer IC has been flip-chip mounted on a low-cost 10-layer printed circuit board (PCB) and connected to a planar antenna array integrated at the backside of the PCB. The antennas are placed with 1.1 mm spacing and each antenna contains 4 aperture-coupled patch units to enhance the radiation pattern. The 4-way TX beamformer has been tested over-the-air (OTA) with a reference receiver achieving 24 Gb/s with −25 dB rms-EVM at 0.4 m distance using 5G NR waveforms.**

***Index Terms*—Antenna array, beamforming, CMOS, D-band, error vector magnitude (EVM), fully depleted silicon on insulator (FD-SOI), flip-chip, high-speed, packaging, quadrature amplitude modulation (QAM), radiation, transmitter, wireless communication, wideband, zero-IF.**

Received 16 July 2025; accepted 17 September 2025. This article is an expanded version from the IEEE Symposium on Radio Frequency Integrated Circuits (RFIC), Washington DC, USA, June 2024. *(Corresponding author: Yang Zhang.)*

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Digital Object Identifier 10.1109/TMTT.2025.3613831

I. Introduction

SYSTEMS operating above 100 GHz can enable >100 Gb/s data rates wireless link [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20] and D-band (110–170 GHz) spectrum offers the necessary wideband. For such systems, the need to fit the system into a space compatible with the wavelength (2.2 mm for 140-GHz operation) can be more easily addressed with the advanced integration level offered by advanced CMOS technologies [6], [13]. The most important challenges of circuit operation in the D-Band are path loss and limited transistor performance [21], [22], [23], [24]. Both issues can be relieved with beamforming: by adding more elements, the equivalent antenna gain is increased at the expense of beamwidth. The equivalent antenna beam pattern is steered in the desired direction by controlling the phase of the different antenna elements. This can be done in the digital or analog domain.

RF beamforming is a widely used architecture in mm-wave frequencies: all signals are phase shifted at RF after a unique up-conversion. However, RF beamforming has its own challenges as far as RF phase shifter (PS) implementation. In fact, if passive, the PS comes with loss and limited granularity and if active, it comes with complexity and trade-offs since it contributes to signal path integrity as far as noise, linearity, and bandwidth. These issues make it challenging to maintain at the same time wide bandwidth operation and fine granularity in phase control. Most D-band beamformers support less than 10 GHz RF bandwidth [6], [9], [19] and [25] demonstrates a wideband beamforming frontend that does not integrate the up/down converter but with a power consumption higher than similar work. A 135–145 GHz RF PS is presented in [26], with excellent gain and phase error performance, unfortunately with a bandwidth requiring to be extended for flexible channel selection within the full D-band. The work reported in [27] demonstrates 0.1° phase step control from 150 to 160 GHz, but the linearity is limited. Digital beamforming is the most flexible option and offers the highest possible signal bandwidth thanks to the absence of PS in signal path and with a phase control granularity limited only by digital implementation. However, silicon area and power consumption are increased

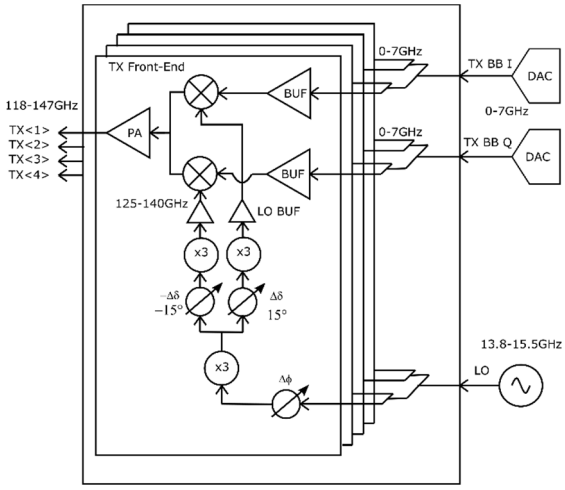


Fig. 1. Architecture of the D-band beamforming transmitter.

due to the duplication of the entire radio, including the digital section and this makes full 2-D scalability difficult [7].

In LO beamforming, the phase control is in the LO chain. The absence of PS in signal path makes it easier to achieve a wider signal bandwidth and avoids all difficulties associated with preserving signal-to-noise ratio in signal path. Additionally, the phase control in the LO chain can be implemented with high granularity and generally in a simpler way versus RF beamforming since LO signal path work at compression. In this work, we propose a TX architecture that solves some of the shortcomings associated with LO beamforming and allows easier implementation, see Fig. 1. This article is an expanded version from [7]. The TX presented here is one antenna path of a 4-way transceiver (TRX) chip. The TX is sized for operation with at least 5 GHz of RF bandwidth in any frequency range between 120 and 145 GHz with 64 quadrature amplitude modulation (64QAM) capability. The TX can operate also with 16QAM modulation in a 14 GHz bandwidth with a rms error vector magnitude (EVM) better than −17 dB, reaching a data rate of 56 Gb/s at a TX power of 3 dBm. The full 4-way TX beamformer has been packaged in a module with antenna and over-the-air (OTA) measurements will be also reported.

This article is organized as follows. Section II presents system-level design considerations of D-band beamforming systems. The design details of the transmitter are given in Section III. Section IV deals with the packaging and antenna array design. Measurement results of the probing and OTA tests for the full IC are provided in Section V. Finally, Section VI concludes this article.

II. Architecture

A. ZIF Architecture and LO Beamforming

The chosen architecture is zero-IF for its inherent advantages: reduced number of blocks on the signal path with associated larger bandwidth and easier trade-off noise and linearity.

Beamforming uses N_{TX} elements with P_{OUT} power to increase equivalent isotropic radiation (EIRP)

$$\text{EIRP} = N_{TX}^2 \cdot P_{OUT}. \quad (1)$$

The beam is steered in the desired direction by controlling the phase shift between elements in the signal path at RF or baseband (BB) or in the LO path.

As anticipated, LO beamforming has been selected for its advantages versus RF beamforming: high granularity LO phase control, orthogonal to signal path so that does not impact signal bandwidth and linearity and easier implementation of the phase shift. However, LO phase shift has its drawbacks: the LO chain and the mixers need to be duplicated for each antenna path which leads to a high-power consumption and increased chip area. Additionally, I/Q quality needed by the modulation scheme needs to be guaranteed for each mixer and the LO phase shift needs to keep I/Q quality during phase shift.

In our architecture, the problems mentioned above are addressed by generating the I/Q split after the PS. Furthermore, passive and lossy I/Q splitters are avoided by using a sub-harmonic I/Q generation scheme: a ±15° phase shift is generated before the last tripler: ±45° phases (I/Q signals) are created after the last tripler. LO amplitude and phase calibration is introduced in the ±15° PS. The benefits of our sub-harmonic I/Q generation are: 1) no I/Q hybrid at D-Band is needed; 2) the limited ±15° phase offset required allows an easy *LC* tuned buffer implementation with limited amplitude variation during phase control; and 3) the 2nd tripler in combination with LO buffers ensures that any limited amplitude variation is eliminated.

Additional fine trimming amplitude and phase controls are implemented in the LO buffers and in the TX upconverter to guarantee an image rejection in the signal band better than 35 dB over the 120–145 GHz frequency range.

B. EVM Analysis

The entire TX signal path is designed for 64QAM modulation with a 5 GHz bandwidth: −25 dB EVM for a signal with a 7 dB peak-to-average-power-ratio (PAPR) has been targeted [28], [29]. The total EVM is set by LO impairments, I/Q mismatch, TX linearity, and thermal noise

$$\text{EVM} = \sqrt{\text{EVM}_{\text{LO}}^2 + \text{EVM}_{\text{I/Q}}^2 + \text{EVM}_{\text{IM3}}^2 + \text{EVM}_{\text{Noise}}^2}. \quad (2)$$

It would be possible to reach a total of −25 dB EVM by allocating −35 dB $\text{EVM}_{\text{I/Q}}$ associated with I/Q mismatch, −40 dB EVM_{LO} associated with LO phase noise, −28.1 dB EVM_{IM3} associated with TX linearity, and −29.5 dB $\text{EVM}_{\text{Noise}}$ associated with thermal noise floor. With −27 dB $\text{EVM}_{\text{Noise}}$ allocated to thermal noise, the total EVM drops to −24 dB and this should be considered the lowest limit to allow 64QAM demodulation.

As far as TX linearity, −28 dB EVM can be achieved by operating Radio at >7 dB back-off from $P_{1\,\text{dB\_TX}}$ compression point. With reference to a minimum healthy margin of −29.5 dB associated with thermal noise, by operating the TX at 7 dB back off from 8 dBm $P_{1\,\text{dB\_TX}}$, and assuming a TX gain of 22 dB, an average input power

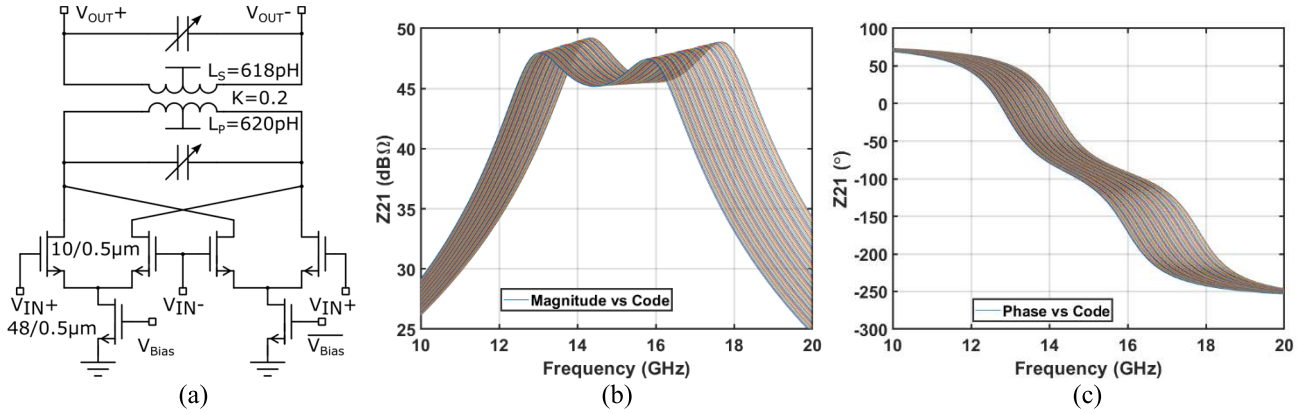


Fig. 2. (a) Simplified schematic of the LO PS/buffer, and simulated performance of the tuneable network, (b) bandwidth and (c) phase.

$P_{\mathrm{IN\_TX}}$ of −21 dBm can be considered in 64QAM mode. The 29.5 dB signal-to-noise (SNR) allocated allows to quantify the thermal noise floor limit as (−21 dBm–29.5 dB) = −50.5 dBm in the 5 GHz bandwidth considered. Consequently, the TX noise figure limit would be given by

$$\mathrm{NF_{TX}} < -50.5\ \mathrm{dBm} - \left(-174\ \mathrm{dBc} + 10\log 10\,(B)\right) < 26.5\ \mathrm{dB}. \quad (3)$$

A reduction in TX gain would relax noise figure requirements, but this would also affect the cumulative $P_{1\,\mathrm{dB\_TX}}$ since the nonlinearity of blocks that precede the PA could not be neglected. The chosen TX gain of 22 dB balances the need to relax the TX noise figure $\mathrm{NF_{TX}}$ and the need to keep the overall $P_{1\,\mathrm{dB,TX}}$ very close to the PA $P_{1\,\mathrm{dB}}$.

As far as LO phase noise: the use of a lower-frequency LO (still external on this prototype) combined with frequency multipliers will allow an easier implementation of a reference PLL running between 14 and 16 GHz with low phase noise, thanks to a potentially large Q of the VCO tank, in combination with a large tuning range. The phase noise added by the cascade of the two triplers is negligible.

Finally, the LO generation scheme and the possibility to calibrate on-chip LO I/Q signals make possible to keep $\mathrm{EVM_{I/Q}} < -35$ dB.

III. Design

A. LO Generation

A single-tone reference signal (14–16 GHz) is off-chip injected, split by a 1-to-4 power splitter and distributed among four antenna/transmitting paths. The LO signal chain in each path is identical and consists of a 15 GHz buffer/phase-shifter, IQ generation, two triplers, and 2-stage LO I/Q buffers. The noise floor of these blocks does not significantly impact phase noise.

The 14–16 GHz PS, shown in Fig. 2, acts also as a buffer and provides isolation from other paths. Since the following triplers also triple the phase, the required phase tuning range at 15 GHz reduces to 360°/9 = 40°, and the controlled phase-step increases by a factor of 9. The design challenge for this block is to maintain a constant amplitude output while achieving full range phase control and subdegree level resolution. The schematic of the designed PS is given in Fig. 2(a). The output matching is a 4th-order network with two 6-bit capacitor banks located in parallel to the primary and secondary windings. By tuning these two capacitor banks, the response of the network moves in frequency which results in a phase tuning. Due to the wideband behavior of the low-k transformer network together with synchronized control of the capacitor banks at primary and secondary, the amplitude variation is reduced, which is further minimized by operating the subsequent stages of the chain in compression. The simulated response is shown in Fig. 2(b) and (c). To further improve the PS tuning range, two differential pairs with tail currents introduce additional polarity swapping.

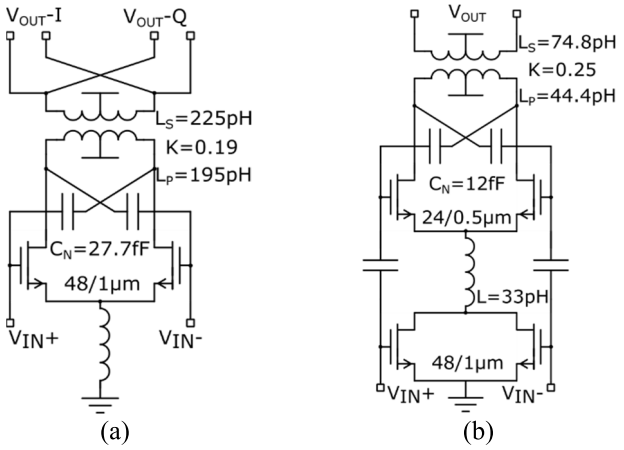


Fig. 3. Simplified schematics of (a) first tripler with 15 GHz input and (b) second tripler with 45 GHz input.

The LO signal is further multiplied to D-band by two cascaded triplers. Triplers are preferred over doublers here for their inherent differential behavior. The first tripler generates around 45 GHz output which is fed into two paths, where I/Q generation is performed. The schematic is shown in Fig. 3(a). A differential pair with capacitive neutralization is used as the active core, which is set in Class-C operation to maximize the harmonic generation. A tail inductor is inserted at the virtual ground to adjust the phase of the common-mode 2nd harmonic component and improve the conversion gain (CG). The differential 3rd harmonic is extracted by

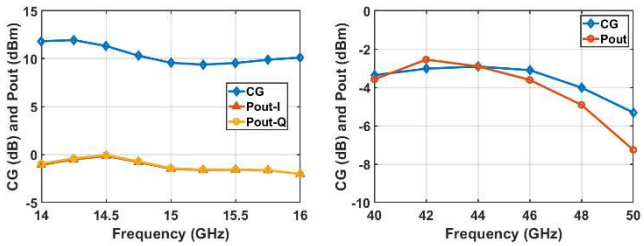


Fig. 4. CG and output power (Pout) of the triplers. (a) First tripler with 15 GHz input and (b) second tripler with 45 GHz input.

a transformer. The simulated CG is better than 9 dB, as shown in Fig. 4(a).

The 45 GHz buffers contain a pseudo-differential pair with capacitive neutralization. An offset between the capacitors in the output-matching network is used to generate a $\pm 15°$ phase offset, which is converted to I/Q LO signals at D-band and fed to the mixers. Like for the 15 GHz PS topology, two capacitor banks are tuned during I/Q calibration. These two buffers also ensure sufficient isolation between the two triplers. Starting from this stage, the back-gate node of all active devices is tuned for fine I/Q calibration, using a V-DAC with a range of 0.15–0.65 V.

A different circuit topology is used for the second tripler because of the reduced transistor gain. The schematic is shown in Fig. 3(b). The second harmonic product is extracted from a frequency doubler and then mixed with the input to generate the D-band output. The phase of the doubler output is adjusted using a series connected inductor to maximize the mixer CG. The simulated performance is shown in Fig. 4(b). The CG is −3 dB at 45 GHz input.

B. I/Q Upconverter

The schematic of the I-path of the upconverter is shown in Fig. 5. The Q-path is identical. The BB input stage contains a feedback loop that enables the input transistors M_{IN} to operate as voltage followers.

The voltages developed at the drain of M_{IN} drive M_F to provide a current $i_{\mathrm{BB}} = (V_{\mathrm{IN+}} - V_{\mathrm{IN-}})/R_B$. This current, multiplied by the area ratio K between M_F and M_{KF}, is then fed into the RF section. The area ratio K sets the total Cgs capacitance that determines the dominant pole, so its value is limited by the required bandwidth. The up-CG, $G_{\mathrm{MIX}} \cong 4/\pi 1/R_B \cdot K \cdot Z_L(f_0)$, does not depend on any transistor transconductance, making this circuit PVT robust, while exhibiting a good linearity at a low supply voltage. Care has been taken in the layout to reduce coupling between RF output signal and LO. Additionally, four independent current mirrors (2 for the I-path, 2 for the Q-path) at the source of the LO switches, keep LO leakage better than 40 dB versus the signal level. The back-gate of M_{KF} is tuneable for additional amplitude calibration to facilitate the image suppression.

C. Power Amplifier

The schematic of the 5-stage PA chain is shown in Fig. 6. Each stage is composed of an nMOS differential pair with

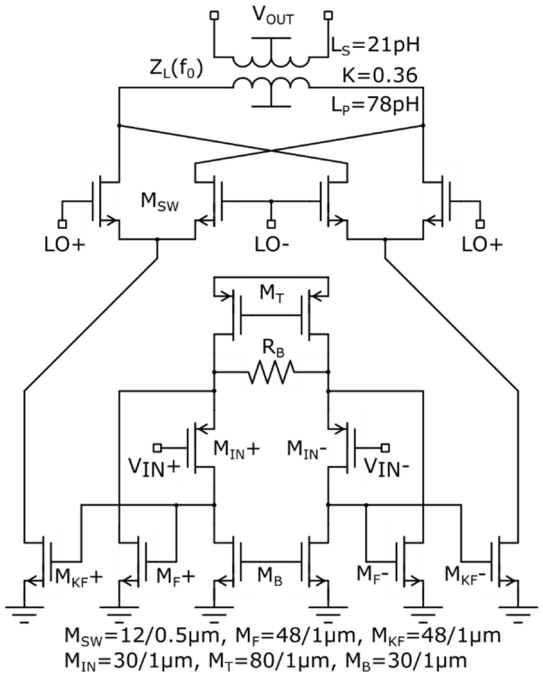


Fig. 5. Architecture of the D-band beamforming transmitter.

capacitive neutralization. The neutralization capacitors are set to ensure unconditional stability at all frequencies. The first stage behaves as a buffer interfacing the I/Q up-conversion mixers, the output of which is split into two subpaths. They are combined at the output of the last stage to increase the output power. Linearity and efficiency have been improved by setting the active cores operating with Class AB biasing. Both differential and common mode stability of the PA chain were ensured by damping any unwanted loop at all frequencies.

The output stage consists of in total 16 nMOS transistor units with a unit size of 1 μm and 24 fingers to ensure an output power larger than 11 dBm. The output balun is optimized to cope with the large output parasitic capacitance while still achieving a proper impedance transformation. The single-ended outputs from two subpaths are combined in parallel at the GSG pad. To achieve a broadband operation, a customized parallel-plate capacitor is inserted in parallel with the GSG pad. The overall insertion loss of the output matching network is around 1 dB and is smaller than 1.2 dB from 110 to 170 GHz. The driver chain in total consists of 4 stages, including the mixer buffer. The size ratio of the full PA is 1:2:3.3:5.3:8, to balance the linearity and efficiency. The interstage matching networks are implemented by 1-to-1 transformers and short differential transmission lines which behave as series inductors to lower the equivalent coupling factor of the transformers for broadband operation. To cope with the large source and load capacitance from the active cores, transformers with small inductance are needed, which lead to low coupling and high loss. In this design, the primary and secondary coils are implemented using two layers to maintain a small inductance, desired coupling factor, and high-quality factor, simultaneously. For instance, the transformer connecting the driver chain output and the last PA stage has a primary and secondary coil inductance of

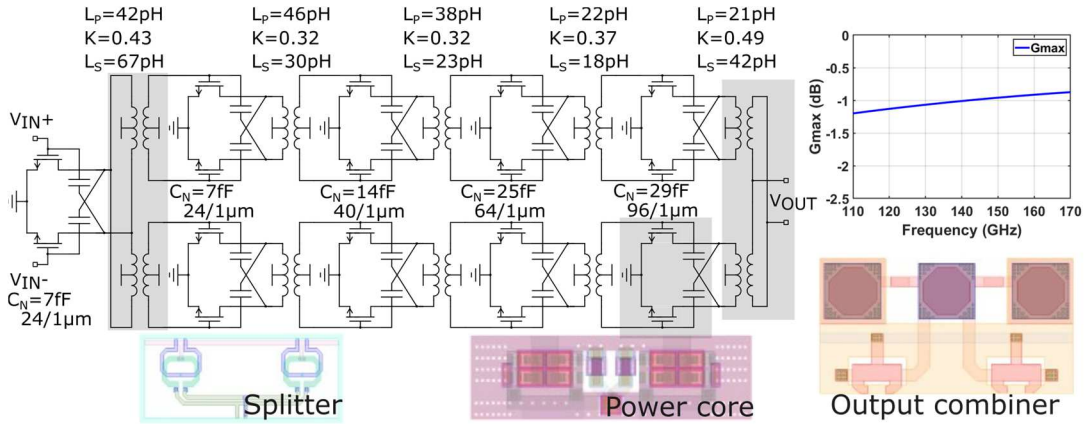


Fig. 6. Architecture of the 5-stage PA chain.

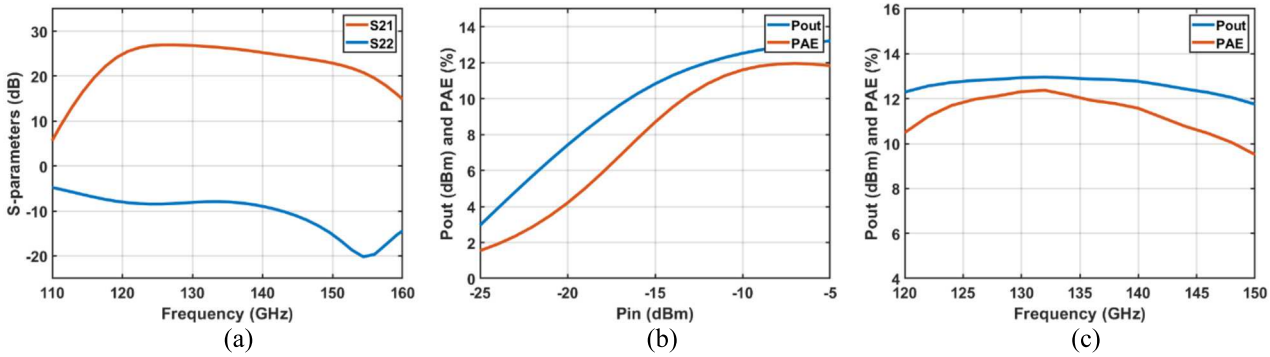


Fig. 7. (a) Simulated performance of the PA chain, including S-parameters, (b) continuous-wave result at 135 GHz, and (c) output power and PAE over frequencies.

21.9 and 19.2 pH, respectively, with a coupling factor of 0.36, and the quality factor is above 25 from 120 to 150 GHz.

The simulated performance is summarized in Fig. 7. The PA achieves a bandwidth from 120 to 150 GHz with power gain larger than 23 dB. It is worth noting that the design of this PA is focused on gain variation within the bandwidth of the modulated signals, for instance, 10 GHz for 16QAM 40 Gb/s transmission, rather than the 3 dB small signal bandwidth or 1 dB $OP_{1\,dB}$ bandwidth which are considered in classical PA designs. At 135 GHz, the PA delivers 12 dBm saturated power to 50 Ω load with a peak 12% PAE. At the 7.5 dBm OP1dB, 6.5% PAE is achieved.

IV. Packaging and Antenna Array

A. PCB Stack-Up

The 4 × 4 phased array is implemented on a ten-layer low-cost high-density interconnect (HDI) printed circuit board (PCB) constructed with Panasonic Megtron7, a commercial high-frequency laminate with a dielectric constant of 3.2 and a loss tangent of 0.002 (Fig. 8). The transmitter beamformer chip is flip-chip mounted on the top metal layer (M1), which primarily handles RF connections and control lines. This layer also accommodates surface-mount technology compatible decoupling capacitors and power distribution lines. Metal layers M2 and M3 are mainly reserved for dc power distribution and digital control signal routing, with

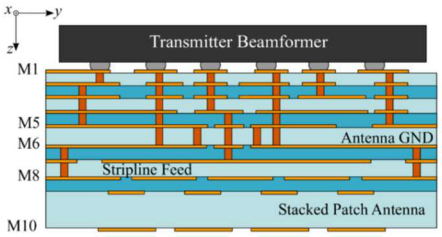


Fig. 8. Ten-layer HDI PCB stack-up for implementation of the antenna array with integrated beamforming IC.

M2 specifically carrying differential transmission lines for BB signals (dc–10 GHz) and LO signals at 14–16 GHz. Layer M4 serves as an RF ground, ensuring proper isolation between the analog and digital domains. To guarantee equal phase and amplitude distribution from the transmitter beamformer to the subarray, four RF interconnect paths at D-band are routed from the center of the subarrays to the IC ports through layer M5. The antenna ground plane is placed on M6, and the hybrid series/corporate-fed array structure occupies the bottommost metal layers, M7–M10. As a result, the IC is positioned behind the subarray-based 4 × 4 phased array, with the total thickness of the PCB being approximately 1 mm.

B. Hybrid Series/Corporate Fed Subarray

Fig. 9(a) illustrates the architecture of the proposed linearly polarized 4 × 4 array, designed for operation within

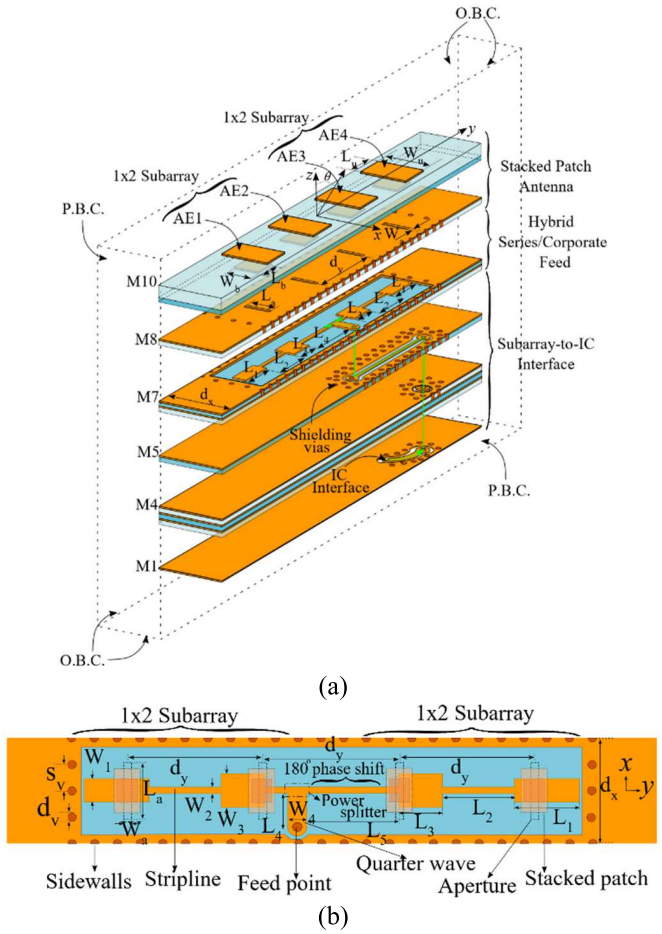


Fig. 9. (a) Exploded view of the hybrid series/corporate fed four-element subarray. (b) Stripline-based subarray feed network. Dimensions: dx = 960 μm, dy = 1241 μm, Wu = 566 μm, Lu = 430 μm, Wb = 440 μm, Lb = 343 μm, Wa = 75 μm, La = 500 μm, $L1$ = 596 μm, $L2$ = 659 μm, $L3$ = 443 μm, $L4$ = 786 μm. (P.B.C.: periodic boundary and O.B.C.: open boundary).

the 120–150 GHz frequency band. The array comprises four 4 × 1 subarrays, each targeting a return loss of at least 10 dB and stable radiation performance across the entire operating band. To support grating-lobe-free beam steering within ±45° in the *XZ*-plane, the subarray width is limited to $0.55\lambda_{\text{min}}$, where λ_{min} is the free-space wavelength at 150 GHz. Furthermore, this architecture enables direct interfacing of the four subarray ports with the four-port transmitter beamformer, integrated at the array's backside to minimize the overall system footprint and mitigate interference. To fulfill these stringent design requirements, a hybrid series/corporate fed aperture-coupled stacked-patch subarray topology is adopted, as illustrated in Fig. 9(b). This topology ensures high isolation between the antenna and IC by placing the chip and antenna on opposite sides of the PCB. Moreover, the use of stripline feeding reduces mutual coupling between subarray feeds. Furthermore, the hybrid series/corporate fed subarray configuration is adopted to achieve stable radiation over a broad impedance bandwidth.

The proposed subarray topology consists of four stacked-patch antenna elements (metal layers M9 and M10), each fed via a stripline feed (metal layers M6–M8) through a rectangular-shaped coupling aperture. The stripline feed network implemented on layers M6–M8 and shown in Fig. 9, realizes the hybrid series/corporate feeding. First, AE1 (antenna element) and AE2 are combined to form a first series-fed subarray, while AE3 and AE4 realize a second. These series-fed subarrays are then fed via a stripline-based power splitter in metal layer M7, equally splitting the input signal. To ensure coherent radiation in the far-field, a 180° phase shift is applied between the output of the power splitter and the series-fed array consisting of AE. Moreover, the elements are spaced $0.55\lambda_c$, where λ_c represents the wavelength at the center frequency of 135 GHz, to minimize deviations across the frequency band, ensuring consistent beamwidth and sidelobe level. This results in a subarray footprint of 0.96 × 5 mm, corresponding to $0.55\lambda_c \times 2.5\lambda_{\text{min}}$. The dimensions of the stacked patches and the coupling aperture remain constant throughout the subarray. Broadband impedance matching is achieved solely by adjusting the stripline feed, while guaranteeing equal phase and amplitude signal distribution. Wide transmission lines are used beneath the apertures of the inner antenna elements to maintain phase-stable power division over the target bandwidth while the widths of the two stubs at each outer end of the array are optimized to achieve the desired radiation conductance. To ensure coherent interference in the far-field, the interconnecting lines between the patches are set to $\lambda/2$, where λ is the guided wavelength at 135 GHz.

C. Wideband Subarray-to-IC Interface

Flip-chip mounting the beamforming IC onto the PCB using bumps introduces inductive effects, while the pads on the M1 layer contribute capacitance. Additionally, the metal layers within the chip add reactance, which becomes increasingly significant at D-band frequencies. These factors can cause significant impedance mismatch between the subarray and the beamformer chip, thereby degrading system performance. Therefore, it is essential to develop a co-simulation model to optimize the subarray-to-IC interface and achieve high performance. The complete co-simulation model includes the chip layout, bump array, layer-to-layer transition, and subarray structure, all modeled using the frequency-domain solver within the CST full-wave electromagnetic simulator. The analysis was conducted under periodic boundary conditions, see Fig. 9. The proposed subarray-to-IC interface achieves a return loss of 15 dB and transition loss of less than 2 dB over 120–150 GHz frequency range, accounting for both the bumps and a 125 μm grounded coplanar waveguide (GCPW) trace length, see Fig. 10(a). The co-simulation model exhibits a wideband input match across the targeted frequency range, even when scanning up to 45° in the *XZ*-plane, as shown in Fig. 10(b). The realized peak gain for different steering angles, illustrated in Fig. 10(c), remains stable at approximately 7.8 dBi throughout the frequency band, with a maximum cross-polarization of 40 dB during scans up to 45°. Note that the ripples in antenna gain versus frequency specifically at 45° and 60° steering angles arise from two primary factors: 1) field leakage due to single-wall RF line routing from M1 to M7 in the periodic boundary condition setup; and 2) unshielded dielectric layers supporting M9 and M10.

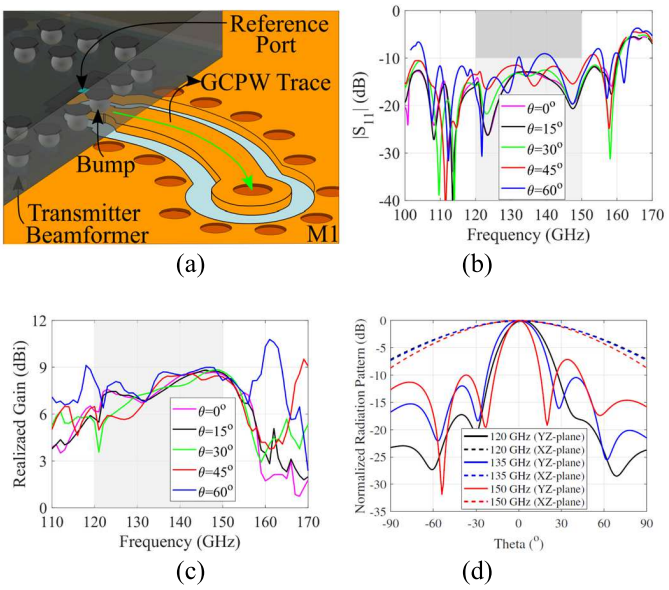


Fig. 10. (a) EM-simulation model of IC-to-subarray interface with detailed view of 50 Ω reference port in positioned in the transmitter beamformer flip-chip mounted onto the PCB. (b) Active reflection coefficient when scanning to 60°. (c) Realized peak gain for different steering angles and (d) normalized radiation patterns when steered to broadside.

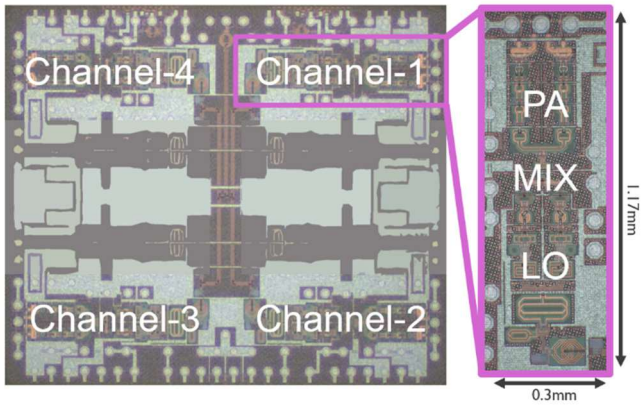


Fig. 11. Chip photograph.

In HDI PCB technology, the thick dielectric layers required for wide impedance bandwidth prevents the inclusion of closely placed laser vias around each subarray to suppress surface wave excitation effectively. This issue is addressed in the finite-sized array design, resembling the final 4 × 4 array implementation presented later in the article [see Section V], by strategically placing larger vias around the array [see Fig. 9(a)] and incorporating a second row of vias [see Fig. 9(b)] to effectively suppress undesired leakage. Importantly, the co-simulation subarray radiation gain accounts for both dielectric and ohmic losses up to the reference port in the chip layout, resulting in an average efficiency of 65% when scanning to 45°. The antenna achieves half-power beamwidths (HPBWs) of 107° in the *YZ*-plane and 28° in the *XZ*-plane at 135 GHz, see Fig. 10(d), while sidelobe levels are suppressed by 10 dB across the operating frequency band.

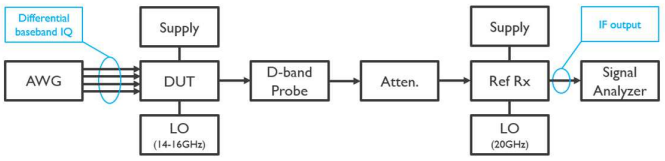


Fig. 12. Measurement setup for single transmitting path probing characterization.

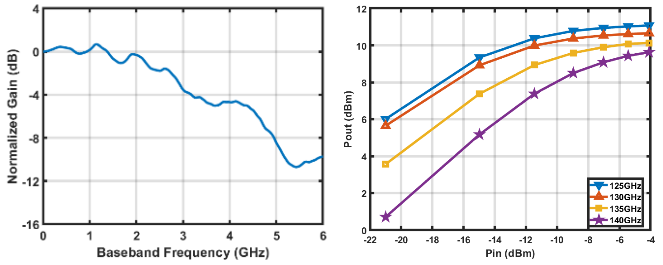


Fig. 13. Channel response for LO of 135 GHz (left), and Pout versus Pin over different LO frequencies (right).

V. Measurements

The IC has been fabricated in a 22 nm fully depleted silicon on insulator (FD-SOI) technology and occupies a chip area of 2.3 × 2.7 mm^2, see Fig. 11. A single transmitting path occupies an area of 1.17 × 0.3 mm^2. The four PAs are located close to the chip edges for better thermal dissipation. The inner half chip area is reserved for four receiving paths which are not covered in this article. The 14–16 GHz LO signal is injected into the chip via GSG pad at top-middle edge, which is split into four paths at the center of the chip. This center area is also reserved for integrating the frequency synthesis on-chip in future implementations.

A. Single TX Element

Single transmitting path characterization, the measurements are done with the setup of Fig. 12. The chip is wire-bonded onto a PCB carrier, including the BB I/Q connections, LO injection, SPI control, and supply connections. The D-band outputs are measured with a probe station. A reference receiver used to characterize the TX chip is built with off-the-shelf components. The frequency response of the cables and the PCB traces is de-embedded from the measurements. The full TX frequency response at an LO frequency of 135 GHz is shown in Fig. 13(a). The measured 4 GHz instantaneous bandwidth includes the influence of the 1.8 mm long bond wires, probes, and the reference receiver. The measured output versus input power of one antenna path at different LO frequencies, shown in Fig. 13(b), the maximum P_{SAT} is around 11 dBm using a 0.8 V supply. In the band 125 and 140 GHz, the TX has less than 6 dB gain variation at low-input power levels. This gain variation is mainly due to reduced LO power as LO frequency increases. The P_{SAT} variation in this frequency range is below 2 dB. The TX spectrum is shown in Fig. 14 for a 135 GHz LO frequency. A BB I/Q signal tone of 1 GHz is injected into the chip, and the TX output is down converted to 10 GHz IF frequency for evaluation. The

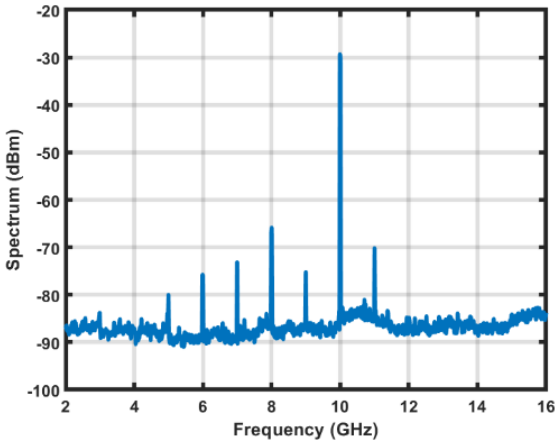


Fig. 14. Measured spectrum (down converted to 10 GHz) with BB and LO frequencies of 1 and 135 GHz.

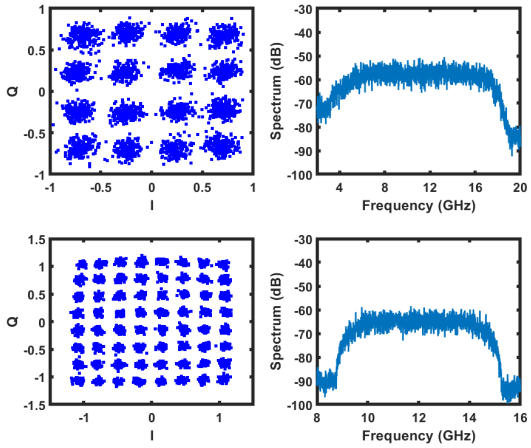
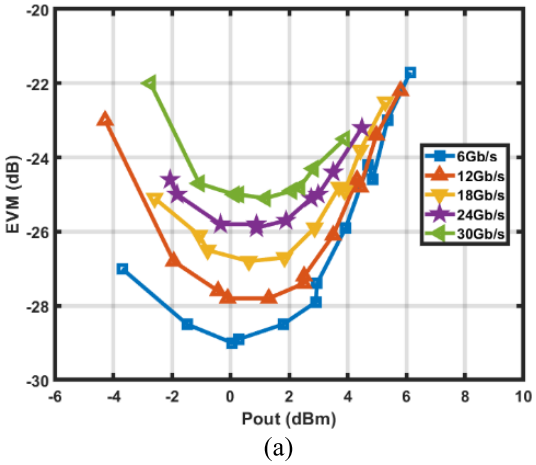
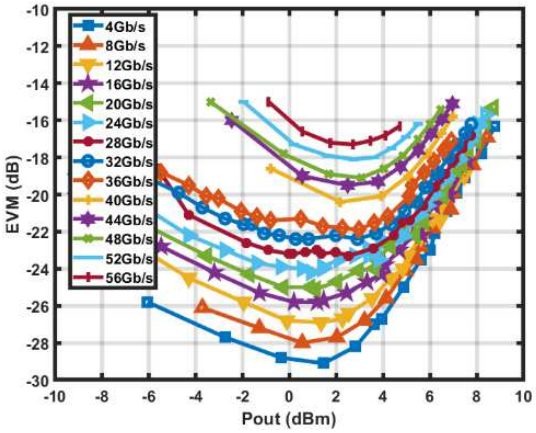


Fig. 15. Measured constellation and spectrum for 56 Gb/s 16QAM (top) and 30 Gb/s 64QAM (bottom).



(a)



(b)

Fig. 16. Summary of EVM versus output power for (a) 64QAM and (b) 16QAM, with LO frequency at 135 GHz.

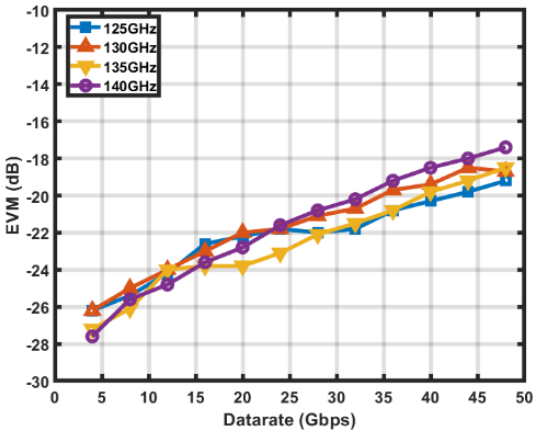


Fig. 17. EVM versus data-rates (16QAM) over four LO channels.

LO feedthrough and the image levels are 35 dB below the carrier. Other spurs at lower levels are generated by the RX reference receiver. The LO feedthrough and the image level are better than 33/34 dB, 35/4 dB, and 38/36 dB, for LO tone of 125, 130, and 140 GHz, respectively.

In Fig. 15, 16QAM and 64QAM constellations are shown for 56 and 30 Gb/s with an EVM better than −17 and −25 dB, respectively. Gain variations due to the measurement setup and by the chip are detected by the equalizer in the vector software analyser (VSA), and the resulting compensated data are applied to the AWG (Fig. 12). Then, EVM performance and corresponding output power are measured without further equalization or error correction. At 135 GHz, the TX can deliver 16QAM modulated data at 56 Gb/s with a 3 dBm output power to a reference 50 Ω load, with EVM better than −17 dB.

The TX EVM versus P_{OUT} is reported for different data rates and modulations in Fig. 16 at an LO frequency of 135 GHz. With 64QAM modulation, the maximum data rate of 30 Gb/s is limited by the TX thermal noise floor. For 16QAM modulation, the EVM versus data rate for different LO frequencies is shown in Fig. 17: 48 Gb/s is guaranteed across the entire 125–140 GHz LO range. The phase measurement at D-band is very challenging. The main reason is that the signal is heavily influenced by the phase noise of the LO reference, and it is even worse when a reference receiver is used due to the superposition of two uncorrelated phase noise source. In this measurement, a replica of the signal

TABLE I
COMPARISON WITH STATE-OF-THE-ART D-BAND TRANSMITTERS

	Process	Freq. Range [GHz]	Architecture Integration Level	Beamforming (BF)	P_{SAT} /P_{1dB} (dBm)	P_{DC} Channel (mW)	Channel Area (mm^2)	Mod.	DR (Gb/s)	P_{OUT} (dBm)	EVM (dB)	Antenna system
This work	22nm FDSOI	120-145	Zero-IF BB to D-Band Ext. 16GHz LO	2x2 LO BF	11 /7.5	232	0.35	16 QAM	56	3	-17	1x4 Subarray (PCB)
								64 QAM	30	2	-25	
[4]	22nm FFET	140	Zero-IF DAC to D-Band, PLL	N/A	7.5[#] /NA	173	0.75	QPSK	80	0.8	-17.3	NA
								16 QAM	160	0.8	-17.1	
[1]	45nm RFSOI	140-158	Super-Het (IF=60GHz) + Channel Bonding Ext. 4.32GHz LO	N/A	NA /1.6[$]	1580	NA	16 QAM	57.6	-8.6[$]	-14.7	Patch + Lens (PCB)
[10]	22nm FDSOI 0.25um InP	131-137	IF (4GHz) to D-Band Ext. 15GHz LO	N/A	17[+] /NA	760	NA	16 QAM	20	14	-21.5	1x8 array (LTCC)
								64 QAM	30	11	-21.4	
[19]	130nm BiCMOS	130-164	RF Front-End	2x2 RF BF	12 /NA	265	0.9	64 QAM	30	4	-24.2	16x16 array (Glass)
								256 QAM	8	4	-26.9	
[9]	45nm RFSOI	137.5-145	IF (9-14GHz) to D-Band Ext. 20GHz LO	8x8 RF BF	-2.5[*] /NA	N/A	1.31[**]	16 QAM	22	-16[*]	-26	8x8 array (PCB)
								64 QAM	24	-14[*]	-29.1	

([#]) Simulated P_{SAT} for PA only, ([$]) Used 25dBi to estimate P_{OUT} and P_{1dB} from 26.4dBm $EIRP_{1dB}$, (+) Computed from EIRP. ([*]) Part of 64 elements array, assumed 40dB array gain for the $EIRP_{SAT}$/$EIRP_{1dB}$ 37.5dBm/33dBm (estimated from figure) and 24/26dBm EIRP for 16QAM/64QAM ([**]) 9.84mm×9.27mm for 64 channels and it also includes RX.

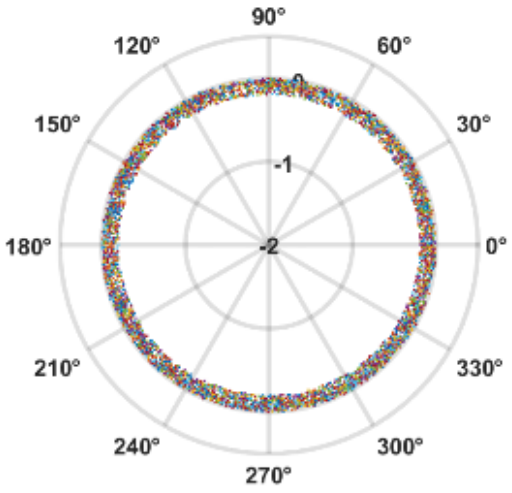


Fig. 18. Performance of phase control versus control code and normalized output power (radial direction).

chain (including DUT) is used to measure the phase control. The reference chain has the same multiplication factor in the up and down conversion, so that these two chains can share the same LO sources. The accurate phase information can be extracted by comparing the receivers' output using a high precision scope while the output power of the TX is captured by a power meter. The measured output power as a function of phase control, see Fig. 18, shows that the phase can be swept in a full 360° range with a 0.1° granularity while keeping the output power variation within 0.2 dB. The measurement is conducted at 4 dBm output power level.

The performance of a single-channel TX is summarized and compared to state of the art in Table I: our work has the highest P_{SAT} among CMOS implementations with a high level of integration and ranks among the lowest power consuming ones. Furthermore, our TX can handle a data rate of 48 Gb/s for any LO frequency between 125 and 140 GHz. Further, the TX can support 64QAM modulation at 30 Gb/s. The 0.1° phase shift resolution enables accurate beamforming of a massive antenna array.

B. 4-Way TX Beamformer–OTA Link

After the probing characterization, the control and calibration profile are obtained. The IC with bumps is flip-chip mounted to the high-frequency PCB to assess functionality and beamforming capabilities. A reference receiver, similar to the probing characterization, equipped with a horn antenna is used to evaluate the radiation performance of the whole system. The measurement environment and packaged module are shown in Figs. 19 and 20. The transmitter board is placed on a rotating platform and the reference receiver is put on 0.4–1 m away at a fixed location to capture the radiation. The received signal is down converted at 9 GHz and analyzed by VSA software in a high-speed scope. 5G NR waveforms are used during the wireless characterization.

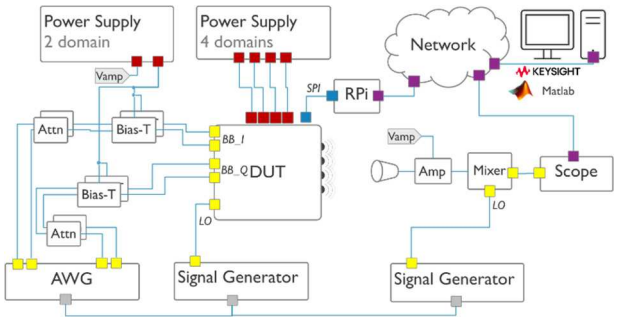


Fig. 19. System diagram of the OTA measurement setup.

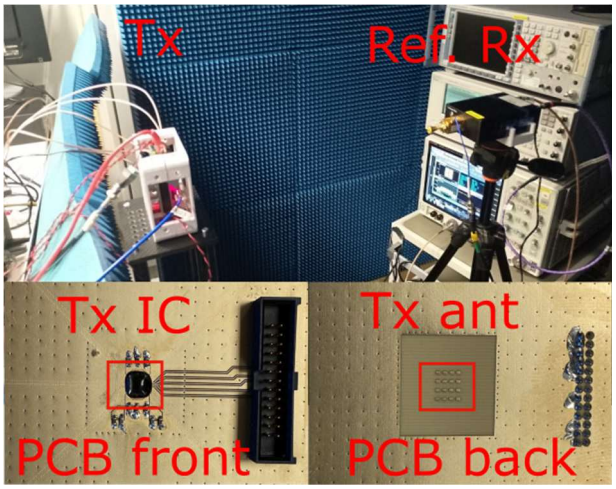


Fig. 20. Photograph of the OTA measurement environment and the packaged transmitting array board.

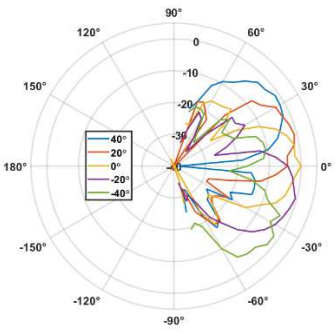


Fig. 21. Measured radiation patterns for ±40° beamforming test in *YZ*-plane.

Two independent LO sources are used, and the impact of the uncorrelated phase noise is included in the results. The radiation pattern of the 4-way beamformer versus steering angle has been measured and a steering angle of ±40° has been demonstrated (see Fig. 21). The 4-way beamformer has 12 dB extra gain versus the on-path elements. The simulated peak EIRP is 30 dBm and due to limitations of laboratory equipment, it has not been possible to conduct an OTA measurement.

A 24 Gb/s data rate 5G NR standard waveform has been sent OTA and demodulated with −24.8 dB EVM (see Fig. 22). Please note that to facilitate the beam-steering measurement

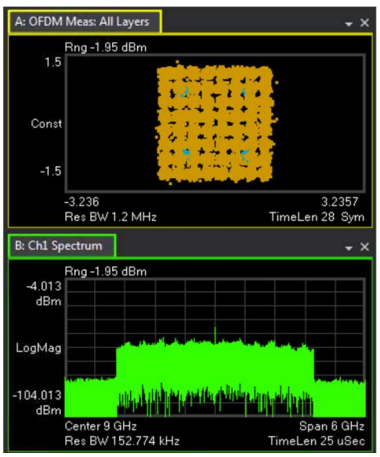


Fig. 22. Measured constellation and spectrum of a 24 Gb/s data rate wireless transmission using 5G NR waveforms.

and reduce the mechanical tension applying on the DUT, flexible coax cables were used for the BB connection, which introduces frequency-dependent amplitude and phase variation. This possible impairment has not been de-embedded from the reported measurements.

VI. Conclusion

We demonstrated a zero-IF D-band 4-way fully integrated TX beamformer based on LO shifting and designed in 22 nm FDSOI. The single-channel TX has a 7.5 dBm output $P_{1\,\mathrm{dB}}$ and achieves a 56 Gb/s data rate with 16QAM modulation at 3 dBm Pout and 30 Gb/s with 64QAM modulation. The single-channel TX draws 232 mW from a 0.8 V supply, and it has an area of 1.17×0.3 mm^2. The PS provides full 360° control range with a 0.1° phase resolution and less than 0.2 dB output power variation. The 4-way TX beamformer occupies and area of 2.7×2.3 mm^2, it has been flip-chip mounted into a PCB with integrated PCB Antenna and measured with a reference receiver. The measured full scanning angle is ±40° with 24 Gb/s with −24.8 dB EVM at 40 cm distance between 4-way beamformer and reference receiver. The full link data-rate is limited by a combination of PCB assembly and measurement setup. This work ranks among the best as a combination of integration level, data rate, output power, and phase resolution and solves some of the challenges of LO beamformings as far as ortogonality of LO phase control and I/Q quality, compact implementation for the full LO chain and PS shifter.

Acknowledgment

The authors would like to thank F. Poelsler, H. Suys, M. Shrivas, and Z. Zong for their valuable support.

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