

Evolution of lithography-to-etch bias in multi-patterning processes ^{EP}

Prem Panneerchelvam; Ankur Agarwal; Chad M. Huard; ... et. al



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Prem Panneerchelvam,^{1,a)}  Ankur Agarwal,² Chad M. Huard,¹  Alessandro Vaglio Pret,¹ Antonio Mani,³ Roel Gronheid,³ Marc Demand,⁴ Kaushik Kumar,⁴ Sara Paolillo,⁵ and Frederic Lazzarino⁵

AFFILIATIONS

¹KLA Corporation, Austin, Texas 78759, USA

²KLA Corporation, Milpitas, California 95035, USA

³KLA Corporation, Haasrode, 3001 Leuven, Belgium

⁴Tokyo Electron Europe Limited, Crawley RH10 9QL, United Kingdom

⁵imec vzw, 3001 Leuven, Belgium

^{a)}Electronic mail: Premkumar.Panneerchelvam@kla.com

ABSTRACT

Quantitatively accurate, physics-based, computational modeling of etching and lithography processes is essential for modern semiconductor manufacturing. This paper presents lithography and etch models for a trilayer process in a back end of the line manufacturing vehicle. These models are calibrated and verified against top-down scanning electron microscope (SEM) and cross-sectional SEM measurements. Calibration errors are within 2 nm, while the maximum verification error is less than 3 nm. A fluorocarbon plasma etch of the spin-on-glass (SOG) layer accounts for most of the etch bias present in the process. The tapered profile in the SOG etch step is generated due to the polymerization process by fluorocarbon radicals generated in the plasma. The model predicts a strong correlation between the etch bias in the SOG etch step and the neutral-to-ion flux ratio in the plasma. The second etch step of the flow, which etches the spin-on-carbon (SOC) layer using an H₂/N₂ plasma, results in a negative etch bias (increase in CDs) for all measured features. The ratio of hydrogen to nitrogen radical fluxes effectively controls the etch bias in this step, with the model predicting an increase in the etch bias from negative to positive values as the H-to-N ratio decreases. The model also indicates an aspect ratio dependent etch rate in the SOG and SOC etch steps, as seen in the etch front evolution in a three-dimensional test feature. The third and final step of the process, SiO₂-etch, generates an insignificant etch bias in all the test structures. Finally, the accuracy of the etch simulations is shown to be dependent on the accuracy of the incoming photoresist shapes. Models that consider only the top-down SEM measurement as input and do not account for an accurate photoresist profile, suffered significant errors in the post-etch CD predictions.

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I. INTRODUCTION

Direct pattern transfer using ArF lithography requires a thin photoresist layer as feature sizes continue to shrink in modern integrated circuits. Such thin photoresist layers are often not sufficient to act as a hardmask for etching the target substrate structures. To solve this problem, multi-layer hardmask systems with oxide and carbon-based intermediate layers are frequently employed. Upper layers are chosen to have high selectivity to the photoresist mask, and lower layers are chosen to provide a strong hardmask for etching the target substrate features. Amorphous carbon and SiON layers are commonly used because of their high etch-selectivity and physical

strength. However, with the advent of spin-coating technology, spin-on-hardmasks (SOHs) have replaced the ACL and SiON layers in state-of-the-art trilayer resist systems.^{1,2} The spin-on process technology also allows manipulating the thickness and optical properties of the hardmask layers, which is crucial for providing optimal anti-reflective properties for the lithography process.

Along with multilayer hardmask systems, multi-patterning techniques are commonly employed in the latest technology nodes to overcome the 193 nm immersion lithography resolution limit. These techniques are particularly essential for back end of the line (BEOL) manufacturing, where the interconnect pitches in the latest technology nodes can be as small as 20 nm. Several multi-patterning schemes like

self-aligned double patterning (SADP),³ self-aligned quadruple patterning (SAQP),⁴ and litho-etch-litho-etch (LELE)⁵ have been successfully used to print features that are otherwise impossible using conventional 193 nm immersion lithography.

In this landscape of complicated processing steps, there can be features on the wafer whose critical dimensions (CDs) deviate from the design values by more than the allowable error budget. These features are often called “hotspots” and can be induced after any step of the multi-patterning flow. These hotspots must not only be detected accurately but also be removed by optimizing either the process conditions of lithography and etching/deposition or by modifying the photomask. Optical proximity correction (OPC) is an especially powerful approach, where the photomask layout is adjusted on a per-feature basis to mitigate hotspots and compensate for CD errors.^{6–8} For OPC engineers who aim to remove etch-related defects, the current standard is to use an *etch bias table*. This technique involves compiling a table of etch CD biases (difference in CD between ADI and AEI) as a function of several pattern parameters such as photomask CD, ADI CD, pitch, and lithography process parameters like focus and exposure dose. The data in this table are typically obtained by running experiments at several lithography process conditions and measuring the CDs for several features using a scanning electron microscopy (SEM) tool. The etch table predicts the etch bias for the defects on the wafer and provides inputs to the extent of corrections required on the photomask layout to clear the defects.

Physically rigorous computational models can aid an OPC engineer because of the availability of rich three-dimensional information in them. Such models can provide valuable insights into the evolution of etch profiles and, for example, their dependence on lithography parameters such as photomask layout and laser settings. Stout *et al.*⁹ discussed the utilization of physics-based models to analyze the cumulative effect of a multistep gate etch process starting from ADI. These models provide insights into the evolution of etch bias through the various etching steps of a multistep process and help understand how to modulate the bias using process parameters like plasma source power, gas chemistry, and pressure. Accounting for the etch process provides additional degrees of freedom for an OPC engineer to remove the hotspots effectively.¹⁰

In this article, we discuss the development of physically rigorous models for both the lithography and etch process steps, which are utilized to simulate a multi-patterning process flow. With sufficient accuracy, these models can help reduce the number of experiments required for optimizing the input settings of the process such that the propensity to form hotspots on the wafer is minimized. In this work, we establish the quantitative accuracy of these models by demonstrating calibration to experimental data obtained from the first pass of a LELELE process in a BEOL test vehicle developed at IMEC. More importantly, we also demonstrate the predictive capability of these models outside the calibration regime. A schematic of the steps involved in the first LE pass of the patterning flow and the wafer topography dimensions relevant to this process is shown in Fig. 1. The hardmask for the target low-k material is a 25 nm titanium nitride (TiN) layer. Patterns are transferred onto the TiN layer using a LELELE process with a stacked trilayer resist system containing 100 nm of spin-on-carbon (SOC)

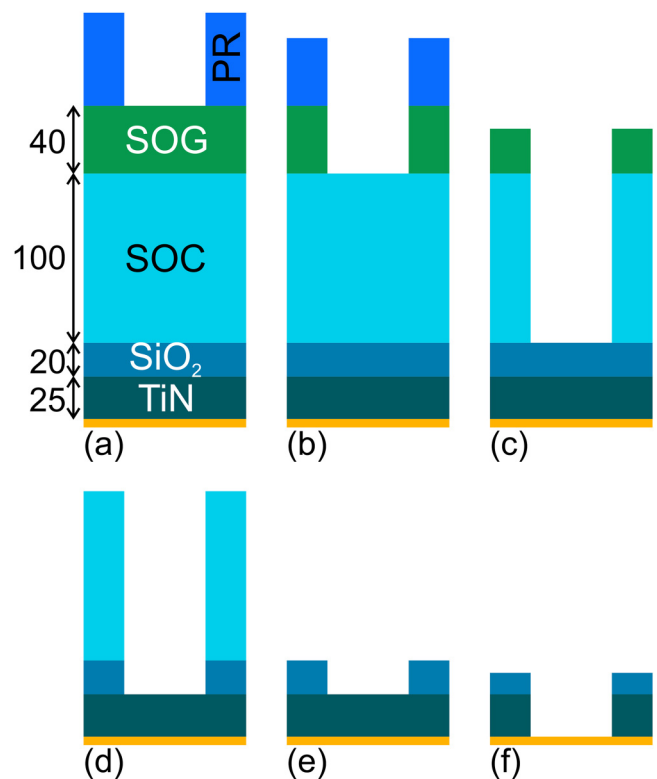


FIG. 1. Wafer topography and schematic of the LE process on a line pitch grating feature. Schematic profiles are shown after (a) lithography step. (b) SOG etch step. (c) SOC etch step. (d) SiO₂ etch step. (e) SOC strip. (f) TiN etch step.

and 40 nm of spin-on-glass (SOG), over which the photoresist pattern is printed using 193 nm ArF immersion lithography. The SOC layer is deposited on top of a 20 nm SiO₂ layer to enable the different passes of the LELELE process. Once the photoresist is printed over SOG, the pattern is transferred onto each layer using a dry etch process with different recipes to ensure selectivity to the over and under layers.

The remainder of the paper is organized as follows. The experimental setup for the lithography and etch steps are described in Sec. II. The computational models used to investigate the processes are described in Sec. III. In Sec. IV, the results of model calibration and verification are discussed. In Sec. V A, the results of the lithography process are described. The SOG and SOC etch steps that account for most of the etch bias present in the trilayer are discussed in Secs. V B and V C. SiO₂-etch and the steps involved in the process are briefly described in Sec. V D. Finally, the role of accurate photoresist shapes in the accuracy of the etch simulations is discussed in Sec. VI.

II. EXPERIMENTAL SETUP

A. Lithography

A negative tone development (NTD) process was utilized to print patterns in the photoresist using 193 nm immersion

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lithography on an ASML NXT:1970i scanner. NTD materials are known for printing features with small critical dimensions with a wider process window.¹¹ In this work, two sets of wafers were exposed under different lithography conditions. The first set was patterned at the optimized focus and dose across the wafer. Measurements from these wafers inform the CD uniformity across the wafer at various stages of the pattern transfer and hence will be referred to as *CDU* wafers in the rest of the article. The second set of wafers was patterned, while varying the focus and dose at different die locations on the wafer, commonly referred to as focus-exposure matrix (FEM) wafers.⁸ These wafers inform the lithography process window for various features of interest in the mask layout.

B. Etching

The trilayer hardmask and SiO₂ films were etched in a capacitively coupled plasma reactor using multiple steps without breaking vacuum. Each etch step was optimized to yield good selectivity to the under and overlayers. The etch recipes are summarized in Table I.

Patterns in the photoresist are transferred into SOG using a fluorocarbon plasma which is known to provide reasonable selectivity for SiO₂ (around 2–5).¹² The SOG layer, which is chemically composed of SiO₂ with nonreactive dopants, is expected to etch with similar selectivity. The over-etch step for SOG utilizes a lower bias power relative to the main etch step to enable the etching of any remaining SOG with high selectivity to SOC. H₂ in the SOC etch recipe effectively ashes the photoresist, but the recipe is selective to SOG, enabling pattern transfer to the SOC layer. The SOG layer is entirely removed in the next step, where patterns are transferred into SiO₂. Following the SiO₂ etch step, the remaining SOC is stripped using an O₂ plasma, ensuring high selectivity to the etched SiO₂.

The process flow comprising the lithography and etch steps constitute the first pass of the LE³ multi-patterning scheme in the manufacturing vehicle. Following this first pass, the SOC and SOG layers are spin-coated on top of the patterned SiO₂ structures, and the second pass of LE is executed. The patterns present in SiO₂ are transferred to the underlying TiN only after the third pass. In this work, we have focused on only the first LE pass of the LE³ flow.

C. Metrology

CDs of different features were measured using the Hitachi CG5000 top-down CD-SEM tool on both the lithography and etch wafers. The line pitch grating structures that were measured are summarized in Table II. The six structures represent a varying duty ratio (ratio of CD to pitch) of 0.22 to 0.65, representing iso and dense features. Note that the photomask CDs in the table represent

TABLE I. Recipes for the trilayer hardmask and SiO₂ etching.

Layer	Plasma	Time (s)
SOG main etch	Fluorocarbon mixture	50
SOG over etch	Fluorocarbon mixture	30
SOC	H ₂ /N ₂	150
SiO ₂	Fluorocarbon	100

TABLE II. List of line-space features measured.

Name	Photomask CD (nm)	Pitch (nm)	Design intent ADI CD (nm)
A1	45.0	96	40
P128	64.0	128	55
P160	96.0	160	93
A2	63.5	144	40
P168	110.0	168	60
P400	88.0	400	60

the line CD of the structures in the mask layout, and they print as space in the photoresist layer because of the NTD lithography process. The table also includes the design-intent ADI space CD of these structures post lithography development for this process based on prior knowledge. The actual measured ADI CDs for these features are reported in Sec. IV A.

Additionally, a tip-to-tip feature on the same die was also measured using CD-SEM. This feature is characterized by a tip-to-tip photomask CD of 72 nm within a dense line pitch grating structure. The schematic of this feature is shown in Fig. 2. This feature was included in the study to investigate the microloading effects that might arise during the etch steps.

III. COMPUTATIONAL MODELS

A. Lithography

Continuum resist model simulations were performed using the PROLITHTM Enterprise (KLA Corporation)¹³ simulator.

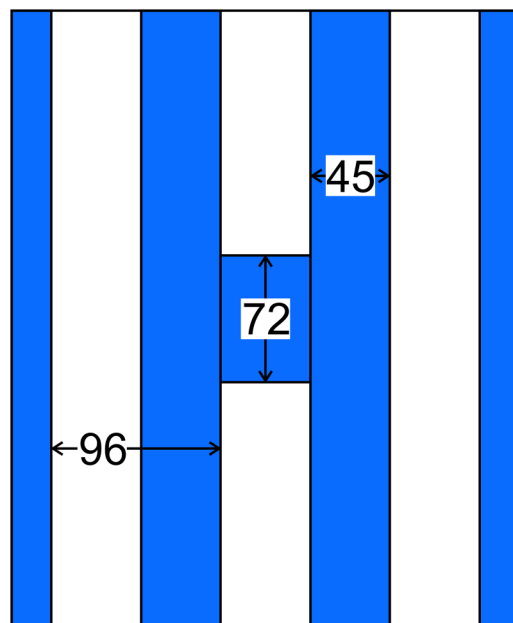


FIG. 2. Photomask layout of the tip-to-tip feature. All dimensions are in nm.

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PROLITH simulates the various steps of ArF immersion lithography using a first-principles description of the underlying physics. The engine models the image formation on the photoresist, post-exposure bake and development. The inputs to the engine are the photomask layout, laser settings like focus and exposure, and chemical properties of the photoresist material, and the output is the three-dimensional photoresist profile generated after development. A more detailed description of the PROLITH engine can be found here.¹⁴

B. Etching

The etch processes are computationally investigated using ProETCH[®], a physics-based dry etch simulator developed at KLA. The simulation engine models the evolution of the features under exposure to energetic and reactive species generated in the plasma. ProETCH inputs the photoresist profiles from PROLITH and the underlying film stack topography. The incoming geometry is discretized as a collection of voxels in 3D space, with each voxel tagged by a material identity. The evolution of this voxel mesh over time due to interactions with the plasma is tracked to predict the post-etch profiles.

The plasma species interacting with the etching feature are modeled as pseudoparticles. Each pseudoparticle represents a collection of the actual atoms or molecules of reactive and energetic species generated in the plasma that are important to describe the plasma-surface interactions. The weight of the pseudoparticle, defined as the number of actual etchant atoms it represents, is calculated by assuming the interaction between a pseudoparticle and the atoms contained in a single material voxel satisfies reaction stoichiometry. Hence, the weight equals the number of real atoms represented by a computational voxel, which is equal to the product of the material density and the voxel volume.

The simulation engine launches these pseudoparticles toward the etching feature until the time elapsed in the simulation equals the process time. After each particle is launched, the simulation clock is updated based on the time per pseudoparticle, given by

$$\delta t_{pp} = \frac{\Gamma_{total} \cdot A_{sim}}{W_{pp}},$$

where Γ_{total} is the total fluxes of the incoming plasma species, A_{sim} is the top-down area of the simulation region (typically thought of as the area in the XY plane), and W_{pp} is the weight of the pseudoparticle. The launched particle's identity, incoming angle, and direction are calculated based on the plasma species flux and energy angle distributions. The overall evolution of the feature is achieved by tracking the transport of pseudoparticles through vacuum and their interaction with the material voxels. When a pseudoparticle interacts with the material voxel, one of the following three types of modification can occur at the interaction site:

- (1) Removal: This interaction occurs during a sputter event by energetic ions or during a thermal etch process.
- (2) Change: This interaction represents the formation of chemical bonds between the impinging plasma species and the surface

material. The modified voxel can be thought of as a mixing or selvage layer.

- (3) Deposition: This interaction represents the process where reactive radical species stick to the material, causing deposition thereby a new voxel with associated material identity is created.

To simulate the different etch steps of the LE process, a surface reaction mechanism representing the physical and chemical interaction of the materials in the trilayer stack with the associated plasma species is used to model the interaction between the pseudoparticles and the voxels.

C. Surface reaction mechanisms

Spin-on-glass is usually a doped variant of SiO₂, with carbon, boron, or phosphorus as possible dopants. While SiO₂ can interact with reactive neutrals from a fluorocarbon plasma, boron and phosphorus do not play an active role in the etching chemistry. Therefore, the surface chemistry mechanism for the etching of SOG is similar to the SiO₂ etch in a fluorocarbon plasma, where the etch proceeds by forming a thin polymer layer over the surface. Reaction pathways in a fluorocarbon etch of SiO₂ are well documented in the literature^{15,16} and are only briefly described here. The mechanism developed here includes pathways for the formation of the mixing layer, where Si-F and C-O chemical bonds exist, and the fluorocarbon polymer overlayer formation. These surface states are formed by the interaction of the substrate with sticky fluorocarbon radicals (example: CF, CF₂) from the plasma. The mechanism includes the physical sputter pathway by the energetic fluorocarbon ions. It also includes the thermal etching of polymer by fluorine, an essential pathway for polymer removal in plasma systems with low ion energies.¹⁷

Spin-on-carbon etching in H₂/N₂ plasmas occurs by successive hydrogenation of surface sites by hydrogen radicals forming CH_x (that is, CH followed by CH₂ and CH₃). Hydrogen radicals in the plasma can also spontaneously etch the passivated CH_x sites to form the volatile CH₄ product. To balance this spontaneous etch, the nitrogen radicals from the N₂ feedstock gas present in the plasma facilitate the formation of a hard CN layer, which has higher sputtering threshold energy relative to CH_x. The hydrogen radicals can also adsorb on this hard CN layer forming HCN, which is removed with a very low energy threshold because of the formation of volatile HCN gas. The reaction mechanism developed here is based on previous work by Van Laer and co-workers.¹⁸ Recall that both the remaining photoresist and SOG films are also exposed to the H₂/N₂ plasma during this step. While SOG does not chemically interact with H or N radicals, the etch of the photoresist is facilitated by the H radicals that interact with the hydrofluorocarbons present in the photoresist.¹⁹

For all the sputter reactions, the energy dependence of the etching yield by ions is assumed to increase as the square root of the ion energy²⁰ and the angular dependence of the physical and chemical etching yields were obtained from Ref. 21.

IV. MODEL CALIBRATION AND VALIDATION

Both the lithography and etch models were calibrated using the metrology data from various steps of the LE process. The

lithography model is critical due to the nature of the test structures, which includes features that print with the very similar ADI CD after the NTD photoresist development. These structures, however, were found to produce different etch biases through the etch processes of LE. A feature scale simulator that assumes an ideal resist profile (that is, uniform ADI CD throughout the photoresist height) cannot account for the etch bias differences for two structures with the same ADI CD; hence modeling a realistic photoresist sidewall profile is necessary. Also, accurately modeling the etch CD bias in the 3D tip-to-tip structure necessitates a rigorous lithography simulator.

A. Lithography model

PROLITH models were developed for each line pitch grating structure in Table II and calibrated using the ADI CD-SEM measurements. The lithography process was spatially uniform with a standard deviation in CD-SEM measurements across all dies less than 1 nm in the CDU wafer for every structure. The measurements from the center die of the CDU wafer were utilized for calibration.

The photoresist profile simulated in PROLITH for the A1 feature and the corresponding XSEM image is shown in Fig. 3. The ADI CD measurement of 38 nm from PROLITH is taken 8 nm above the SOG layer and matches the CD-SEM reported value of 38.6 nm. (Note that CD-SEM measurement only provides the information in the XY plane. The exact location along the height of PR is not known. The location of the measurement varies depending on the line/pitch dimensions of the feature.) Further, the predicted PR profile indicates both corner rounding at the top and a footer at the SOG interface, which qualitatively matches the profiles as seen in the XSEM.

PR profiles from PROLITH for the remaining test structures are shown in Fig. 4. The calculated ADI CD reported in the figure matches the experimental values within 1 nm. Note the variation in sidewall profile across the structures, especially between P400 and P168 structures [Figs. 4(d) and 4(e)], which have the same ADI

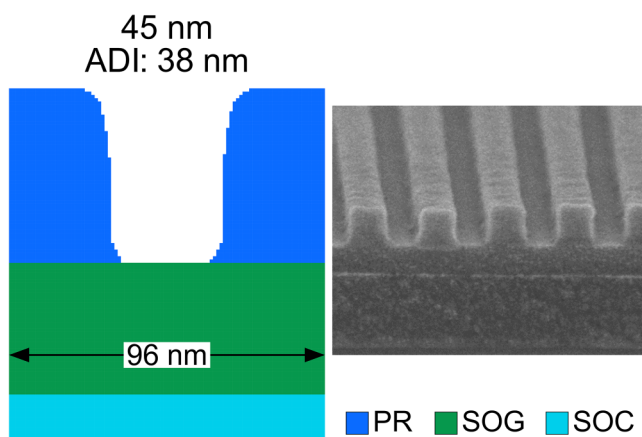


FIG. 3. Photoresist profiles for A1 features and corresponding cross-sectional SEM image from the experiment.

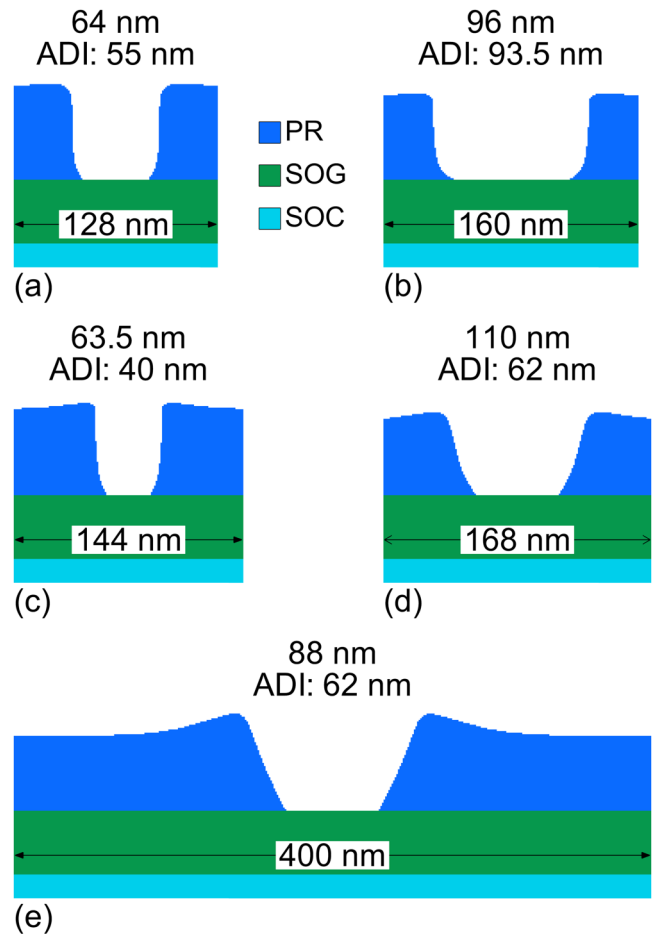


FIG. 4. Simulated photoresist profiles for different test structures. Pitch, photo-mask CD and measured ADI CD for the structures are (a) 128, 64, 55, (b) 160, 96, 93.5, (c) 144, 63.5, 40, (d) 168, 110, 62, and (e) 400, 88, 62. All measurements are in nm.

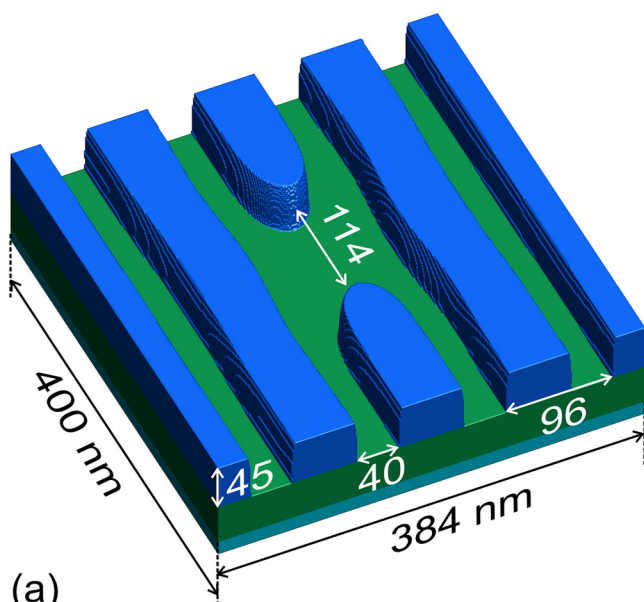
CD. However, as will be shown later, these two structures are etched with different etch biases.

The PR profile for the tip-to-tip feature is shown in Fig. 5 and is characterized by a tip-to-tip measurement of 113.4 nm versus 114 nm in PROLITH. Two regions in the feature: cut-line and trench, are labeled in Fig. 5(b). These regions are expected to differ in their etching characteristics during the various etch steps. The sidewall profile of PR in the trench regions shows a similar slope and footer as that of the A1 feature, and the photoresist height is approximately 45 nm.

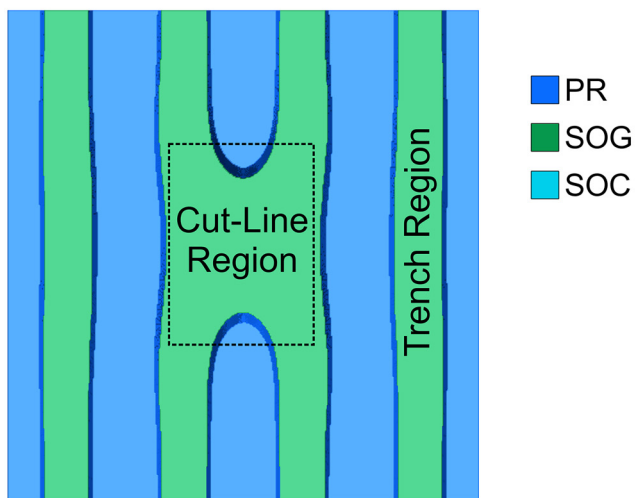
B. Etch model

ProETCH models for surface mechanism and the corresponding plasma properties were similarly calibrated to match the CD-SEM measurements after every etch step. Each model contains several internal parameters that are difficult to measure

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(a)



(b)

FIG. 5. Photoresist profiles predicted by PROLITH for the tip-to-tip feature. (a) 3D view. (b) Top-down view. All dimensions are in nm.

experimentally, such as plasma species properties (fluxes, ion energy, and angular distributions) and surface reaction kinetic parameters (such as sticking coefficients and ion incident angle resolved sputtering yields). To avoid overfitting and ensure predictability, only a subset of the line pitch structures were utilized for calibration and are summarized in Table III.

Experimentally, the within wafer CD uniformity is less than 10% for each etch step. This variation in CD is driven, in large part, by the variation in ion and neutral flux distribution in the chamber due to the asymmetric architectural elements (such as the

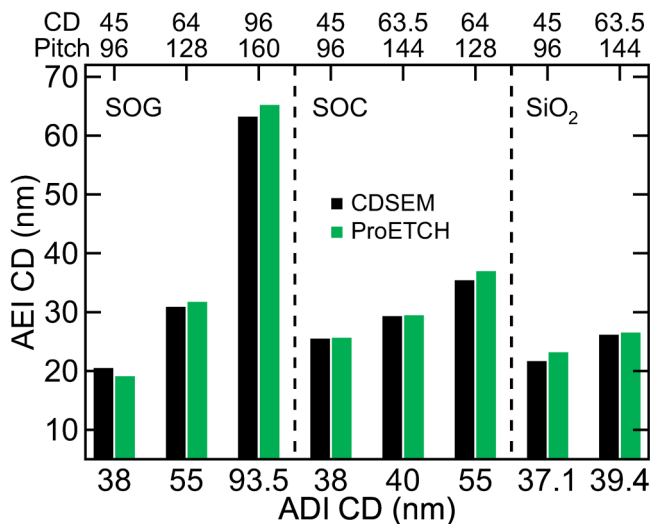


FIG. 6. Calibration results for the ProETCH model across different etch steps.

one-sided pump port). Similar to the calibration of the resist profile, measurements from the center die of the CDU wafer were used, and therefore, the calibrated fluxes and IEADs represent the value at the wafer center. The experimentally measured and calibrated CDs for each etch step are shown in Fig. 6. Error in the calibration is quantified using the root mean squared (RMS) error between experimental measurements and model-generated values. The RMS error in the AEI CDs for the SOG, SOC, and SiO₂ etches is 1.1, 0.9, and 1.0 nm, respectively, which is within 10% of the experimental data. Note that the CD generally decreases (relative to the pre-etch profile CD) for both the SOG and SiO₂ etch but increases for the SOC etch. The variation in etch bias across these steps will be discussed in detail in Sec. V.

The etch model is validated using the measurements from the FEM wafer. In particular, the variation of the AEI CDs for A1 and A2 with varying exposure doses was used for validation. For NTD photoresist materials, variation in exposure dose results primarily in a change in ADI CD, while the photoresist profile does not change dramatically across the explored exposure doses. Accordingly, the photoresist sidewall shapes from PROLITH simulations for A1 and A2 were kept the same, and a constant offset was applied to edges to modify the ADI CDs. The choice of voxel size of 1 nm for ProETCH simulations limited us from utilizing the exact ADI CDs from the FEM wafer. The experimentally measured and model-predicted CDs for each etch step are shown in Fig. 7.

TABLE III. ProETCH calibration data.

Etch step	Structure
SOG	A1, P128, and P160
SOC	A1, A2, and P128
SiO ₂	A1 and A2

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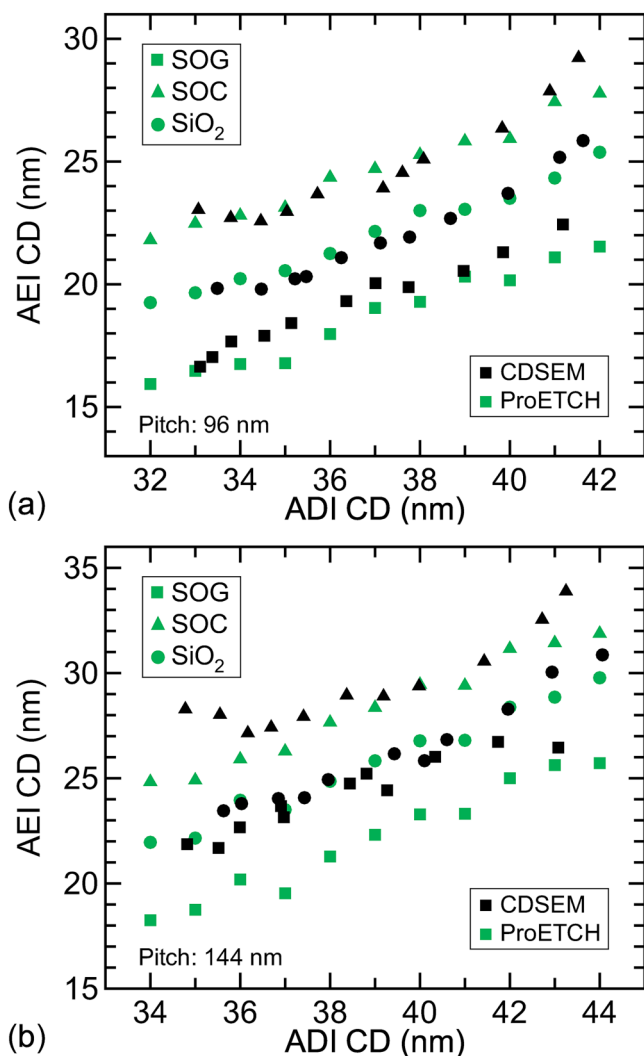


FIG. 7. Verification results for the ProETCH model across different etch steps. Results are shown for two structures: (a) A1 structure which has a pitch 96 nm and nominal ADI CD of 38 nm and (b) A2 structure which has a pitch of 144 nm and nominal ADI CD of 40 nm.

The model accurately captures the mostly linear relationship between the ADI and AEI CDs for each etch process. The RMS error in the AEI CDs for A1 is 0.9, 0.8, and 0.6 nm following the SOG, SOC, and SiO₂ etches. As such, the CDs are within 10% of the experimental data. Similarly, the RMS errors in the AEI CDs for A2 are 2.6, 1.5, and 0.6 nm, with the simulated CDs being within 20% of the experimental measurements. The error between the model and experiments in this data set is attributed to the assumption of a constant PR sidewall profile shape across varying doses. Recall that the measurement points for different doses in the FEM wafer are obtained from different dies on the wafer. Since the plasma properties in the calibrated model represent the values at

the center die, AEI predictions for data points that are away from the center of the wafer additionally incur errors due to the radial nonuniformity of plasma properties across the wafer, which is commonly observed in CCP plasmas.^{22,23}

V. EVOLUTION OF ETCH BIAS ACROSS ETCH STEPS

For multi-patterning etch processes, the final etch bias, defined as the difference between a feature's CD after lithography (ADI) and after the multiple etches (AEI), often evolves non-linearly, exacerbating the process development challenge. For example, the evolution of etch bias for the A1 and A2 features through the different etch steps of the LE process is shown in Fig. 8. Note that the etch bias evolution is reasonably independent of the line-pitch grating dimensions of the feature. The etch bias evolves non-linearly, and most of the final etch bias is introduced through the etch of SOG (17–20 nm) but decreases to 10–13 nm after the etch of the SOC layer, indicating that the profile in SOG is highly tapered, while it might have a retrograde shape or a bowed shape in SOC. The etch of SiO₂ is slightly tapered, resulting in an increase of etch bias by 3–4 nm. These non-linearities present process development challenges since the chamber level nonuniformities interspersed with the pattern complexity can be difficult to co-optimize. The primary cause for the etch bias across each step and possible ways to modulate the bias is discussed in the next section.

A. SOG-etch

The evolution of the etching profile in SOG layer for the nominal A1 structure (ADI CD: 38 nm) from ProETCH is shown in Fig. 9. The model predicts the etch to land on the underlayer at about 30 s with a bottom CD of approximately 15 nm. The

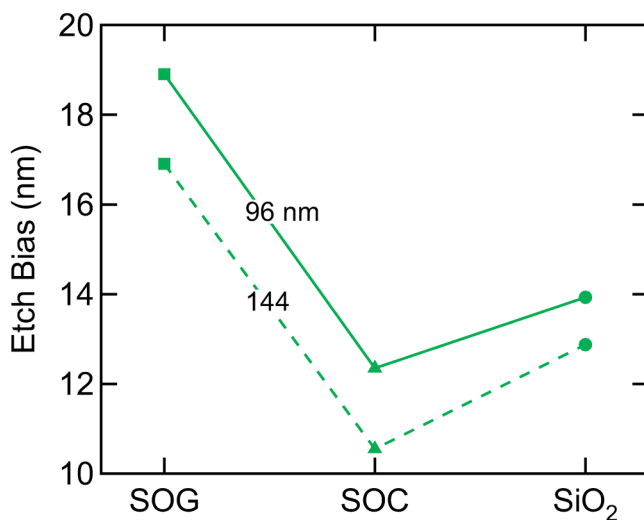


FIG. 8. Evolution of etch bias over different etch steps for the 96 nm pitch and 144 nm pitch line-space structures. After the lithography step, both structures print with approximately 40 nm trench ADI CD.

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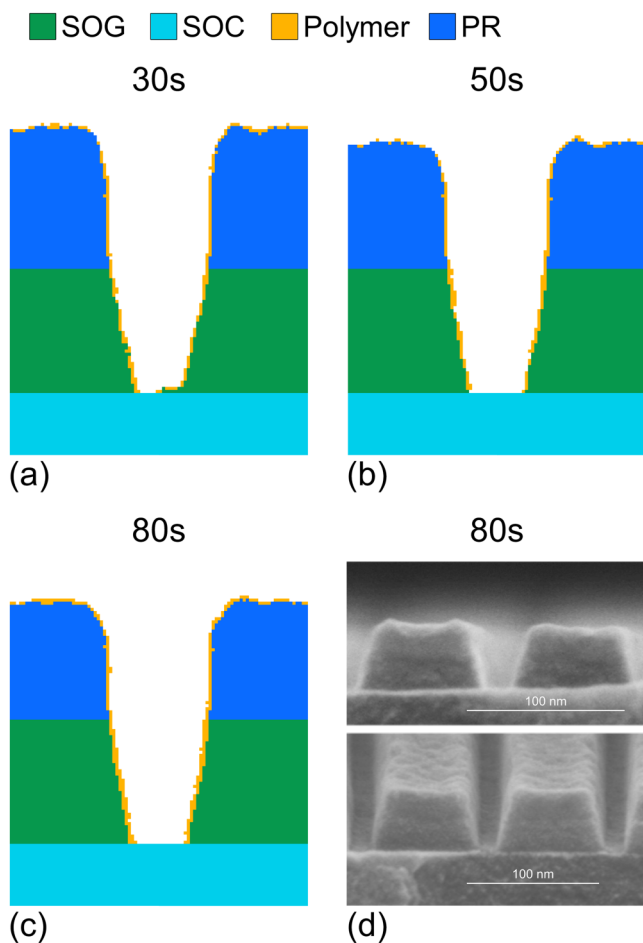


FIG. 9. Etching profile of A1 feature during the SOG-etch. (a) Simulated profile at 30 s, (b) Simulated profile after the end of the main-etch phase (50 s), (c) Simulated profile after the end of the over-etch phase (80 s), (d) Cross-sectional SEM image after the end of the over-etch phase.

subsequent main etch phase induces lateral etching in SOG, increasing the bottom CD to 18 nm. There is a marginal change in the SOG profile during the over-etch phase, indicating a balance between the deposition and the removal process. The post-etch CD for this feature predicted by the model is 19.1 nm which compares well with the CDSEM measurement of 20.5 nm. Concurrently, the change in photoresist thickness during the main and over-etch phases is small, as shown in Figs. 9(b) and 9(c), indicating an overall selectivity of 2.5. The model predicted profile in SOG compares well with the XSEM image from the experiments, as shown in Fig. 9(d). Profile attributes, such as photoresist thickness loss and the sidewall slope, are well-reproduced by the model.

The etch of SOG proceeds through the formation of a polymer overlayer via the polymerizing radicals from the plasma. The presence of the polymer layer on top of both the photoresist and SOG layer is evident in the simulated profiles. The thickness of

the polymer layer predicted by the model is less than 2 nm during the entire process. While the polymer can be removed both thermally and by physical sputtering, the calibrated kinetic parameters indicate that thermal etching is the dominant mechanism of polymer removal (70%), as has also been reported in experimental studies previously.^{24,25} The profile simulated by ProETCH shows a significant sidewall taper which occurs due to the passivation of the sidewall by the polymerizing radicals. Passivating species depositing on the sidewalls tend to reduce the CD at the etch front. As the etch progresses this continual deposition process leads to a continual reduction of the CD at the etch front, resulting in a tapered profile.

The profile evolution of SOG in the tip-to-tip feature at 30, 50, and 80 s (see Fig. 2 for photomask layout and Fig. 5 for pre-etch profile) is shown in Fig. 10. The salient features of the profile observed in the A1 structure like the tapered sidewalls, selectivity to photoresist, and the polymer layer formation is also predicted for this feature. Additionally, the model predicted profile shows spatial nonuniformity in the etch rate of this feature. The etch progresses slower in the lower aspect ratio cut-line region than in the higher aspect ratio trench region. This nonuniformity is evident from the observation that at 40 s, the etch is fully open to the underlayer in the trench region, while there is about 10 nm of unetched material in the cut-line region. The unetched material in this region is subsequently etched away during the remainder of the main-etch and over-etch phases, with a trace amount of material remaining after the end of the process [see Fig. 10(c)]. The presence of unetched material can lead to CDSEM measurement failures, which was indeed the case for our experiment. Further, any unetched material can potentially lead to defects in the subsequent etch steps due to selectivity differences.²⁶

The difference in the etch rate between the cut-line and trench region arises due to the neutral conductance effect in the transport of the polymerizing radical species in the plasma. In the cut-line region, the lower aspect ratio facilitates higher view angles to the plasma resulting in higher incidences of the isotropic flux of polymerizing radicals. Commensurate to this flux increase, the extent of polymer deposition is relatively larger at the etch front in the cut-line region. The SOG etch recipe operates in conditions where the deposited polymer acts as an etch suppressant instead of accelerating the etch through chemical sputtering.²⁴ Since the lower AR regions in the feature experience a higher etch rate, the opposite of traditional aspect ratio dependent etching (ARDE) scaling^{27–29} this phenomenon is called inverse ARDE. Inverse ARDE in the etching of dielectric materials has been experimentally observed earlier.³⁰

The tapered sidewalls, characteristic of the profiles in the SOG etch step, manifest into a significant positive etch bias. As mentioned earlier, this tapering is induced due to the surface interaction of polymerizing radicals from the plasma with the sidewalls of the SOG layer. The impact of the polymerization rate on the profile taper was investigated by reducing the rate of polymerization in the model to 50%. The corresponding etch profile of the A1 feature is compared to the baseline polymerization rate, and the results are shown in Fig. 11. The profiles are compared at 30 s and not at the end of the process so that the results are not confounded by the lateral etching once the SOC layer is opened. The model predicts a decrease in the sidewall slope from 13° in the baseline case to 5° in

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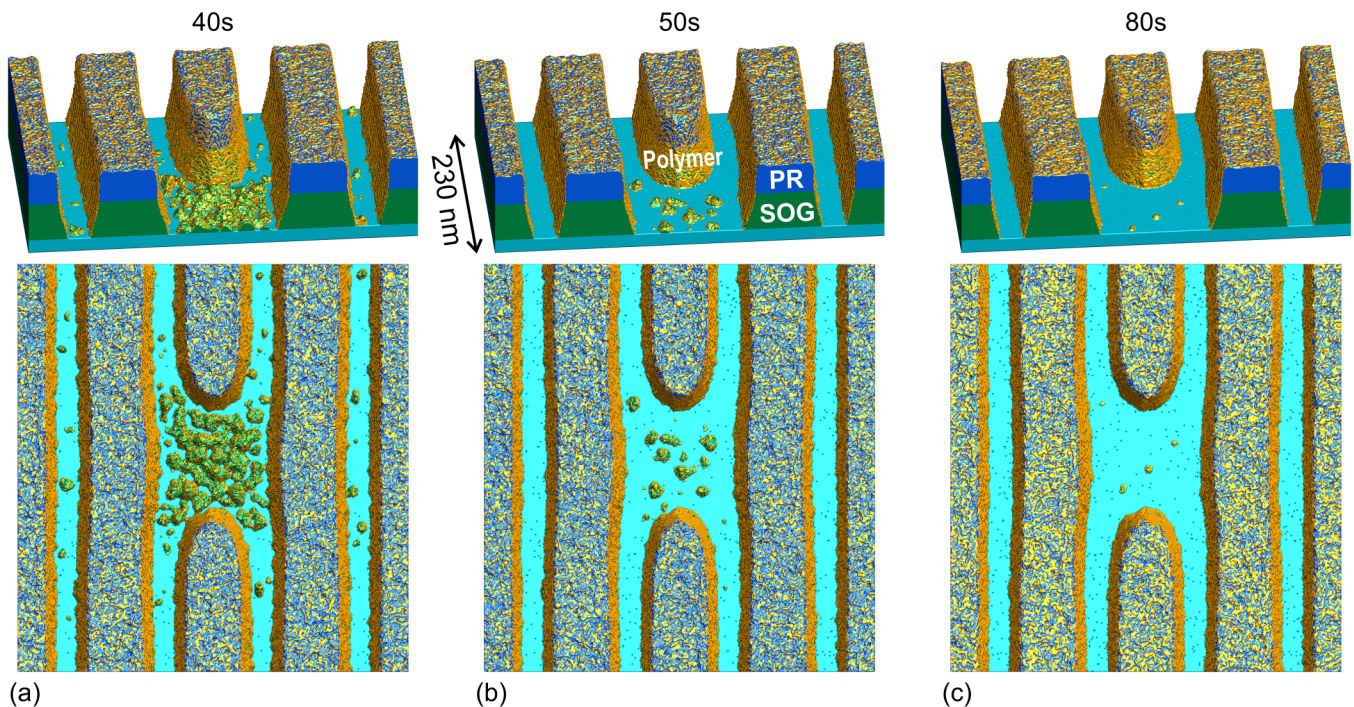


FIG. 10. Simulated etch profile for the tip-to-tip feature during the SOG-etch process at (a) 40 s, (b) end of main-etch phase—50 s, (c) end of over-etch phase—80 s.

the reduced polymerization case. The taper reduces because, with lesser polymerization rates, the extent of passivation occurring in the sidewalls of SOG reduces, causing less reduction of CD as the etch progresses. The apparent increase of etch depth in the full passivation

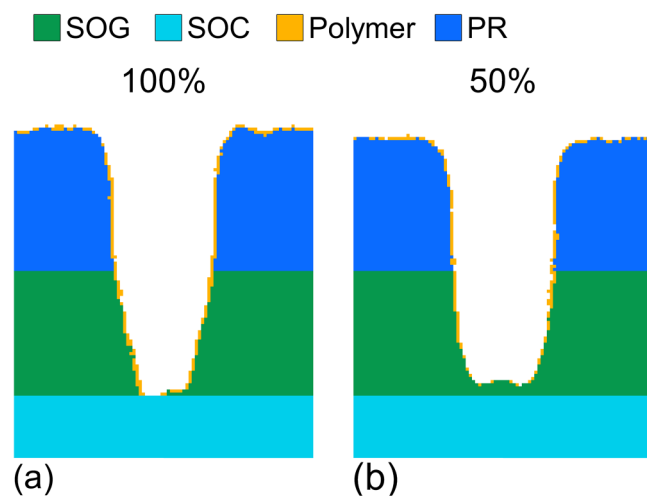


FIG. 11. Effect of polymerization on the sidewall slope of the profile during SOG-etch. (a) Simulated profile at 30 s for the baseline case. (b) Simulated profile at 30 s for reduced polymerization rates.

case may seem at odds with the inverse ARDE trend but is slightly misleading. Both cases have a similar total amount of material removed, since the CD is larger for the lower passivation case. Another side effect of this parameterization is the slight increase in the photoresist etch rate, attributed to the smaller polymer thickness on the photoresist layer. Overall, the polymer layer acts as an etch suppressant in the operating conditions of this process, and in general, the lesser the polymerization, the higher the etching rate.

The rate of polymer deposition and consequently the sidewall slope (or the etch bias) during the SOG etch step can alternatively be modulated by the neutral-to-ion flux ratio from the plasma. The impact of the neutral-to-ion flux ratio was investigated by varying the neutral flux and maintaining a constant ion flux. The simulated etch profiles of the A1 feature at 30 s are shown in Fig. 12 for varying flux ratios of 3.2 (baseline value), 2.7 (15% lower) and 2.1 (34% lower). Decreasing the flux ratio results in a slight decrease in etch rate of SOG [compare the etch depth in Figs. 12(a) and 12(c).] due to reduced polymerization at the etch front. The average sidewall slope decreases from 13° to 6° when the flux ratio is 34% lower, and the conditions are radical flux-limited. The model predicts the SOG etch bias at the end of the process (80 s) to decrease by around 20% from the baseline value of 18.9–14.8 nm when the flux ratio is reduced by 15%. Interestingly, the experimental variation in the SOG etch bias across the different dies of the CDU wafer was around 10%. This indicates that the neutral-to-ion flux ratio in the actual process varies significantly lesser than 15% across the wafer. We note that by comparing the model and

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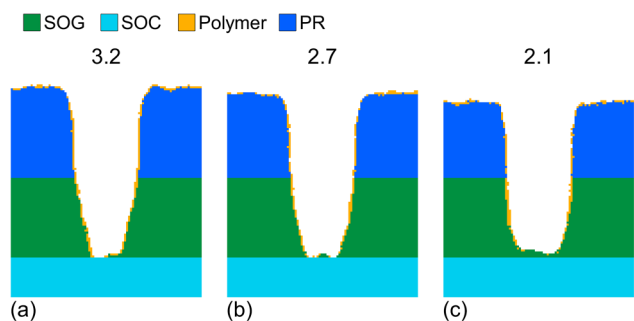


FIG. 12. Effect of neutral to ion flux ratio on SOG-etch bias. Simulated profiles for neutral to ion ratio of (a) 3.2, (b) 2.7, (c) 2.1.

experimental etch biases at different dies, one can map out the flux distribution over the wafer, which will be considered in future work.

B. SOC-etch

Recall that the etch bias for the A1 structure decreases between the SOG and SOC etch by nearly 50% (see Fig. 8). To understand the origin of this negative etch bias, or CD increase, the simulated profiles are shown in Fig. 13 at various instances of the process following the baseline SOG etch profile shown in Fig. 9(c). The photoresist is etched rapidly in the H_2/N_2 plasma during the early transients and is entirely removed in 40 s (not shown in the figure). The removal is facilitated primarily due to the thermal etch by H radicals, and the isotropic thermal etch process is well captured by the model, as shown in Fig. 13(a), where the CD in the photoresist region is significantly larger than the CDs in the rest of the stack. Upon photoresist clearance, the SOG layer provides the necessary selectivity for the remainder of the process, where it is primarily removed due to physical sputtering by the energetic ion bombardment. At the end of the process, ~30 nm of SOG remains, indicating a selectivity of 10 to SOC. For the A1 structure, the etch is predicted to land on the underlying SiO_2 at around 130 s; therefore, the process has minimal over-etch time, which helps minimize any significant punch through of SiO_2 .

The presence of tapered sidewalls in the SOG layer introduces profile variation through the SOC stack. As shown in Fig. 13(c), there is some undercut and bow in the SOC layer due to lateral etching. The energetic ions from the plasma undergo specular reflections from the tapered SOG sidewalls and hit the SOC layer at slightly oblique angles to induce lateral etching. Recall that the SOC etch proceeds by successive hydrogenation and ion sputtering of the HCN and CH_x sites. We investigated the surface site composition on the SOC layer and found that HCN accounts for ~70% of the surface site composition. This increase in CD ultimately accounts for the negative etch bias during the SOC etch process.

The corresponding evolution of profile in SOC for the tip-to-tip feature is shown in Figs. 14 and 15. The unetched SOG material in the cut-line region from the previous process [see Fig. 10(c)] acts as a micromask which leads to the formation of pillarlike features during the early transients of the process, as shown

in Fig. 14(a) and evident in the 20 s contour line in Fig. 15. Once the residual SOG materials on these pillar features are etched away by physical sputter, the pillar's height begins to reduce, and the etching surface recovers local conformality. Contrary to the SOG-etch, the model predicts a higher etch rate in the cut-line relative to the trench region during the SOC-etch. This outcome is evident in Fig. 14(c) which shows the simulated profile at 110 s, where the etch is opened to the underlayer only in the cut-line region. The nonuniform etch rate is also evidently visible from the 100 s contour line in Fig. 15. This nonuniformity in etch rate is caused by the ARDE effect, where the fluxes of H and N radicals arriving at the etch-front in the cut-line region are higher than in the trench region because of larger view angles to the plasma in the cut-line region. Overall, the H and N radicals passivate the etch front and enhance the etch rate compared to the bare SOC sites. Consequently, the etch rate is higher in regions where the local fluxes of H and N are relatively higher. During the remainder of the process, the etch front progresses in the other regions in the feature, and by the end, the underlayer is open everywhere. The model predicted tip-to-tip CD at 150 s is 98.75 nm which is within 10% of the top-down SEM measurement of 106.4 nm.

Hydrogen and Nitrogen radicals play contrasting roles in the etch of SOC. The H radicals serve as etch-enhancer through the passivation and thermal etching pathways, while the N radicals are etch-inhibiting due to the formation of the hard CN surface sites, which can be removed only by physical sputtering. Sputter removal of CN sites also generates gaseous CN by-products, which readily get redeposited on the surface. As a result, the ratio of H-to-N

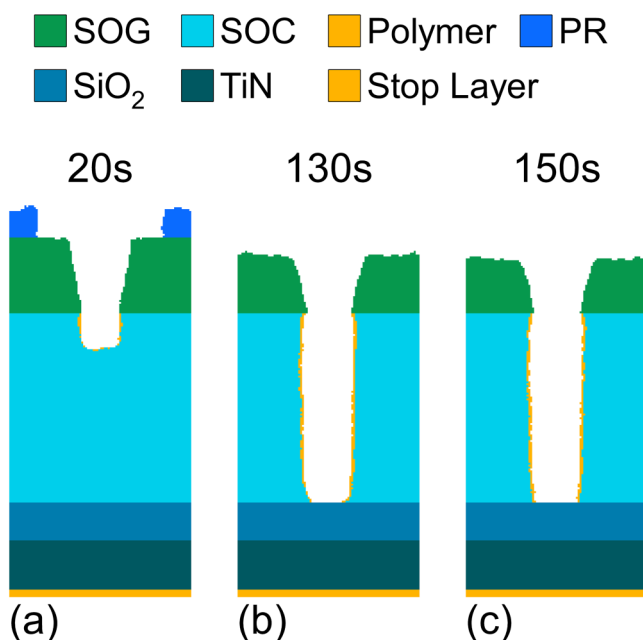


FIG. 13. Simulated profile of A1 features during the SOC-etch process. Profile at (a) 20 s, (b) 130 s, (c) 150 s—end of the process.

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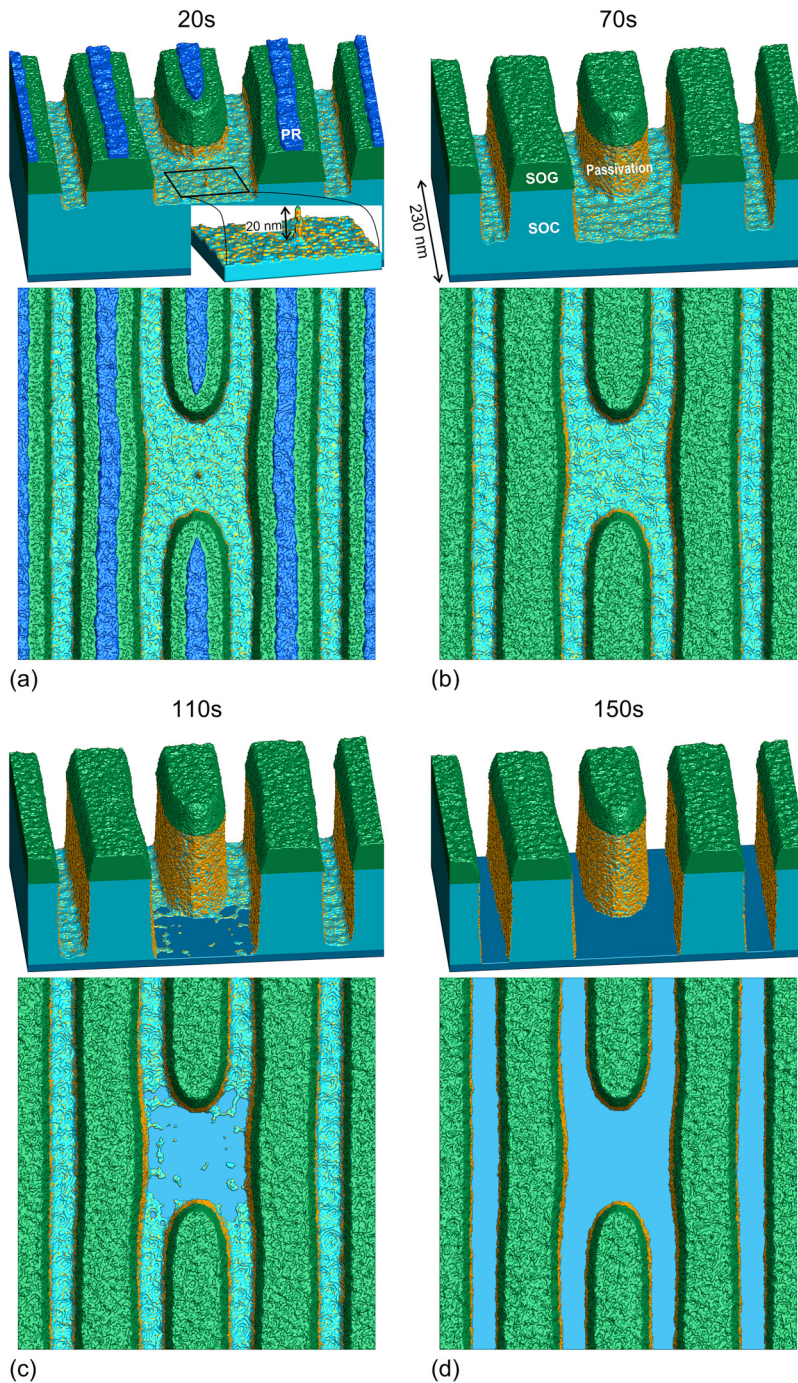


FIG. 14. Simulated profile of the tip-to-tip feature during the SOC-etch process. Profiles are shown at (a) 20 s, (b) 70 s, (c) 110 s, and (d) 150 s—end of the process.

radicals is a critical parameter that governs the etch profile in SOC and, by extension, the etch bias in the process. The impact of the H-to-N flux ratio on the etch profile at 110 s is shown in Fig. 16. The profile is characterized by tapered sidewalls in the N-rich regime. The taper is attributed to the dominant presence of CN sites on the etch front, which results in significant redeposition

upon sputter removal. The extent of CN coverage is reduced when the H-to-N flux ratio increases as most sites get converted to HCN, which can be etched with a very low sputter threshold due to the formation of stable HCN gas. Also, the bare SOC sites are increasingly hydrogenated to form the CH_x sites that are eventually thermally etched. These effects result in an etch that proceeds

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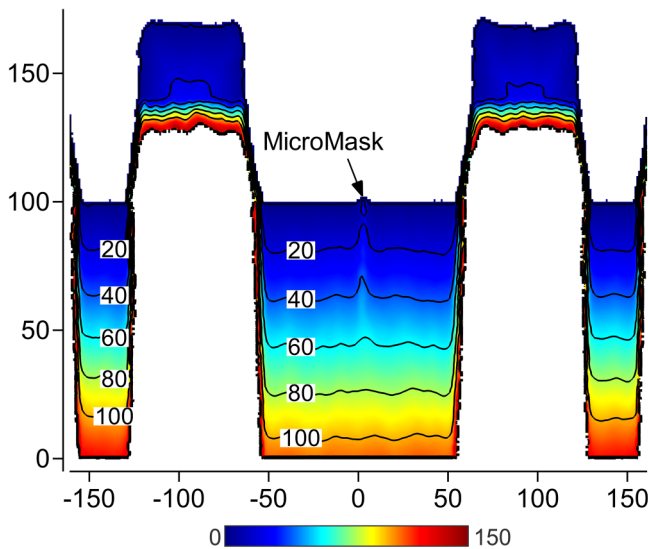


FIG. 15. Slice view of the simulated profile of the tip-to-tip feature demonstrating the etch contour evolution during the SOC-etch process. The slice is taken at the middle of the cut-line region spanning in the horizontal direction.

significantly faster both laterally and vertically. For comparison, the etch opens to the underlayer in 200, 150, and 110 s, as the H-to-N flux ratio increases. Correspondingly, the bottom CDs increase from 14.9 to 26.8 nm, modulating the etch bias from positive to negative values. This effect of increasing etch rate with higher hydrogen in feedstock composition has been previously reported.³¹

C. SiO₂ etch and pattern transfer

The final etch in the multistep LE process is that of SiO₂. The oxide etch process results in a moderate change in etch bias (relative to SOG and SOC). This is attributed to the process recipe, which operates in a low neutral-to-ion flux ratio (compared to the baseline SOG etch process.) The simulated profile for the baseline process is shown in Fig. 17. The etch profile exhibits minimal taper since the extent of polymerization is significantly reduced, following the trends discussed earlier in Fig. 12. Due to the nature of the material similarities between SOG and SiO₂, etch rate of SOG is fairly high, and the model predicts the SOG to be entirely consumed at around 100 s. The remaining etch proceeds with SOC as the hardmask with minimal loss to its thickness.

As mentioned earlier, the SiO₂ layer is present in the material stack to enable multiple passes of the LE³ process, where the final patterns are printed on the TiN layer. The TiN etch occurs only after the third pass of the LE³ process, where the patterns present in the SiO₂ layer are transferred. After each of the three SiO₂-etches, the SOC is stripped away using an oxygen plasma, which is highly selective to SiO₂, and the etch bias during the process is nonexistent. Following the SOC-strip, the spin-on

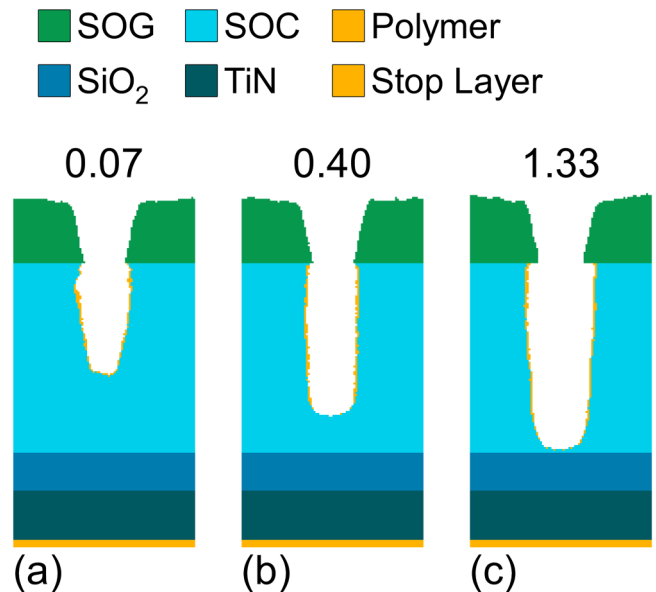


FIG. 16. Effect of H-to-N flux ratio on SOC etch profile. Simulated profiles for H-to-N ratio of (a) 0.07, (b) 0.4, (c) 1.33. Profiles are shown at 110 s.

hardmask layers are redeposited, and the second pass of the LE³ process is initiated. After all three litho-etch steps are completed, the SiO₂ serves as a hardmask to transfer into the TiN layer. Finally, TiN will be used as a mask to pattern the underlying high-k dielectric, which will then be metallized via a Damascene process to form the desired metal circuit pattern.

VI. ROLE OF PHOTORESIST SHAPE ON ACCURATE ETCH MODEL PREDICTIONS

Multi-patterning processes rely on the evolution of etch bias through each etch step to realize the design target CD. We have demonstrated that the etch steps can be accurately modeled to virtually aid the process design. In the LE process investigated here, the final etch bias is dominantly driven by the etch bias induced during the etching of SOG layer. Due to a variety of patterns on a typical logic cell, accuracy of the etch model predictions significantly depends on the initial PR profile (not limited to CD). To illustrate the importance of the PR profiles, the etch model was calibrated for the line-pitch grating structures shown in Table I using two different types of PR profiles. The first set of PR profiles was obtained from PROLITH, while the second set of PR profiles was assumed to be idealized (that is, without any CD variation through its thickness) with the constant CD corresponding to the CDSEM measurements. The calculated and measured AEI CD after the SOG etch for the various calibration features is shown in Fig. 18(a). The calibration error is low for both the etch models, with an RMS error of 0.9 nm for idealized and 1.5 nm for PROLITH profiles.

The calibrated model was then utilized to predict the AEI CD for the remaining line pitch grating features, and the results are

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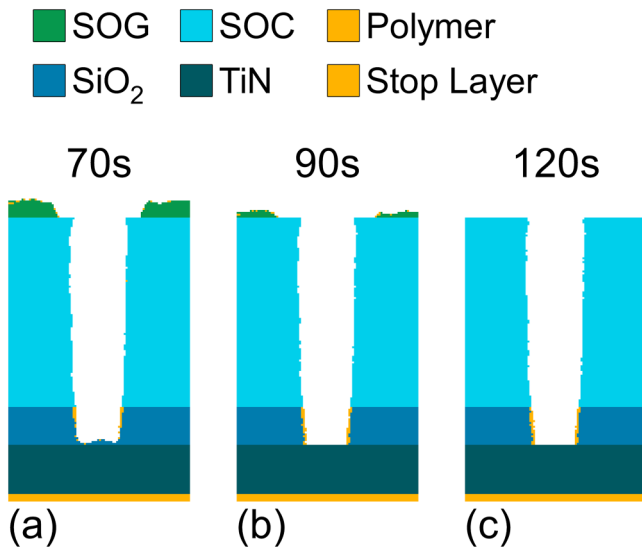


FIG. 17. Simulated profile of A1 features during the SiO₂-etch process. Profiles are shown at (a) 70 s, (b) 90 s and (c) 120 s—end of the process.

shown in Fig. 18(b). The lack of predictive accuracy for the model corresponding to the idealized PR profile is evident. The RMS error for the idealized profiles is 7.8 nm, while for the profiles from PROLITH is 1.8 nm. The etch model corresponding to the idealized PR profiles is particularly limited by features with similar ADI CD despite their photomask CD and pitch differences. The nature of the lithography development process and the pitch variation introduces significant PR profile attributes such as sidewall slope, footing, and top corner rounding (e.g., shown in Fig. 4), which strongly influence the etch process.

VII. SUMMARY AND CONCLUSIONS

Lithography and dry etch process in a multi-patterning flow used in a test vehicle for BEOL manufacturing were investigated using experiments and computational models. The etch processes comprised multiple steps to etch the trilayer hardmask (photoresist, SOG, and SOC) and the underlying SiO₂. The models were calibrated using top-down SEM and cross-sectional SEM measurements. Calibration and verification errors in the calculated CDs at AEI for the targeted line pitch grating features and a three-dimensional tip-to-tip test feature were within 10% of the experimental measurements. The simulations also qualitatively agreed well with other profile attributes such as sidewall slope in the etched features. The etching of the SOG layer generated a highly tapered etch front because of polymerization by the fluorocarbon radicals, which resulted in a significant etch bias. The final etch bias between lithography and the multiple etch steps originated primarily during the etching of SOG layer. The extent of polymerization during this step, and hence the etch bias, can be modulated by controlling the neutral-to-ion flux ratio in the plasma. The model predicted a 20% reduction in the etch bias when the flux ratio was reduced by 15%. On the other hand, the SOC etch step generated a

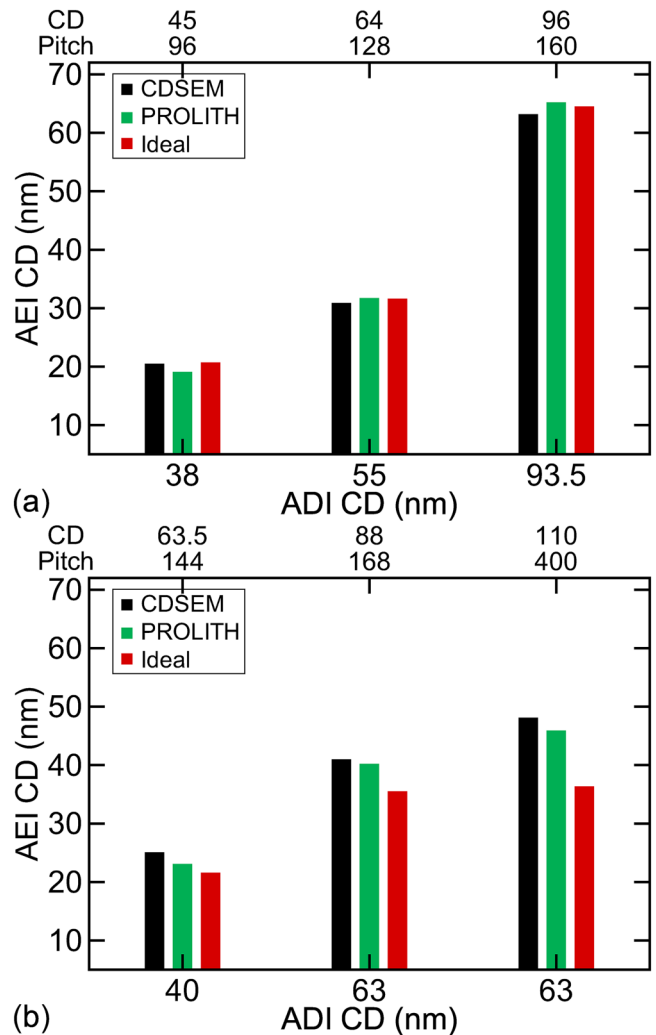


FIG. 18. Comparison of ProETCH calibration and predictions using idealized and PROLITH photoresist profiles. Measured and calculated CDs are shown for (a) calibration features and (b) verification features.

slightly bowed profile, thereby decreasing the cumulative etch bias. The ratio of hydrogen to nitrogen radicals was shown as an effective knob to control the etch bias during this step, with the model predicting a tapered sidewall profile in the hydrogen starved regime and a bowed profile in the hydrogen-rich regime. Simulations also show a nonconformal etch front evolution in the tip-to-tip feature during the SOG and SOC etch steps. This phenomenon occurs because of aspect ratio dependent etching effects. The SOG etch step exhibited an inverse ARDE scaling with high aspect ratio regions etching at a lower rate, while the SOC etch step showed a conventional ARDE scaling. The final etch step, where patterns are transferred into the SiO₂ layer, produced an insignificant etch bias because of the low neutral-to-ion flux ratio in the plasma. Finally,

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the importance of accurate photoresist sidewall shapes toward the accuracy of the etch models was demonstrated. Etch models that assumed an ideal photoresist shape with no realistic profile attributes such as sidewall slope and footer suffered from significant prediction errors. An extension of this work is to demonstrate how these models can be utilized to effectively identify conditions to address hotspots on the wafer and is a subject of future publication.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts of interest to disclose.

Author Contributions

Prem Panneerchelvam: Conceptualization (equal); Data curation (lead); Formal analysis (lead); Investigation (lead) Methodology (lead); Validation (equal); Visualization (lead) Writing – original draft (lead). **Ankur Agarwal:** Conceptualization (equal); Methodology (equal); Project administration (equal); Visualization (lead); Writing – review & editing (equal); Chad Huard: Methodology (equal); Conceptualization (equal); Formal analysis (equal); Methodology (lead); Writing – review & editing (equal). **Alessandro Vaglio Pret:** Methodology (equal); Data curation (equal); Formal analysis (equal). **Antonio Mani:** Methodology (equal); Data curation (equal). **Roel Gronheid:** Methodology (equal); Data curation (equal). **Marc Demand:** Methodology (equal); Data curation (equal). **Kaushik Kumar:** Methodology (equal); Data curation (equal). **Sara Paolillo:** Methodology (equal). **Frederic Lazzarino:** Methodology (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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