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RESEARCH ARTICLE

Investigation of DC Characteristics Degradation in Silicon Nanosheet FET Due to Interface Traps

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ABSTRACT Nanosheet field-effect transistors (NS FETs) utilizing the gate-all-around (GAA) architecture have emerged as the primary alternative to tri-gate FinFETs. However, several technical issues arise in the fabrication of NS FETs, with interface trap states being a critical concern. These traps primarily originate from defects at the Si/SiO_2 interface during O_3 treatment prior to interlayer formation. As NS FETs transition toward higher numbers of vertically stacked nanosheets to enhance performance, the impact of these interface traps becomes increasingly significant. In this study, we investigate the influence of two distinct types of interface traps—donor-like and acceptor-like—on the DC characteristics of NS FETs. We systematically evaluate the sensitivity of electrical parameters to trap configurations and provide a guideline for optimizing cutting-edge nanosheet device technologies.

INDEX TERMS DC performance, interface trap, neutral trap, acceptor-like trap, donor-like trap, gate-all-around field-effect transistor (GAA FET), nanosheet (NS) FET, technology computer-aided design (TCAD).

I. INTRODUCTION

The performance of integrated circuit (IC) chips has been improved, achieving higher computing speed and lower power consumption, through the scaling of silicon devices [1]. However, decades of continuous device scaling have led to reduced gate controllability and increased static power consumption due to short-channel effects (SCEs). As a result, considerable efforts have been made to suppress SCEs [2], [3]. In this context, silicon device architectures have evolved from two-dimensional (2-D) planar field-effect transistors (FETs) to three-dimensional (3-D) Tri-gate FinFETs [4], [5]. This evolution enhances gate controllability by increasing the gate oxide capacitance (C_{OX}) through an expanded gate–channel interface area under limited design rules. As device scaling advanced to technology nodes below 3 nm, nanosheet (NS) FET architectures based on the gate-all-around (GAA) structure were introduced as alternatives to Tri-gate FinFETs and have been in mass production since 2022 [6].

However, the NS FET fabrication process is significantly more challenging than that of FinFETs. The increased complexity originates from the GAA structure, which requires the formation of multiple suspended silicon nanosheets and the subsequent filling of gate dielectrics and metal gates between vertically stacked nanosheets [7], [8], [9].

One of the particular challenges is the increased surface roughness of the nanosheet surface and the formation of interface traps at this surface. Control of this surface roughness is closely related to the iterative Si/SiGe epitaxial growth process, which requires the careful consideration of both Ge interlayer interdiffusion and dry-etching selectivity [10], [11], [12], [13].

It is evident that increased surface roughness of the nanosheet contributes to a higher interface trap density at the silicon nanosheet/silicon dioxide (SiO_2) interface.

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Among interface traps, neutral-type interface traps (hereafter referred to as neutral traps) are the most prevalent. Neutral traps correspond to energy states with zero net charge and can exist in both donor-like and acceptor-like configurations [14], [15], [16], [17]. The presence of neutral traps at the nanosheet/gate-dielectric interface can degrade device performance by degrading mobility and increasing scattering during carrier transport.

As a result, neutral traps can degrade the DC characteristics of NS FETs, resulting in threshold voltage (V_{TH}) mismatch, reductions in on-state current (I_{ON}) and transconductance (g_m), as well as degradation of off-state leakage current (I_{OFF}) and subthreshold swing (SS). However, despite the significant impact of neutral traps, analyses based on the energy and spatial distributions of both types of neutral traps in silicon NS FETs remain underexplored [17]. Furthermore, according to the IRDS 2024 roadmap, nanosheet FETs (NSFETs) are expected to incorporate an increased number of stacked nanosheets. Consequently, the management of interface traps becomes increasingly critical in determining device performance, reliability, and manufacturing yield [18]. Unlike conventional FETs such as planar FETs and FinFETs, NS FETs consist of vertically stacked multiple channels. Therefore, it is highly critical to analyze how interface traps affect each individual channel. However, despite the significance of multi-channel interface trap analysis, most previous studies have not sufficiently investigated these effects.

In this study, we comprehensively investigate the impact of both donor- and acceptor-like Si/SiO_2 interface traps on the electrical characteristics of multi-channel silicon NS FETs. We perform a comprehensive comparative analysis regarding the spatial distribution of traps by defining two distinct trap configurations at the silicon nanosheet/interlayer dielectric (IL) interface. Furthermore, to reflect realistic device conditions, the non-uniformity of interface traps across individual nanosheets is incorporated. Finally, a quantitative evaluation of trap-induced effects on device performance is conducted.

II. SIMULATION DETAILS

Fig. 1a shows a schematic view of the NS FETs investigated in this study. All simulations were conducted via technology computer-aided design (TCAD) simulations using the Synopsys Sentaurus tool [19], [20]. The gate length (L_G) and channel width (W_{CH}) were set to 12 nm and 45 nm, respectively. The gate dielectric stack consists of a SiO_2 interlayer (IL) and a HfO_2 high-k dielectric. The physical thicknesses of the SiO_2 (T_{OX}) and HfO_2(T_{HK}) layers were assumed to be 0.5 nm and 1.28 nm, respectively, resulting in an equivalent oxide thickness (EOT) of 0.7 nm [21], [22].

Furthermore, the nanosheet thickness (T_{CH}) and the vertical space between nanosheets (V_{SPC}) were defined as 5 nm and 10 nm, respectively. A 3-nm-thick inner spacer composed of Si_3N_4 was employed to account for the source/drain (S/D) extension regions. Finally, the punch-through stopper (PTS) doping concentration (N_{PTS}) in the silicon substrate was set to 1×10^{18} cm^{-3} to suppress substrate leakage current. The detailed device parameters used in this simulation are summarized in **Table 1**.

Fig. 1b shows the I_D-V_G characteristics, which were calibrated based on previously fabricated NS FETs [6]. The device modeling utilized Poisson equations and drift-diffusion models to account for carrier transport. To accurately represent nanoscale devices, quantum potential and thin-layer models were adopted. Furthermore, the Slotboom model was incorporated to account for bandgap narrowing effects at high-doping concentrations. Regarding recombination mechanisms, Auger, Shockley-Read-Hall (SRH), and Hurkx models were employed to consider band-to-band and trap-assisted tunneling. Lastly, the work function of the TiN metal gate was set to 4.48 eV to align with an I_{OFF} of 0.1 nA at 0 V, with all traps removed during calibration. Given that the simulated electrical characteristics closely match the experimental data from the fabricated device, it is reasonable to employ the aforementioned physical models and corresponding parameter values. Consequently, the NRMSE quantifies the normalized prediction error, with lower values indicating closer agreement with the experimental data. The coefficient of determination (R^2) denotes the proportion of variance in the fabricated data explained by the calibration framework. The extracted NRMSE and R^2 values are 0.0195 and 0.9964, respectively.

Fig. 2 illustrates the fabrication process flow of the n-type NS FET. (I) The process begins with a bulk silicon wafer featuring a retrograded PTS layer. Iterative epitaxial growth was conducted to stack multiple Si and SiGe layers. (II) Shallow trench isolation (STI) formation was performed to define the active regions. (III) A dummy poly-Si gate and outer spacers were deposited. (IV) The SiGe and Si layers were recessed at the S/D regions via dry etching, followed by a SiGe cavity etch using a selective SiGe trimming process. (V) Accordingly, SiN inner spacers were formed, an Si epitaxial growth was performed for source/drain formation. (VI) The silicon nanosheet channel release process was conducted by removing the dummy poly-Si and sacrificial SiGe layers. (VII) The gate dielectric stack, including the interfacial layer (IL) and high-k (HK) dielectric, was deposited. (VIII) Finally, the replacement metal gate (RMG) process with a work-function metal (TiN) was performed.

III. RESULTS AND DISCUSSION

At the silicon surface, the periodic lattice structure is abruptly terminated, resulting in the formation of silicon dangling bonds. Although most silicon dangling bonds are passivated during the thermal oxidation process, unpassivated dangling bonds, weakly bonded-oxygen, including distortion in bonded length and angle, oxygen vacancies, and defects induced during the nanosheet channel release process generate trap states at the Si/SiO_2 interface [15], [23], [24].

Fig. 3 illustrates the potential interface trap configurations for each silicon channel in the NS FETs. The interface traps are located in both the stacked nanosheet channels and the substrate-parasitic channel.

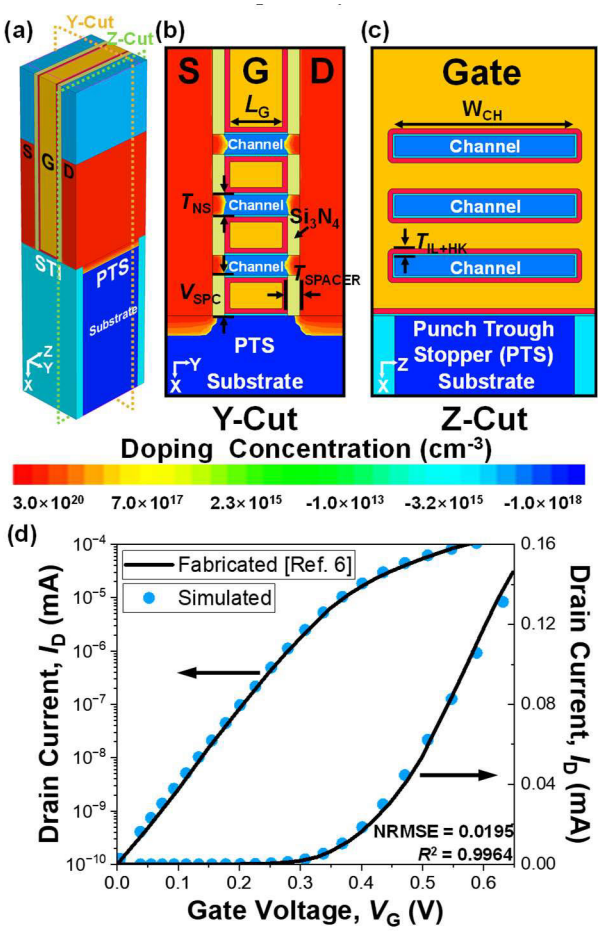


FIGURE 1. a) Schematic view of the simulated NS FET. Cross-sectional views along the (b) y- and (c) z-directions and (d). Calibrated I_D-V_G characteristics of the simulated NS FETs, validated against previously fabricated devices [6] with an NRMSE of 0.0195 and an R^2 of 0.9964.

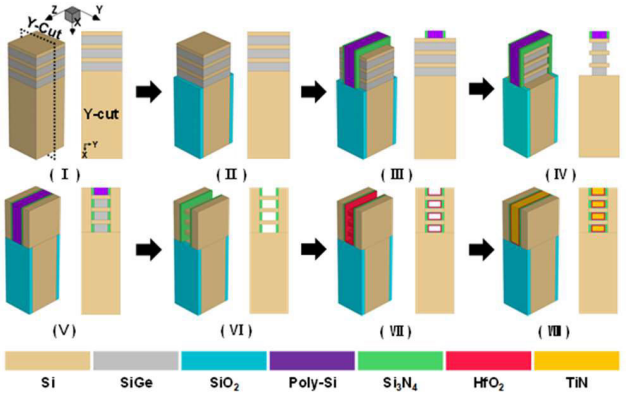


FIGURE 2. Schematic fabrication process flow for NS FETs.

Fig. 4 illustrates the distribution of D_{it} as a function of energy within the Si bandgap. To investigate position-dependent effects, the D_{it} profiles are categorized into three distinct cases: I, II, and III. Although previous studies indicate that Si/SiO_2 interfaces typically exhibit a

TABLE 1. Device parameters used in this study.

Device Parameters	Values
Number of Stacked Nanosheets, N_{NS}	3
Physical Gate length, L_G	12 nm
Channel Width, W_{CH}	45 nm
Nanosheet Thickness, T_{CH}	5 nm
Inner Spacer thickness, T_{SPACER}	3 nm
Vertical Space Between Nanosheets, V_{SPC}	10 nm
Interlayer Dielectric Thickness, T_{IL}	0.5 nm
High-k Dielectric Thickness, T_{HK}	1.28 nm
Contacted Poly-Si Pitch, CPP	44 nm
Fin Pitch, FP	56 nm
Source/Drain Doping Concentration, N_{SD}	3×10^{20} cm^{-3}
Punch-Through Stopper Doping Concentration, N_{PTS}	1×10^{18} cm^{-3}
Nanosheet Doping Concentration, N_{CH}	1×10^{17} cm^{-3}

U-shaped D_{it} distribution, this study models the D_{it} distribution as a combination of independent Gaussian peaks.

A Gaussian distribution function was utilized as follows [25], [26], [27], [28]:

$$= N_0 \exp\left(\frac{-(E-E_0)^2}{2E_\sigma^2}\right) \quad (1)$$

The peak interface trap density (N_0) was varied from 1×10^{11} eV^{-1}·cm^{-2} to 1×10^{13} eV^{-1}·cm^{-2}. This wide range was selected to clearly investigate the dependence of device characteristics on the interface trap density. The peak interface trap energy level (E_0) shifted within the silicon bandgap, as shown in **Fig. 4** [24].The standard deviation coefficient (E_σ) was set to 0.1 eV [27]. The neutral trap capture cross-section coefficient (σ) for both electrons and holes (σ_N, σ_P) was assumed to be 1×10^{-15} cm^2 based on previously reported values [29], [30].

Fig. 5 illustrates the charge trapping configurations of amphoteric interface traps at the Si/SiO_2 interface, where the traps are modeled as neutral centers [23]. The trap states are configured based on the intrinsic fermi energy level (E_I). Above E_I, acceptor states exist, while below E_I, the trap states are configured as donor states according to the neutral center configuration model [23], [24], [31], [32].

As shown in **Fig. 5a**, positive charges accumulate at the Si/SiO_2 interface in the accumulation mode. Donor states at the Si/SiO_2 interface, located at energy levels lower than the E_I but higher than the Fermi level (E_F), become positively charged by capturing holes. Conversely, as shown in **Fig. 5b**, Donor states at the Si/SiO_2 interface under inversion mode, located at energy levels lower than E_F, become neutral. References [23], [24], [31], [32], [33], [34].

Fig. 6 illustrates the I_D–V_G and I_D–V_D characteristics of the NS FETs as a function of donor-like trap density, ranging from 1×10^{11} eV^{-1}·cm^{-2} to 1×10^{13} eV^{-1}·cm^{-2}. While acceptor-like traps primarily shift the V_{th} in n-channel MOSFETs, donor-like traps within the high-k and interlayer

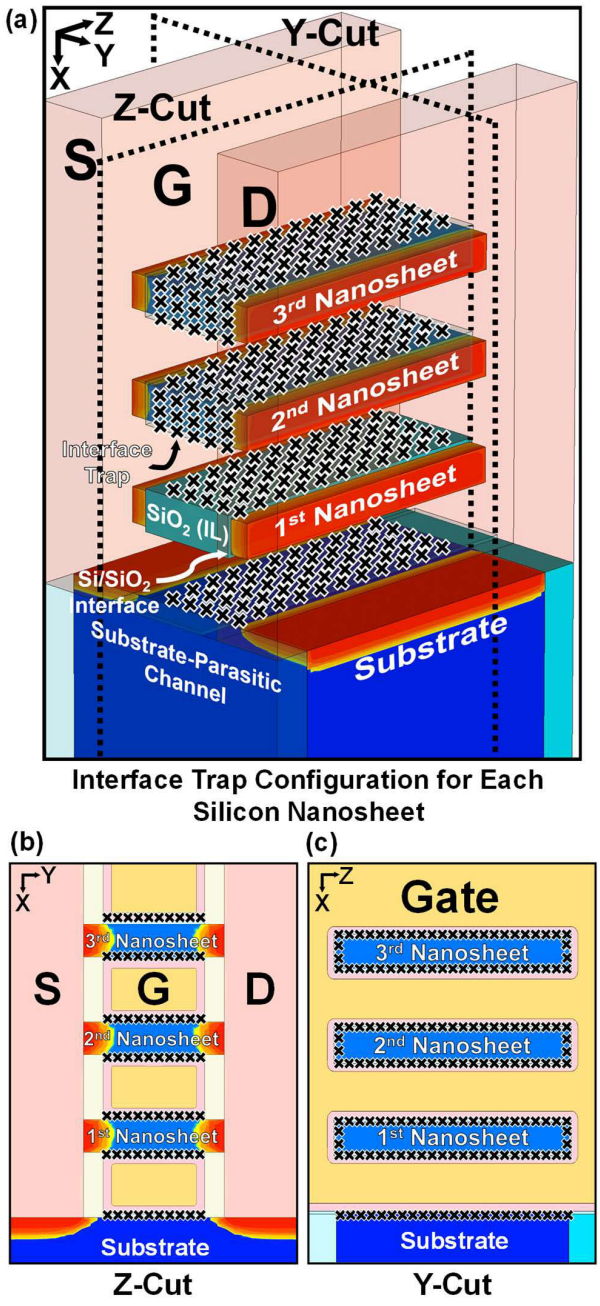


FIGURE 3. (a) 3-D schematic of a NS FET illustrating the interface trap charges between Si channel and the SiO_2 IL. (b) Cross-sectional view along the z-axis. (c) Cross-sectional view along the y-axis.

dielectric stacks significantly contribute to the degradation of the *SS* and I_{OFF}. Consequently, a rigorous sensitivity analysis of these donor-like traps is essential to evaluate their impact on device performance [26].

Specifically, the trap configuration was assumed to follow **Case I** as described in **Fig. 4**.

The peak interface trap level (E_0) was fixed at the mid-gap energy of silicon ($E_M = 0.56$ eV) to independently evaluate the impact of trap density on the device characteristics under identical E_0 conditions.

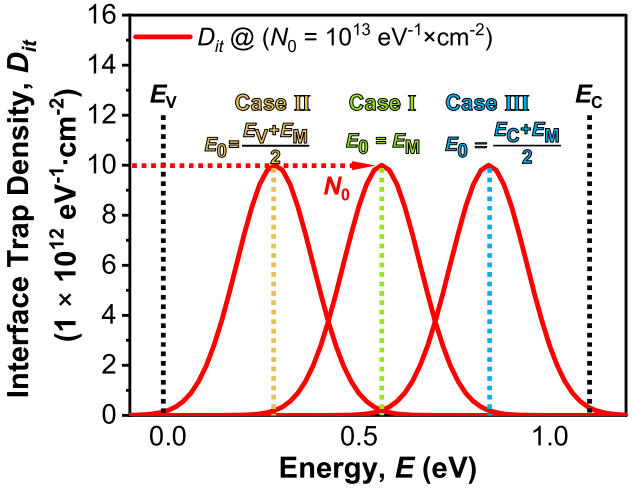


FIGURE 4. Interface trap density (D_{it}) distribution within the Si bandgap.

As shown in **Fig. 6a**, the impact of donor-like traps is negligible at densities up to 1×10^{12} $eV^{-1}{\cdot}cm^{-2}$. However, a significant degradation in the I_D–V_G characteristics becomes apparent when the density reaches 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$. The V_{TH} variation was approximately 0.5 %, where V_{TH} was extracted using the constant current method at 100 nA. Although advanced extraction techniques such as the Y-function method [35] can mitigate mobility degradation and series resistance, the conventional constant current method was preferred here to provide a consistent baseline for evaluating relative shift trends. This choice avoids the extensive parameter-extraction complexities inherent in decoupling the intertwined mobility responses of the multiply stacked channels and the substrate parasitic channel in NS FET architectures.

In contrast, the I_D-V_G curves exhibited a significant leftward shift in the subthreshold region, leading to a substantial increase in I_{OFF}. Consequently, the subthreshold swing (*SS*) degraded from 69.10 mV/dec to 103.25 mV/dec as the trap density increased from 1×10^{11} $eV^{-1}{\cdot}cm^{-2}$ to 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$. The *SS* was extracted by two orders below method, ranging from 1 nA to 100 nA below the V_{TH} extraction current baseline. The corresponding extraction range was selected to include subthreshold region where the affected by donor-like traps and potential parasitic conduction path, as well as the relatively higher subthreshold region mainly affected by acceptor-like traps.

Fig. 6b shows the I_D-V_D characteristics of NS FETs with donor-like traps under various overdrive voltages, where the donor-like trap density varies from 1×10^{11} $eV^{-1}{\cdot}cm^{-2}$ to 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$. As illustrated in **Fig. 6b**, the I_D-V_D characteristics exhibit a negligible difference across the investigated trap densities. This is because donor-like traps predominantly influence the subthreshold region rather than the strong inversion region. Consequently, varying the trap density within this range does not lead to noticeable variations in the output characteristics.

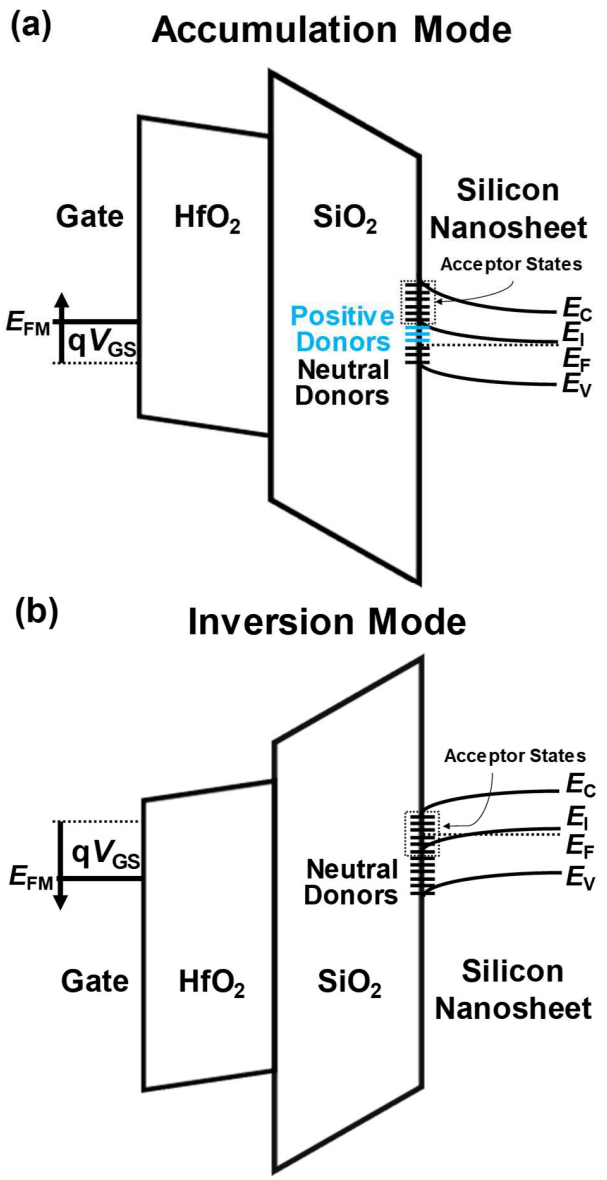


FIGURE 5. Schematic energy band diagrams of n-type MOS in NS FETs, illustrating the occupancy of donor-like traps under different gate-bias conditions: (a) accumulation mode and (b) inversion mode.

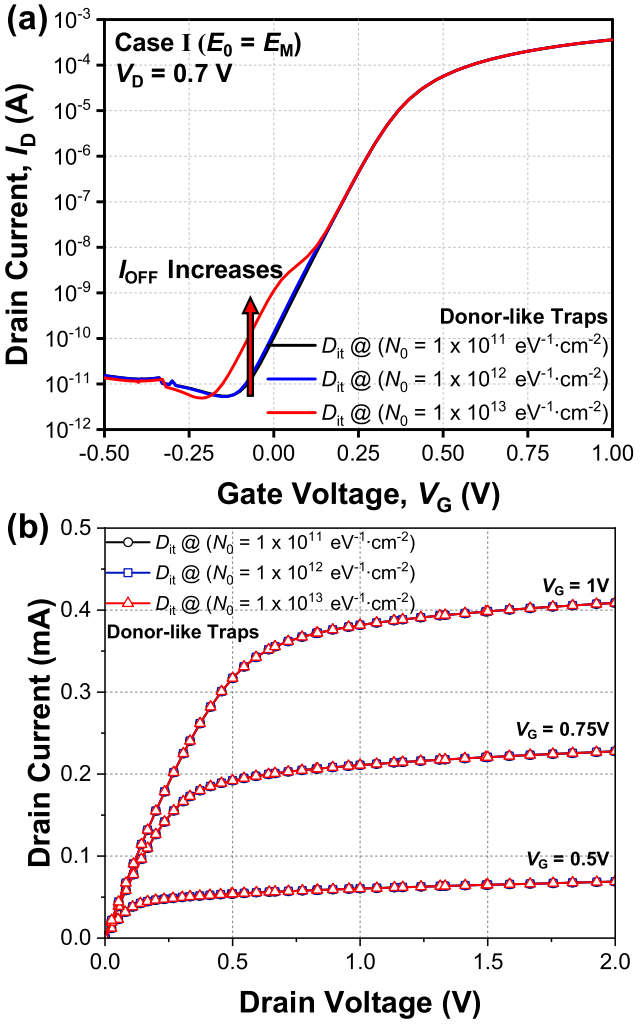


FIGURE 6. (a) Simulated I_D–V_G characteristics of NS FETs with various donor-like trap densities. (b) Simulated I_D–V_D characteristics of NS FETs with respect to FETs with various donor-like trap densities under various overdrive voltage.

Fig. 7 shows cross-sectional views of the internal current density and electrostatic potential distributions in the NS FET with donor-like traps, comparing cases with trap densities of 1×10^{12} $eV^{-1}{\cdot}cm^{-2}$ and 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$ at $V_G = 0$ V. **Fig. 7a** illustrates the internal current density of the NS FET with donor-like traps at $V_G = 0.0$ V. As shown in the figure, the electron current density increases significantly in the presence of donor-like traps with an N_0 of 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$ compared to the 1×10^{12} $eV^{-1}{\cdot}cm^{-2}$. This increased current density in the off-state corresponds to the rise in I_{OFF} observed in the I_D-V_G characteristics. **Fig. 7b** shows the electrostatic potential of the NS FET with donor-like traps at $V_G = 0.0$ V, where the electrostatic potential in the SiO_2 interlayer dielectric was extracted along the x-axis. As shown in **Fig. 7b**, when the donor-like trap density (N_0) increases from 1×10^{12} to 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$, the SiO_2 region becomes more positively charged. Consequently, the electrostatic potential within the SiO_2 layer becomes higher.

Fig. 8a illustrates the space charge distributions in the NS FETs with a donor-like trap density of 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$ at $V_D = 0.7$ V and $V_G = 0.2$ V. $V_G = 0.2$ V was selected as the bias condition to investigate the space charge distributions in the subthreshold region, where the influence of interface traps on the electrostatic control is most prominent. As shown in the figure, positively charged donor states at the Si/SiO_2 interface induce minority carrier inversion, leading to electron accumulation at the channel surface. These accumulated electrons create parasitic conduction paths in each channel region, thereby significantly increasing the I_{OFF} even in the off-state.

Fig. 8b shows the I_D-V_G characteristics for donor-like traps as a function of different E_0. The trap density was set to

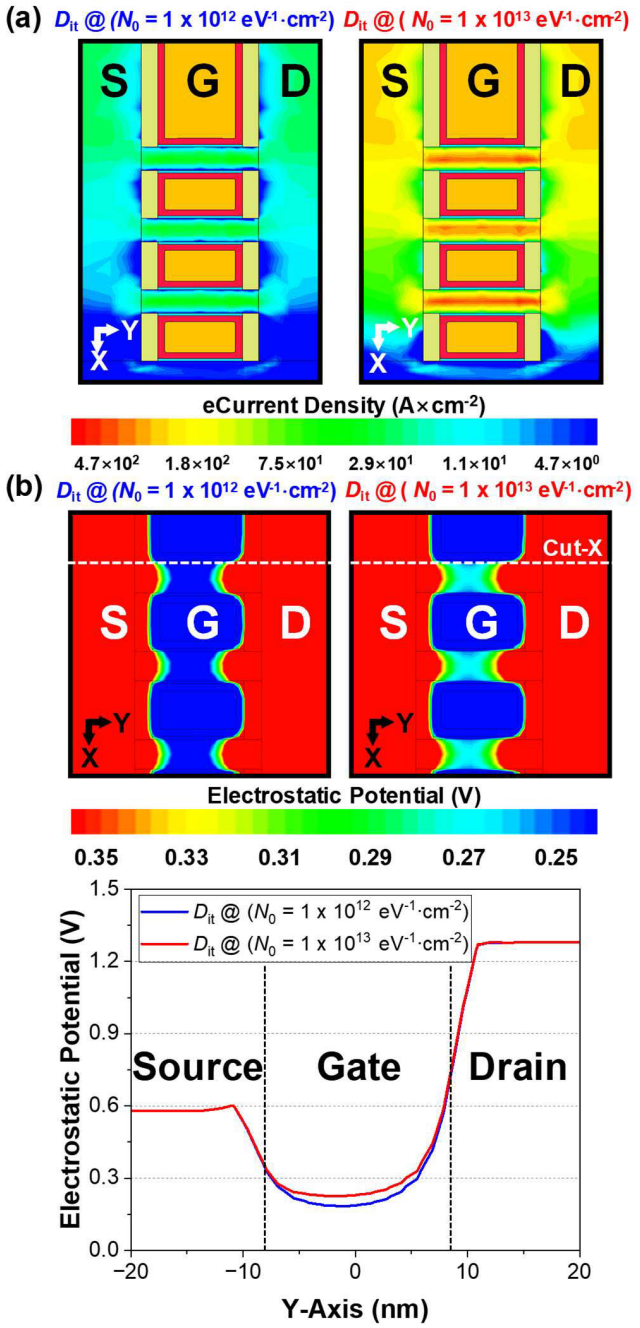


FIGURE 7. (a) Comparison of internal current density distributions in the NS FET with and without donor-like traps at V_D = 0.7 V and V_G = 0.0 V. (b) Simulated electrostatic potential plots of the NS FETs with and without donor-like traps, and the extracted electrostatic potential profile along the SiO_2 interlayer at V_D = 0.7 V and V_G = 0.0 V.

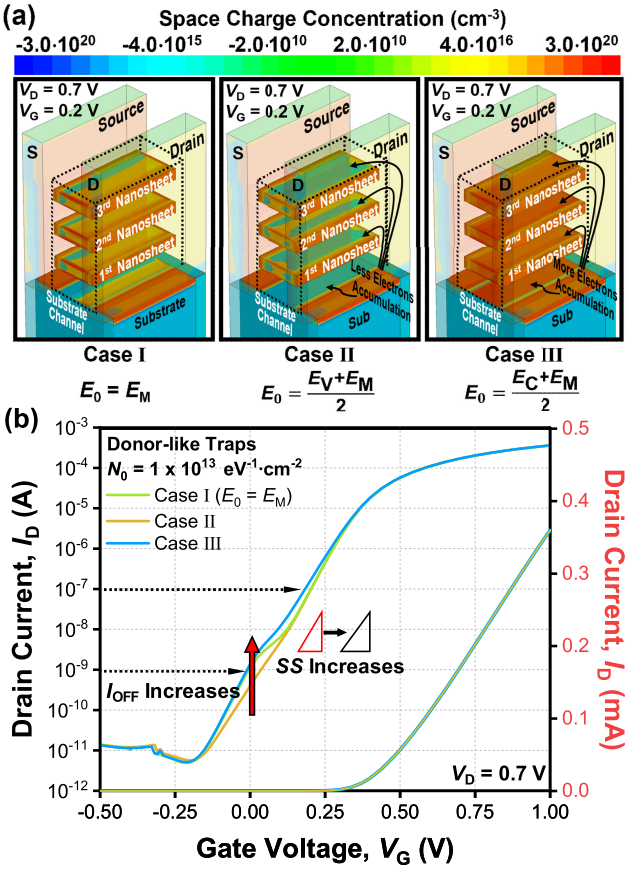


FIGURE 8. (a) 3-D schematic views of the space charge distribution regions for various peak interface trap energy levels (E_0) of donor-like traps. (b) I_D-V_G characteristics of the NS FETs as a function of different E_0 values for donor-like traps.

1×10^{13} eV^{-1}·cm^{-2} to evaluate the impact of the donor-like trap energy level under identical conditions. As illustrated in the figure, **Case III**, where E_0 is located above E_M, the largest I_{OFF} is exhibited. The impact of donor-like traps on I_{OFF} gradually decreases as E_0 shifts toward lower energy levels.

Although these data are not included in the main text, the Gaussian trap distributions for both cases near E_C and E_V exhibited identical trends. For donor-like traps, the I_{OFF} increased as the trap distribution shifted closer to the E_C, which is consistent with **Case III**.

These results demonstrate that donor-like traps with lower E_0 values are more likely to be neutralized under accumulation mode as a larger portion of the trap distribution is occupied. Consequently, the occupancy of donor-like traps depends significantly on their E_0 and Esigma values. The extracted electrical characteristics of the NS FETs, including different E_0 and N_0 values, are summarized in **Table 2**.

TABLE 2. Extracted DC characteristics for different donor-like trap distributions.

	Peak Interface Trap Density, N_0 [eV^{-1}·cm^{-2}] @ Case I ($E_0 = E_M$)			Peak Interface Trap Energy level, E_0 (eV) (N_0 = 1 x 10^{13} eV^{-1}·cm^{-2})		
	1 x 10^{11}	1 x 10^{12}	1 x 10^{13}	Case I	Case II	Case III
V_{TH} (mV)	203.66	203.47	202.61	202.61	203.57	183.49
SS (mV/dec)	68.74	72.33	103.25	103.25	83.68	96.72
I_{OFF} (pA)	102.76	133.04	1,119.9	1,119.9	390.49	1,367.6
I_{ON} (μA)	170.53	170.53	170.53	170.53	170.53	170.68

Fig. 9a shows the I_D-V_G characteristics of the NS FET with donor-like traps as a function of the spatial locations of the traps. The N_0 and E_0 were set to 1×10^{13} eV^{-1}·cm^{-2}

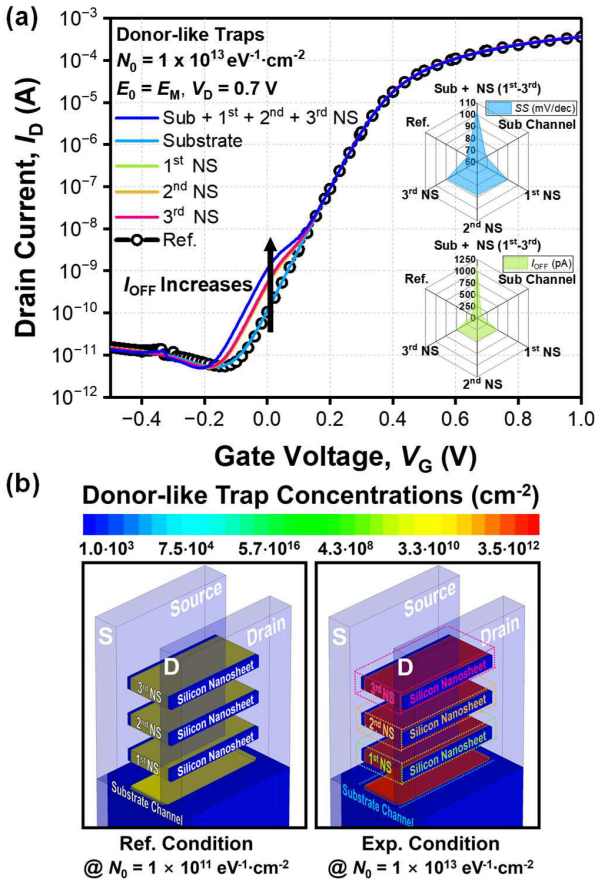


FIGURE 9. (a) I_D-V_G characteristics of the NS FET as a function of trap location, and corresponding spider charts for SS and I_{OFF} with donor-like traps, while the reference denotes the donor-like traps are distributed across entire Si/SiO_2 interface at N_0 = 1 × 10^{11} eV^{-1}cm^{-2} and E_0 = 0.56 eV (b) 3-D schematic comparing reference and experimental conditions, where each of the colored 1st, 2nd, 3rd nanosheets and substrate channel regions indicate the donor-like traps are selectively introduced only at a single Si/SiO_2 interface.

and 0.56 eV, respectively, to evaluate the effects of different trap locations under identical conditions. Additionally, the reference condition for donor-like traps was established at $N_0 = 1 \times 10^{11}$ eV^{-1}·cm^{-2} and $E_0 = 0.56$ eV across the entire Si/SiO_2 interface as shown in **Fig. 9b**. This baseline accounts for non-ideal interface conditions and is considered the minimum interface trap density for the NS FETs.

The spider charts shown in the inset of **Fig. 9a** illustrate the degree of variation for *SS* and I_{OFF} at each location. When traps are present solely at the substrate interface (*i.e.*, the Si/SiO_2 interface above the substrate parasitic channel region), the differences in *SS* are negligible compared to the reference condition.

The substrate was fully doped with a retrograded PTS to suppress the formation of parasitic conduction paths beneath the silicon substrate. Consequently, this suggests that the impact of donor-like traps in the silicon substrate must be evaluated by considering the actual doping concentration and distribution of the PTS.

On the other hand, when donor-like traps are located in the first, second, or third silicon nanosheet, I_{OFF} increases throughout the off-state region. The donor-like traps in each stacked nanosheet exert a similar influence on the I_D-V_G characteristics. Specifically, the *SS* increases by approximately 20 mV/dec per each silicon nanosheet, and the I_{OFF} increases by 4.4 to 4.7 times compared to the reference.

It is evident that the presence of donor-like traps at the Si/SiO_2 interface of even a single stacked silicon nanosheet substantially degrades both the *SS* and I_{OFF}. Furthermore, when traps are located across the entire Si/SiO_2 interface in the channel regions, the *SS* and I_{OFF} increase to 103.2 mV/dec and 10.6 times the reference values, respectively.

However, no differences in I_{ON} are observed compared to the reference, regardless of the donor-like trap locations within the stacked silicon nanosheet channels. This is because most donor-like trap states are fully occupied by electrons in the inversion mode at $V_G = 0.7$ V. Consequently, the net charge of the donor-like traps becomes nearly neutral, resulting in no change to the on-state characteristics. The detailed DC characteristics, depending on the donor-like trap locations, are summarized in **Table 3**.

TABLE 3. DC characteristic variations for different spatial locations of donor-like traps.

	Location of Acceptor-Like Traps at Si/SiO_2 interfaces, @ Case I (E_0 = E_M), N_0 = 1 x 10^{13} eV^{-1}·cm^{-2}					
	Ref.	Sub	1st NS	2nd NS	3rd NS	(Sub + 1st + 2nd + 3rd NS)
V_{TH} (mV)	203.64	203.66	203.30	203.26	203.28	202.61
SS (mV/dec)	69.10	68.85	89.52	88.09	88.90	103.25
I_{OFF} (pA)	105.43	107.59	495.45	464.33	482.72	1120.05
I_{ON} (μA)	170.52	170.52	170.52	170.52	170.52	170.52

As shown in **Fig. 10a**, most acceptor-like traps at the Si/SiO_2 interface in the accumulation mode located at energy levels higher than E_F, remain neutral. Conversely, as shown in **Fig. 10b**, negative charges accumulate under the inversion mode. Acceptor states at the Si/SiO_2 interface, located at energy levels higher than the E_I but lower than E_F, become negatively charged by capturing electrons [23], [31], [32], [33], [34].

Fig. 11a shows the I_D-V_G and I_D–V_D characteristics of the NS FETs for acceptor-like trap densities ranging from 1 × 10^{11} eV^{-1}·cm^{-2} to 1 × 10^{13} eV^{-1}·cm^{-2}. Prior studies have established that acceptor-like traps are primarily responsible for the degradation associated with positive bias temperature instability (PBTI).

Consequently, a rigorous sensitivity analysis of these acceptor-like traps is essential to elucidate their quantitative impact on reliability [36].

The trap configuration follows **Case I** ($E_M = 0.56$ eV), consistent with the donor-like trap setup described in **Fig. 10**. As shown in **Fig. 11a**, acceptor-like trap densities of up to 1× 10^{12} eV^{-1}·cm^{-2} have a negligible impact on device characteristics. However, significant degradation in I_D-V_G characteristics is observed when the density reaches

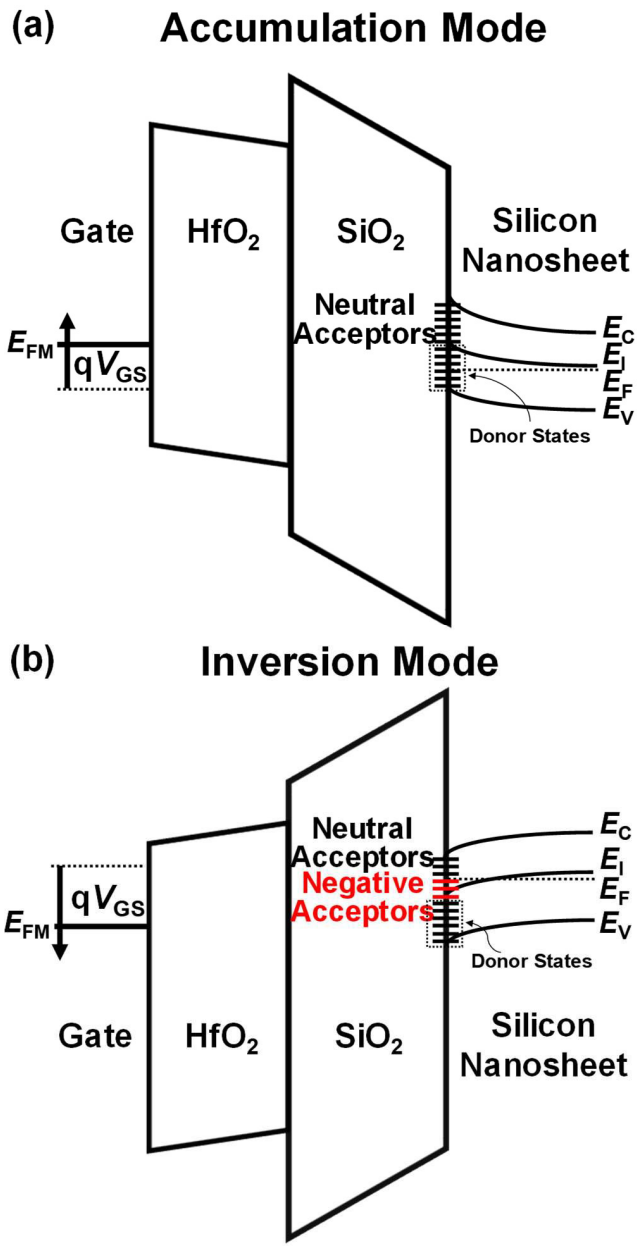


FIGURE 10. Schematic energy band diagrams of n-type MOS in NS FETs, illustrating the occupancy of acceptor-like traps depending on different gate-bias conditions: (a) accumulation mode and (b) inversion mode.

1×10^{13} $eV^{-1}{\cdot}cm^{-2}$. The V_{TH} shifted from 204.4 mV to 282.8 mV, and the *SS* degraded from 69.1 mV/dec to 103.0 mV/dec. Additionally, a substantial reduction in I_{ON} is observed as the trap density increases from 1×10^{11} $eV^{-1}{\cdot}cm^{-2}$ to 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$.

Fig. 11b shows the I_D-V_D characteristics of NS FETs with acceptor-like traps at different overdrive voltages, where the trap density varies from 1×10^{11} $eV^{-1}{\cdot}cm^{-2}$ to 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$. In contrast to donor-like traps, acceptor-like traps significantly influence the I_D-V_D characteristics. Consequently, a substantial degradation in the overdrive current (I_{OV}) was observed as the trap density increased.

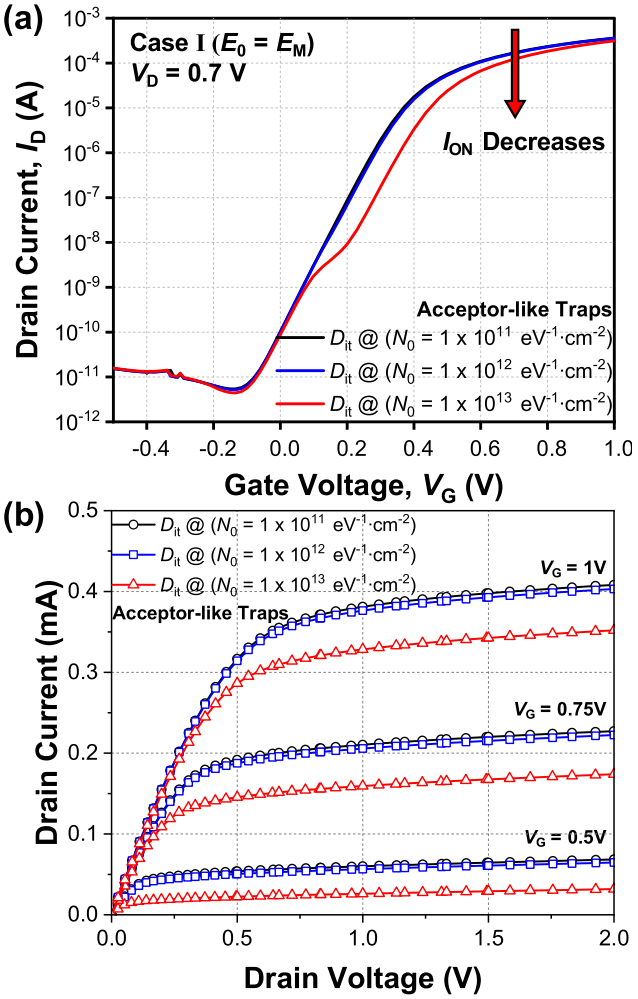


FIGURE 11. (a) Simulated I_D–V_G characteristics of NS FETs with various acceptor-like trap densities. (b) Simulated I_D–V_D characteristics of NS FETs with respect to FETs with various acceptor-like trap densities under various overdrive voltage.

Fig. 12 illustrates the internal current density and electrostatic potential distributions in the NS FETs, comparing cases with acceptor-like trap densities of 1×10^{12} $eV^{-1}{\cdot}cm^{-2}$ and 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$ acceptor-like traps at $V_G = 0.7$ V.

Fig. 12a shows the internal current density of the NS FET with acceptor-like traps at $V_G = 0.7$ V. As illustrated, the electron current density decreases significantly when N_0 increases from 1×10^{12} $eV^{-1}{\cdot}cm^{-2}$ to 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$. This reduction in current density under the on-state condition is responsible for the I_{ON} degradation observed in the I_D-V_G characteristics.

Fig. 12b shows the electrostatic potential of the NS FET with acceptor-like traps at $V_G = 0.7$ V, where the electrostatic potential in the SiO_2 interlayer dielectric was extracted along the x-axis. In contrast to the donor-like traps, the SiO_2 region becomes more negatively charged as the acceptor-like trap density (N_0) increases from 1×10^{12} to 1×10^{13} $eV^{-1}{\cdot}cm^{-2}$. Consequently, this leads to a reduction in the extracted electrostatic potential within the layer.

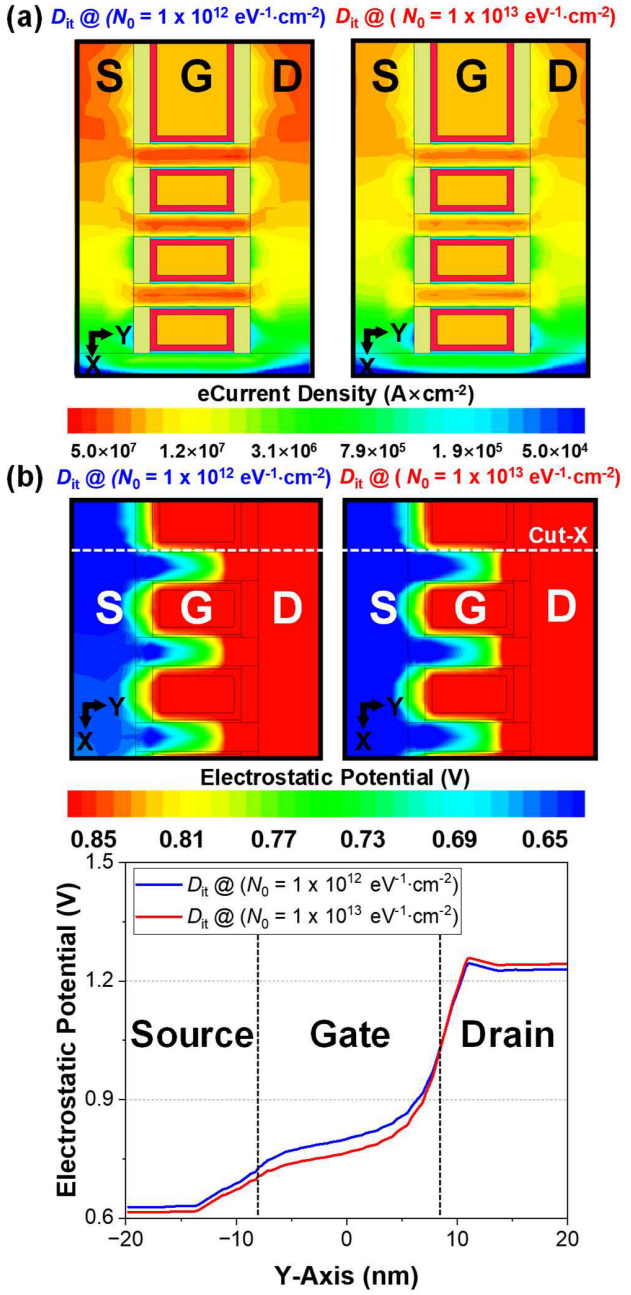


FIGURE 12. (a) Comparison of internal current density distributions in the NS FET with and without acceptor-like traps at V_D = 0.7 V and V_G = 0.7 V. (b) Simulated electrostatic potential plots of NS FETs with and without acceptor-like traps, along with the extracted electrostatic potential profiles along the SiO_2 interlayer at V_D = 0.7 V and V_G = 0.7 V.

Fig. 13a shows the space charge distributions in the NS FETs with acceptor-like traps at a density of 1×10^{13} eV^{-1}·cm^{-2}, under $V_D = 0.7$ V and $V_G = 0.2$ V. Consistent with the analysis of donor-like traps, $V_G = 0.2$ V was selected as the bias condition. As shown in the figure, the negatively charged acceptor states at the Si/SiO_2 interface induce majority carrier accumulation, leading to hole accumulation at the channel surface. These accumulated holes suppress channel formation under inversion bias conditions, thereby substantially decreasing I_{ON} in each nanosheet channel.

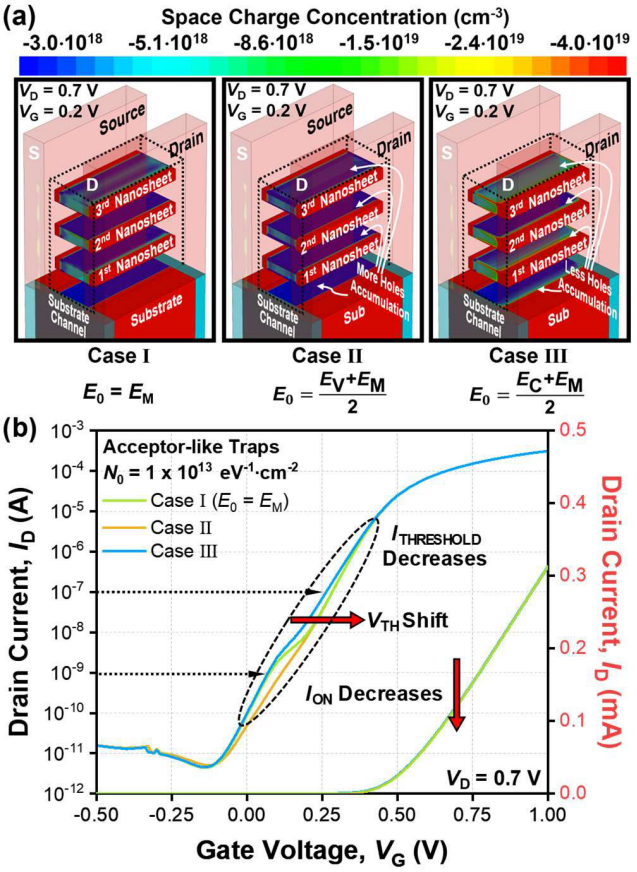


FIGURE 13. (a) 3-D schematics of the space charge distribution regions for various acceptor-like trap energy levels (E_0). (b) I_D-V_G characteristics for various E_0 values of acceptor-like traps.

Fig. 13b shows the I_D-V_G characteristics as a function of different E_0. Consistent with the donor-like trap analysis, the trap density was set to 1×10^{13} eV^{-1}·cm^{-2} to evaluate the effects of E_0 under identical conditions. In **Case II**, where E_0 is positioned at the lowest energy level, a significant decrease in drain current is observed in both the subthreshold and on-state regions.

As E_0 shifts toward higher energy levels, a substantial increase in ΔV_{TH} is observed. Furthermore, **Case I** exhibits the highest Δ *SS*. This is attributed to a higher concentration of negatively charged acceptor-like traps at the Si/SiO_2 interfaces.

In contrast to donor-like traps, these results demonstrate that acceptor-like traps with lower energy levels are more likely to be occupied. However, under the strong inversion mode, little difference in I_{ON} is observed among **Cases I**, **II**, and **III**. Although these data are not included in the main text, the Gaussian distributions located near E_C and E_V exhibited identical trends. Specifically, the V_{TH} shift was similar to **Case II** as the distribution shifted closer to the E_V. This is because most acceptor-like traps are occupied regardless of their E_0 positions under strong inversion bias conditions.

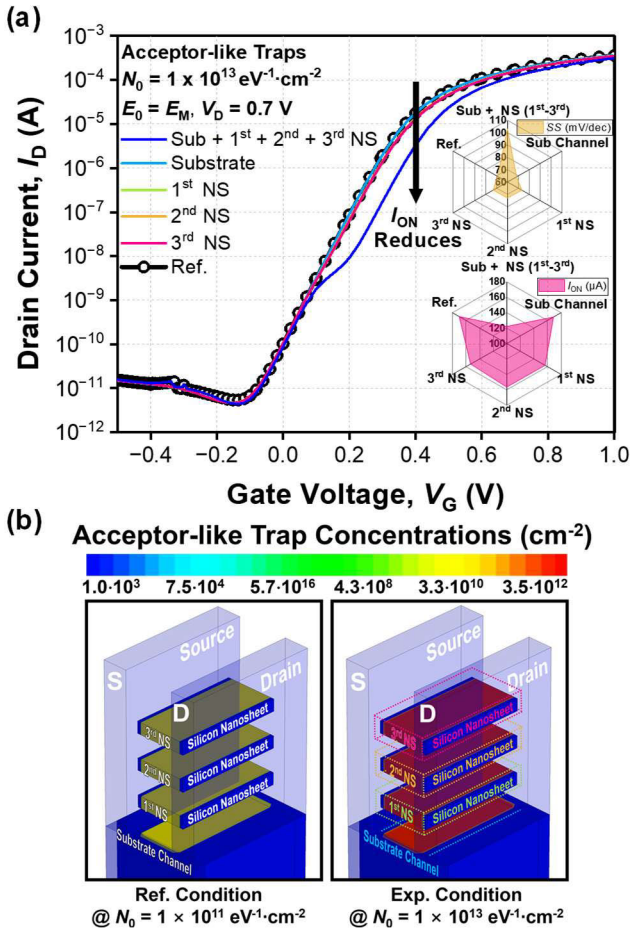


FIGURE 14. (a) I_D-V_G characteristics of the NS FET as a function of trap location, and corresponding spider charts for SS and V_{TH} with acceptor-like traps, where the reference represents the acceptor-like traps distributed across the entire Si/SiO_2 interface at N_0 = 1 × 10^{11} eV^{-1}·cm^{-2} and E_0 = 0.56 eV (b) 3-D schematic comparing reference and experimental conditions, where the highlighted 1st, 2nd, 3rd nanosheets and substrate channel regions indicate that the acceptor-like traps are confined to only a single Si/SiO_2 interface.

Consequently, it is clear that the occupancy of acceptor-like traps depends strongly on the E_0 and Esigma values of the trap distribution, similar to the behavior observed in donor-like traps. The detailed extracted electrical characteristics of the NS FETs with acceptor-like traps, including various E_0 and N_0 values, are additionally summarized in **Table 4**.

Fig. 14a shows the I_D-V_G characteristics of the NS FET with acceptor-like traps as a function of trap location. Consistent with the donor-like trap analysis, N_0 and E_0 were set to 1 × 10^{13} eV^{-1}·cm^{-2} and 0.56 eV, respectively. The reference condition was established with N_0 = 1 × 10^{11} eV^{-1}·cm^{-2} and E_0 = 0.56 eV across the entire Si/SiO_2 interface as shown in **Fig. 14b**. As illustrated in the inset of **Fig. 14a**, the spider charts represent the degrees of variation for *SS* and ΔV_{TH} at each location.

Similar to the donor-like trap cases, when acceptor-like traps are located solely at the substrate interface (*i.e.*, the Si/SiO_2 interface above the substrate parasitic channel), the variations in both *SS* and I_{ON} are negligible.

TABLE 4. Extracted DC characteristics for different acceptor-like trap distributions.

	Peak Interface Trap Density, N_0 [eV^{-1}·cm^{-2}] @ Case I (E_0 = E_M)			Peak Interface Trap Energy level, E_0 (eV) @ (N_0 = 1 x 10^{13} eV^{-1}·cm^{-2})		
	1x10^{11}	1x10^{12}	1x10^{13}	Case I	Case II	Case III
V_{TH} (mV)	204.45	211.51	282.80	282.80	283.54	263.38
SS (mV/dec)	69.104	72.357	103.02	103.03	83.83	96.77
I_{OFF} (pA)	102.62	101.36	87.887	87.887	48.381	98.361
I_{ON} (μA)	170.03	165.59	122.17	122.17	122.30	122.54

TABLE 5. DC characteristic variations for different spatial locations of acceptor-like traps.

	Location of Acceptor-Like Traps at Si/SiO_2 interfaces, @ Case I (E_0 = E_M), N_0 = 1 x 10^{13} eV^{-1}·cm^{-2}					
	Ref.	Sub	1st NS	2nd NS	3rd NS	(Sub + 1st + 2nd + 3rd NS)
V_{TH} (mV)	204.45	203.99	215.01	214.08	214.68	282.80
SS (mV/dec)	69.10	68.40	73.37	72.99	73.23	103.03
I_{OFF} (pA)	102.61	96.807	100.27	100.79	100.42	87.88
I_{ON} (μA)	170.03	168.90	156.48	156.51	153.23	122.17

This is due to the effectiveness of the retrograded PTS in the silicon substrate. However, significant degradation in I_{ON} and *SS*, along with a V_{TH} shift, are observed when acceptor-like traps are located in the stacked first, second, or third silicon nanosheet.

Specifically, the *SS* increases by approximately 4 mV/dec per stacked nanosheet compared to the reference condition. These results confirm that both donor-like and acceptor-like traps degrade the *SS*. Furthermore, each affected nanosheet contributes to a reduction in I_{ON} of approximately 15 uA and a ΔV_{TH} of +14 mV. When acceptor-like traps are distributed across the entire channel region, substantial degradation occurs, with I_{ON} and *SS* degrading by 48 uA and 34 mV/dec, respectively, while the ΔV_{TH} reaches 72 mV.

Regarding I_{OFF}, a reduction is observed across all locations. This occurs because most acceptor-like trap states are unoccupied in the accumulation mode, resulting in a nearly neutral net charge. However, partially occupied acceptor-like traps still hinder conduction path formation in the accumulation mode, thereby contributing to the reduction in I_{OFF}. The detailed DC characteristics depending on acceptor-like trap locations are summarized in **Table 5**.

Although this study focuses on the effects of the Si/SiO_2 interface traps, questions may arise regarding the trap effects between the Si channel and the SiN inner spacer. To address this, we compared the electrical characteristics under the Si-SiN interface trap conditions with the trap-free case. As a result, the traps showed no notable differences for either donor-like or acceptor-like cases. This is because the SiN inner spacers are located in the source/drain extension regions, where highly diffused dopants exist underneath the interface due to annealing processes. Consequently, unlike the traps at the Si/SiO_2 interface that directly influence the

channel potential, the interface traps at the Si/SiN interface have a negligible impact on the overall device performance.

IV. CONCLUSION

We investigated DC characteristic degradations induced by two distinct types of interface traps in n-type nanosheet FETs using 3-D TCAD simulations. Both types of traps exhibited negligible impact up to a density of 1×10^{12} $eV^{-1} \cdot cm^{-2}$. However, significant degradation occurred at 1×10^{13} $eV^{-1} \cdot cm^{-2}$. Specially, donor-like traps increased subthreshold swing *(SS)* by 49.4 % and off-state leakage current (I_{OFF}) by 10.6-fold. In contrast, acceptor-like traps led to a 49.0 % increase in the threshold voltage shift (ΔV_{TH}), while degrading the *SS* by 38.3 % and reducing the on-state current (I_{ON}) by 28.5 %.

Energy-level dependent analysis revealed that donor-like traps near the conduction band edge (E_C) and acceptor-like traps near the valence band edge (E_V) are predominantly occupied, dictated by their respective charging tendencies. Furthermore, while the impact of both trap types in the substrate parasitic channel was effectively suppressed by the punch-through stopper (PTS), the presence of interface traps on even a single silicon nanosheet caused severe DC performance degradation. These findings provide a comprehensive analytical guideline for characterizing donor and acceptor-like interface traps in advanced nanosheet FET structures.

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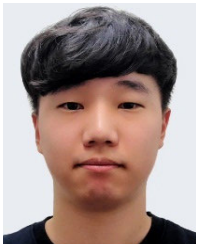
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