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Efficient DC-coupled linear 60-GBd EML-based O-band transmitter

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Abstract: O-band transmitters are key to current and next-generation communication links. In this paper, the authors present a transmitter based on an InGaAlAs multi-quantum well (MQW) electroabsorption modulated laser (EML) and a 130 nm SiGe BiCMOS driver integrated circuit (IC). The functionality and architecture of both ICs are discussed, including the co-design aspects deriving from the DC-coupled interface, with a particular focus on the driver's high immunity to the EAM photocurrent and capability to supply a very wide bias voltage range to the EAM. The proposed transmitter is able to send 60 GBd PAM4 signals with an extinction ratio (ER) of 8 dB at a power efficiency of 4.3 pJ/bit. Additionally, it is able to transmit up to 80 GBd NRZ signals and is even sufficiently linear to transmit PAM8 signals at 40 GBd, showcasing the transmitter potential in a wide range of applications.

1. Introduction

The rapid growth in data traffic from cloud computing, big data, the Internet of Things (IoT), industry 4.0 and Artificial Intelligence (AI) requires fast, energy-efficient optical communication links in hyper-scale data centers and metro-scale optical interconnects.

The O-band is the primary choice for low-cost intensity modulated optical interconnects beyond 50 Gb/s per lane supporting distances beyond several tens of kilometres [1,2] thanks to its near zero chromatic dispersion.

Multiple technologies and implementations of O-band transmitters have been proposed such as vertical cavity surface emitting laser (VCSELs) [3], distributed feedback DFB lasers [4], pEML [5], silicon photonic ring modulators [6] and Mach-Zehnder modulator (MZMs) on various platforms [7].

In this work we focus on EML-based transmitters as these generally provide higher speed and longer reach compared to directly modulated VCSELs or DFB lasers lasers, while EMLs are integrated in a small footprint compared to MZMs. Furthermore, the DFB laser and semiconductor optical amplifier (SOA) are monolithically integrated with the electroabsorption modulator (EAM), which allows for a higher output power on a smaller footprint when comparing to silicon photonic transmitters, which require an external or hybrid integrated laser. Moreover, a III-V-based EAM provides a higher extinction ratio than a silicon photonic ring or EAM [8].

In this paper we focus on the driver IC design for an O-band EML based transmitter. The driver IC targeted 60 GBd 4-level pulse amplitude modulation (PAM4) modulation, and offers what we believe to be some novel, particularly useful features to drive electroabsorption modulated lasers (EMLs). The enhanced linearity of the output stage has been previously discussed in [9], whereas this paper focuses on the key features related to driving EMLs. First of all, this driver can be DC-coupled to the EML, which means no external bias-tee is needed and DC-coupling can even make it suitable for burst-mode traffic. Additionally, it supports an extended Electroabsorption

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Modulator (EAM) bias voltage range from 0 V to beyond 10 V, without transistor breakdown. Furthermore, the DC-coupled interface can accept a photocurrent from the EAM up to 30 mA, without noticeable degradation in the eye quality.

The paper is structured as follows. Section 2 presents the architecture, going into detail about both the EML and driver Integrated Circuit (IC) functionality and their features. Section 3 details the measurements and Section 4 compares the results to other state of the art O-band transmitters.

2. Architecture

Fig. 1 depicts the schematic of the two chips in the proposed transmitter: the electronic driver IC, fabricated in 130 nm SiGe BiCMOS is wirebonded to an InGaAlAs multi-quantumWell (MQW) photonic integrated circuit (PIC) containing the distributed feedback (DFB) laser, the optical modulator and the semiconductor optical amplifier (SOA). Both of these blocks will be discussed in detail below.

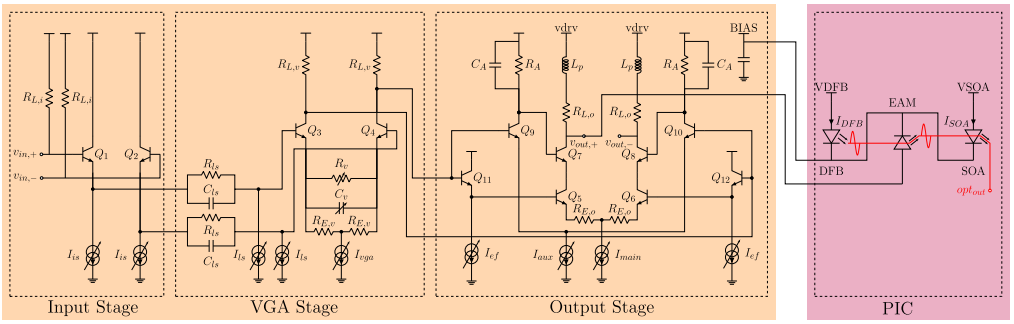

Fig. 1. Schematic of driver without matching circuits or electrostatic discharge (ESD) protection pictured (orange) and schematic of the EML (purple).

2.1. EML

The co-integrated EML PIC is an improved design of [5]. The device comprises a single EML chip designed for operation in the O-Band wavelength range, shown in Fig. 2. Light generation is accomplished using a DFB laser with an index-coupled grating that includes a $\lambda/4$ phase shift, ensuring a high side mode suppression ratio exceeding 45 dB. The back facet of the DFB laser is anti-reflection (AR) coated to improve single-mode operation. The forward-emitted light from the DFB laser is modulated by an integrated EAM section, which features ground-signal-ground (GSG) contacts for high-speed electrical access. These connections are routed through transmission lines to the backside of the chip, ensuring a short wire bond connection to the driver for optimal high bandwidth performance. A SOA, integrated after the EAM, increases the output power of the modulated signal. The three closely integrated devices share the same cathode contact, as can be seen in Fig. 1. The DC-contacts of the DFB and SOA are routed to the front of the device for access with wirebonds. The waveguide at the front facet is tilted and AR-coated to suppress back reflections into the laser cavity. The entire device is manufactured using a ridge waveguide structure on a single InGaAlAs-based multi-quantum well (MQW) layer stack.

Fig. 3 illustrates the test results of bare die EML across heatsink temperatures from 30 to 70°C. Fig. 3(a) shows the ex-facet output power versus DFB current (I_{DFB} in Fig. 1) for three heatsink temperatures, with threshold current decreasing from 55 mA to 33 mA as temperature rises. This is due to the significant detuning between the lasing wavelength and DFB gain maximum needed for EMLs with identical MQW layers. For uncooled operation, this large detuning is advantageous, allowing similar output power at varying temperatures. By adjusting the SOA

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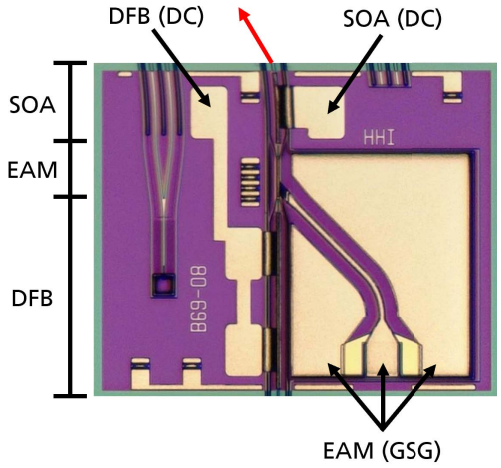

Fig. 2. Micrograph of fabricated EML, with its different components annotated.

current between 20 mA and 40 mA, an equal output power of approximately 10 mW is achieved for all temperatures at 100 mA DFB current. Fig. 3(b) shows the ER versus EAM bias voltage. At 30 °C, a static extinction ratio of up to 5 dB is achieved, increasing to 12 dB at 70 °C. This is caused by the band edge of the EAM shifting with respect to temperature by 0.5 nm/K [10], which consequently also changes the extinction ratio (ER) of the EAM. Fig. 3(c) displays the frequency response measured at different temperatures when loaded with a 50 Ω termination, with the EAM bias adjusted for linear operation. As the linear portions of the ER curve in Fig. 3(b) shift with temperature, the bias voltages when measuring S_{21} have to change accordingly. Across the temperature range, the device maintains a high 3 dB bandwidth above 42 GHz, with a modulation bandwidth of 46 GHz at 50 °C. The drop in response in the 0 to 5 GHz range is caused by an optical reflection back into the EML, since it was coated to be compatible with ultraviolet (UV) glue, but tested in air. Additionally, the small peaking that can be observed between 20 and 30 GHz is due to the RF probes that were used.

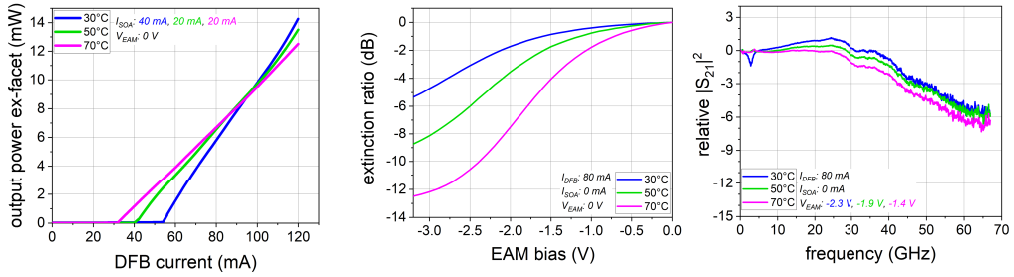

Fig. 3. (a) ex-facet output power of DFB laser a.f.o. its current (b) Extinction ratio for different EAM biases. (c) Electro-optic transmission frequency response of PIC.

2.2. Driver

The output stage of the proposed driver electronic integrated circuit (EIC) is based on the breakdown voltage doubler (BVD) architecture [11,12], which can be seen in the orange portion of Fig. 1. The driver EIC was designed in a 130 nm SiGe BiCMOS technology, chosen for its

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high f_T of 350 GHz and breakdown voltage BV_{CEO} above 1.6 V, to achieve high-speed operation in combination with a high output swing and high linearity, while also providing CMOS logic for the implementation of digital registers. Naturally, the driver is matched to 50 Ω by the resistors $R_{L,i}$ in the input stage. A micrograph is provided in Fig. 4.

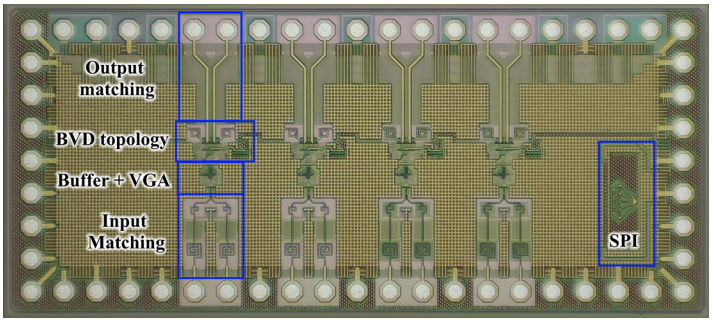

Fig. 4. Micrograph of fabricated driver EIC. Dimensions are 2.7 mm x 1.2 mm.

The most straightforward way to understand the principle behind the BVD is to compare it with a regular cascode architecture. In the regular cascode, most of the signal swing at the output of the driver is over the cascode transistors. Intuitively, this can be understood because the base-emitter voltage V_{BE} of the cascode transistor is quasi-constant, and the base voltage is usually decoupled very well in order to increase the stability of the circuit. Contrarily, the BVD doesn't have a DC voltage at the base of the cascode transistor. Instead, it moves correspondingly with the base voltage of the main transistors. In this way, the full output swing of the driver gets equally distributed over both main and cascode transistors, allowing or a higher total output swing, since we are now able to employ both transistors close to their breakdown voltage, instead of only the cascode transistor in the traditional case. The breakdown voltage of the combination is now doubled, hence the name.

Usually, the BVD architecture is thus used for very high swing drivers. Furthermore, previous research has demonstrated the excellent linearity behaviour of the architecture as well, beyond what would be expected by using the 2 Ω emitter degeneration resistances $R_{E,o}$ [9]. Because the EML discussed in Section 2.1 needs only a modest voltage swing to achieve an appropriate ER, in this work, the BVD was primarily used because of its excellent linearity properties.

In addition, the driver possesses an input buffer and a variable gain amplifier (VGA). The VGA has internal load terminatations $R_{L,v}$ of 50 Ω and can on one hand control the DC gain of the driver, due to the variable resistor R_v, which varies the 15 Ω fixed emitter degeneration $R_{E,v}$ of the differential pair in the VGA and thus its gain [13]. ddditionally, it can introduce a small amount of peaking [14,15], due to the variable capacitor C_v. Both variable passives are implemented using MOSFETs.

To interface between the input buffer and VGA, a level shifter [16] was needed, because the shift in common mode DC voltage caused by the emitter followers in the input stage is too large, and will cause the input of the VGA to clip. It was implemented using a parallel RC network (R_{ls} = 2 kΩ, C_{ls} = 250 fF) in combination with a tunable current source I_{ls} with a nominal value of 100 μA. This combination thus has a low frequency cutoff of 2 GHz. The DC level at the VGA side is determined by the current applied by the source and the voltage at the input stage side, and thus in the nominal case, a 200 mV difference between the two DC levels is observed. For RF, the capacitor acts as a short, which directly passes the AC signal.

Additionally, this level shifter topology can use the tunability of the current source to compensate for possible DC offset between positive and negative output. In this particular application, this function is not used, since the EML is a single ended device and one of the

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differential outputs of the driver is unused. However, if a differential modulator s utilized, the DC offset can be sensed in the output stage, and a feedback loop can be employed to vary the current between the positive and negative branches of the level shifter slightly in the opposite direction, which makes the offset disappear.

To make optimal use of the increased breakdown voltage while not unnecessarily increasing the power consumption of the driver, only the supply of the main differential pair of the BVD was increased to 4 V, compared to 2.5 V for the auxiliary differential pair, the other stages and auxiliary blocks like current mirrors and the DC offset loop.

A final measure taken to ensure that the driver and the PIC are properly co-designed is the fact that the internal termination resistor $R_{L,o}$, is reduced to 30 Ω in order to minimize the RC product of this resistor and the capacitance the EAM presents. Additionally, 110 nH parallel peaking inductors L_p have been added and the load impedance of the auxiliary path (R_A = 30 Ω, C_A = 500 fF) is tuned such that the signals from both the main path, through Q_5 and Q_6, and the auxiliary path, through Q_9 and Q_{10}, interfere constructively at the cascode transistors Q_7 and Q_8 [12]. All of this, in combination with a matching circuit to absorb pad capacitance and interconnect inductance, allows the driver to have a bandwidth in excess of 30 GHz, supporting symbol rates of more than 56 GBd.

The bias voltage for the EAM is applied to a bond pad on the EIC and is then connected to the PIC next to the signal pads, to ensure that the high frequency path the signal has to take is as small as possible. Since this DC voltage can be several volts higher than the output stage supply voltage, special care was taken to ensure that no oxide layer can break down. This was done by routing the ground and bias voltage nets on different metal layers and by spacing their tracks far enough apart. This also means that no ESD protection circuitry is present on this bias voltage net, which is not an issue since there are no transistors on this net, and that the on-chip decoupling is only done with metal-insulator-metal (MIM) capacitors, since only those are able to withstand the high bias voltage. Everything considered, the maximum possible applied bias voltage without breakdown is 15 V.

Finally, the driver has an Serial Peripheral Interface (SPI) interface with some digital registers, to be able to vary the bias currents of each stage, gain and peaking of the VGA. All elements that can be varied through this interface have been drawn with a variable arrow in Fig. 1. The default startup behavior of the registers is set up such that the main output branch draws about half of its nominal current. This was done to assure that some current is always able to flow, even when there are some unexpected startup conditions.

An important factor to consider when interfacing the EML and the driver ICs is the fact that the EML's EAM produces a non-negligible amount of photocurrent when absorbing photons, similar to a photodetector. In [17], the EAM's photocurrent is extensively discussed, alongside the possible solutions that can be taken to connect the EAM in a differential way to the driver. Their solution however, while elegant, is still quite susceptible to the presence of photocurrent. The co-integrated EML presented in this work can generate about 10 mA of photocurrent, depending on the laser power which can be beyond 10 mW for a DFB current of 100 mA. Since the EML requires a relatively low voltage swing to have a sufficient ER, a choice was made to connect it single-endedly to the driver.

To check what the impact of connecting the EAM like this is, a simulation using the schematic of Fig. 5(a) was performed, replacing the EAM by an 80 fF capacitor in parallel with a current source. The resulting voltage for different photocurrents at the single-ended output of the driver can be seen in Fig. 5(b). From the figure, it is clear that the eye quality changes negligibly, the only difference that is observed is a change in DC-level of the output.

As long as the voltage at the cathode of the EAM is higher than the supply of the output stage, the generated photocurrent will flow through the termination resistor of the output stage into the supply, as annotated with red arrows in Fig. 5(a), effectively reducing the current through that

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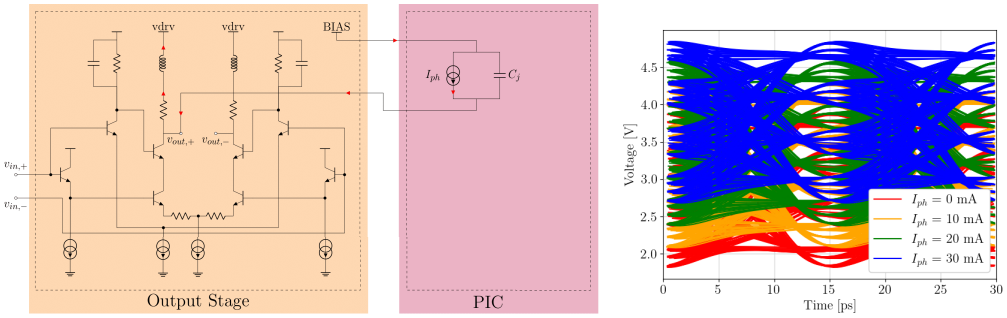

(a) (b)

Fig. 5. (a) Schematic of driver output stage and electrical equivalent of PIC, photocurrent annotated in red. (b) Simulation of effect of photocurrent on output of driver IC.

resistor and onsequently increasing the DC-level of the output. A possible danger with this is the fact that the collector-emitter voltage V_{CE} of the cascode transistor also increases, potentially above its breakdown voltage, but as long as the base of that transistor is driven by a relatively low impedance, as is the case for the BVD, that breakdown voltage is much higher than the effective voltage across it [18].

From the perspective of the EAM, its anode voltage will be lowered. Since the cathode voltage of the EAM is completely separated, it is straightforward to adjust this cathode voltage to circumvent the change in anode voltage.

3. Measurements

In order to analyze the performance of the combined EML and driver, they were mounted on a Printed Circuit Board (PCB) and wirebonded appropriately. To combat thermal issues, the PCB was outfitted with an aluminum (passive) cooling block. However, the bulk contacts of the EIC and the PIC are at a different electric potential. The bulk contact of the PIC is the common cathode of all diodes it contains. To reverse bias the EAM properly, it should thus be at a higher voltage than the anode of the EAM, which is DC coupled to the output of the driver. In contrast, the bulk contact of the EIC is connected to all ground pins of the chip. To prevent a short-circuit of these contacts, the PIC was mounted on a silicon spacer, which is thermally but not electrically conductive, and is itself mounted on the aluminum cooling block. The experiments that follow were conducted at room temperature, without active temperature control. An infrared camera did not show temperatures in excess of 30 °C. A microscope image of the packaged EML PIC and driver EIC can be seen in Fig. 6.

An electrical signal generated by a 92 GSa/s Arbitrary Waveform Generator (AWG) was applied to the input pads of the driver using 67 GHz GSSG RF probes, while the optical output signal was retrieved using a tapered fiber probe with spot size of 5 μm. This optical signal was converted by a Thorlabs' RXM42AF optical receiver featuring a bandwidth of 42 GHz and adjustable transimpedance gain. The receiver output was then applied to a 50 GHz sampling oscilloscope.

The optimal bias point of the EML was in this case decided by the point with minimal Level Mismatch Ratio (R_{LM}). As can be seen in Fig. 3(b), the linear range of the EAM is limited, especially for temperatures closer to 30 °C. Because of this, the drive signal was required to be relatively small. Conveniently, the digital registers allowed the driver to adapt its output swing accordingly. For the default SPI settings, the DC output of the driver is 3.5 V and the applied bias voltage to be in the linear range of the EAM extinction ratio is 4.8 V. For the nominal settings, since there is more DC current flowing through the on-chip termination resistors, the DC output

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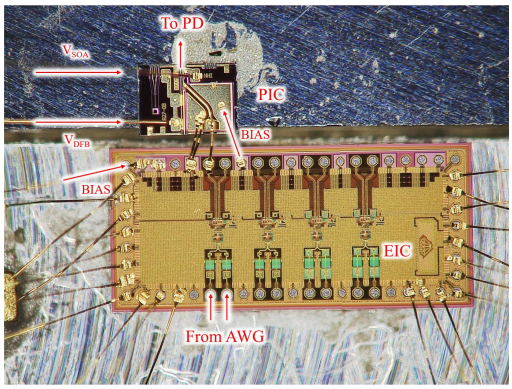

Fig. 6. Microscope image of packaged driver and EML.

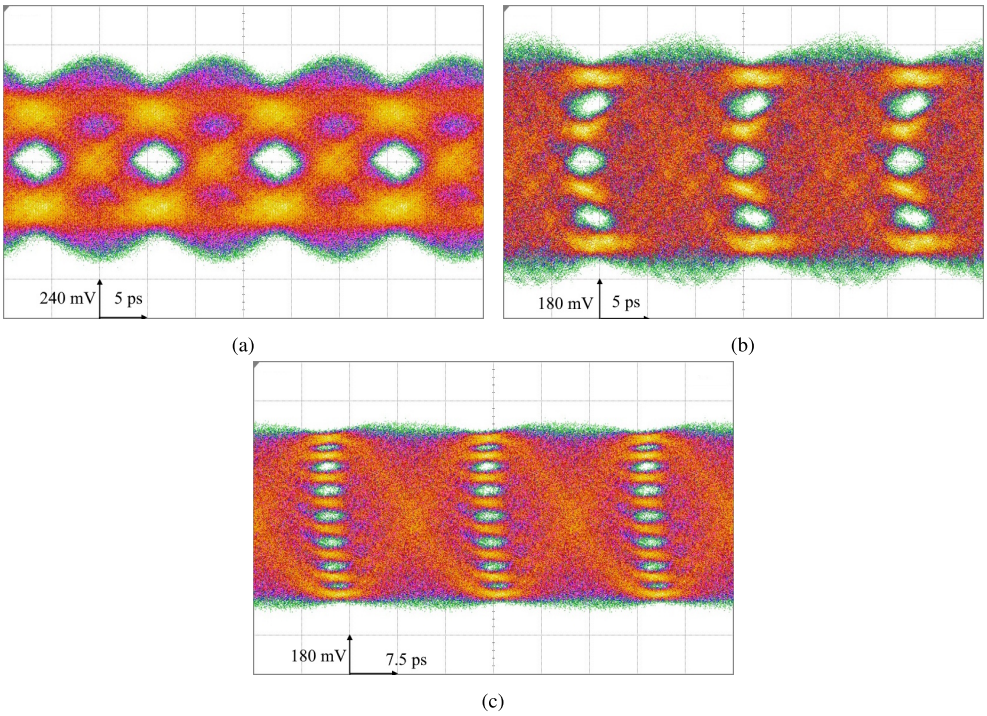

Fig. 7. Eye diagrams for (a) 80 GBd Non Return to Zero (NRZ), (b) 60 GBd PAM4, (a) 40 GBd 8-level Pulse Amplitude Modulation (PAM8), 5-tap feedforward equalisation used for all.

of the driver is about 3 V and thus the optimal common cathode voltage (BIAS in Fig. 1) was lower, 4.4 V.

The DFB laser and the SOA were powered using a Source Measurement Unit (SMU) in order to accurately control the current through these devices, I_{DFB} and I_{SOA} respectively. Initially, these currents were set at 100 mA and 20 mA.

First, the measured dynamic ER for the driver-EML assembly was compared to the ER measured on solely the EML (see Fig. 3). Under default settings, the expected output voltage of the driver is 750 mV. The measured ER with these settings was 4.78 dB, so this measures up to

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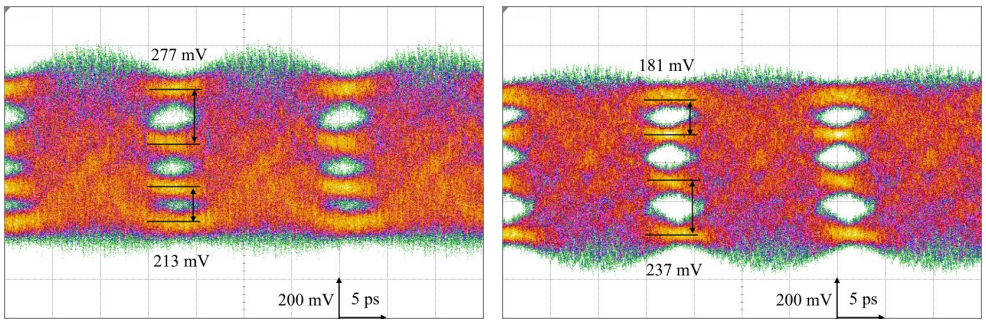

(a) (b)

Fig. 8. Eye diagrams for 56 GBd PAM4 (a) reverse bias voltage over EAM: 1 V, lower eye closing (b) reverse bias voltage over EAM: 2.2 V, upper eye closing, 5-tap feedforward equalisation used for both.

the graph of Fig. 3(b). With nominal, full-current settings, the driver output swing is expected to be 1.5 V, and the measured ER is 7.92 dB. While this is certainly an improved ER figure, this increase is at the expense of the eye linearity due to compression of the outer eyes. Because of this, the following experiments were done with the default settings, which means an output swing of 750 mV.

The eye diagrams for 80 GBd NRZ, 60 GBd PAM4, 40 GBd PAM8, can be seen in Fig. 7. To compensate for the frequency roll-off associated with the test equipment (AWG and optical receiver) and test fixtures (cables and probe), a basic 5-tap feedforward equalizer was used to depict the eye diagrams. In these experiments, the driver consumed 1200 mW, which amounts to 300 mW per channel. The DFB laser consumes 100 mA out of a 1.5 V supply, while the SOA consumes 20 mA out of a 1.2 V supply, and the EAM sources 10 mA out of the 4.4 V bias voltage supply. Together, the EML PIC amounts to a power consumption of 218 mW. As discussed above and as seen in Fig. 7, the 10 mA of photocurrent induced by the EAM forms no obstacle for a clean eye diagram.

To show both the capability of the driver EIC to change the bias voltage over the EAM independently of the RF modulation and the dependence of the EAM on its reverse bias voltage, this voltage was swept from 0 to 6 V (which means the bias net is swept from 3 to 9 V). Only for reverse EAM bias voltages between 1 V and 2.2 V, a distinguishable eye was present. In Fig. 8(a), it is clear that the bottom eye is compressed, which indicates that the bias voltage is too low to be optimal for linearity. In Fig. 8(b), the opposite can be observed, although to a lesser degree.

4. Discussion

In Table 1, the proposed transmitter is compared to other recently published O-band transmitters [19–23]. Note that the effective data rate of all transmitters presented is similar, while the power efficiency of this work's transmitter (incl. laser and SOA) is the highest and the ER is significantly higher thanks to the III-V EML technology.

It also needs to be addressed that [19,21] have presented quad channel versions of their devices, which will boost the overall data rate of their solution when compared to the one presented here. However, the driver has already been designed with this in mind. The worst case crosstalk observed during driver electrical-only measurements is -40 dB, due to to the differential implementation of the data path and >1 nF on-chip decoupling, so designing and including a quad-channel EML is enough to make this solution competitive in this regard, then being able to transmit at 480 Gb/s.

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Table 1. Comparison to state of the art O-band transmitters

	This work	VLSI 2021 [19]	JLT 2025 [20]	JSSC 2024 [21]	OFC 2022 [22]	PTL 2025 [23]
Symbol Rate per Channel [GBd/λ]	60	56	128	56	64	50
Modulation scheme	PAM4	PAM4	NRZ	PAM4	PAM4	NRZ
EIC process	130nm SiGe BiC-MOS	28nm CMOS	28nm CMOS	180nm SiGe BiC-MOS	130nm SiGe:C BiC-MOS	28nm CMOS
Modulator type	EAM	MRM	dual-segment MRM	MZM	EAM	EAM
PIC process	InGaAlAs MQW	SiPh	220 nm SOI SiPh	180nm SOI SiPh	-	-
ER [dB]	7.92	2.7	3	5	2.5	7.0
Total power consumption per channel [mW]	518excluding laser power	650[a]	665[a]	538[a]	240[b]	373[b]
Power Efficiency [pJ/bit]	4.3[a]	5.8[a]	5.2[a]	4.8[a]	1.88[b]	7.64[b]

[a]including laser power
[b]excluding laser power

5. Conclusion

In this paper, a fully operational O-band transmitter based on an InGaAlAs MQW EML and SiGe BiCMOS driver is demonstrated. The transmitter is sufficiently linear to be able to send PAM8 signals at 40 GBd and sufficiently fast to send NRZ signals at 80 GBd, while it has an excellent power efficiency of 4.3 pJ/bit when transmitting PAM4 signals at 60 GBd. The EML is able to modulate light with an ER of almost 8 dB and the driver is able to withstand more than 10 mA of photocurrent without noticeable eye degradation. Since the driver is a quad-channel device already, the total throughput of the transmitter can be scaled to 480 Gb/s by co-integrating a quad version of the EML.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

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