A Duty-Cycle Switching 30-Gb/s Burst-Mode CDR With 1.6-ns Locking Time in 28-nm CMOS

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***Abstract*— This article presents a closed-loop type burst-mode clock and data recovery (BM-CDR) circuit with fast phase offset detection using 8/3x-fractional oversampling in the periodic preamble. The proposed phase offset detector achieves a resolution of 1/8 unit intervals (UIs) with a detection time of 4 UIs. A 2x-oversampling closed-loop bang-bang CDR is performed after the phase offset detection to provide jitter filtering. The switching between these two different oversampling ratios is realized in a single multi-phase clock generator (MPCG) by changing the duty-cycle in four differential quarter-rate clocks. Furthermore, fast duty-cycle switching (DCS) is introduced in the injection-locked ring oscillator (ILRO) design to speed up the transition from one sampling ratio to another. A prototype fabricated in 28-nm CMOS achieves a locking time of 1.6 ns at 30-Gb/s data rate, a BER of 1E-12 with a recovered clock integrated rms jitter of 398.4 fs. The jitter tolerance curve shows a corner frequency around 20 MHz with a 20-dB/dec slope in the low-frequency region. The receiver including the proposed CDR consumes 75.53 mW with 0.9-V supply and occupies an area of 0.148 mm^2.**

***Index Terms*— Burst-mode clock and data recovery (BM-CDR), closed-loop, duty-cycle switching (DCS), fractional oversampling, injection-locked ring oscillator (ILRO), jitter filtering, multi-phase clock generator (MPCG), phase offset detector.**

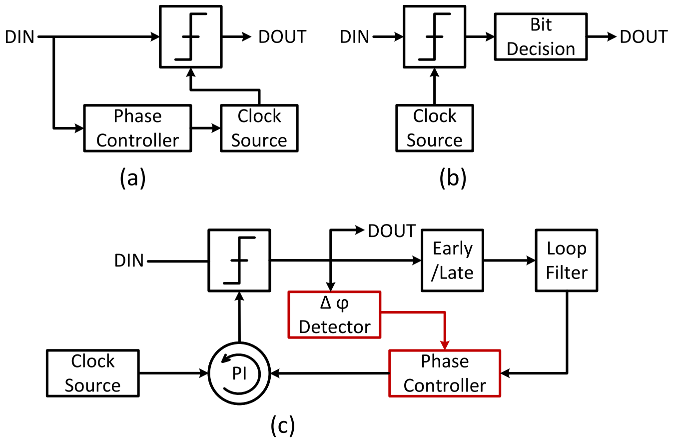

Fig. 1. Three types of BM-CDR architecture overview. (a) Type-A. (b) Type-B. (c) Type-C.

I. INTRODUCTION

THE surge in artificial intelligence applications has generated new demands for burst-mode (BM) data transfer in data centers [1], [2], [3] and high-performance computing systems [4], [5], [6]. Applications such as non-blocking optical packet switching and configurable wafer-level GPU interconnection have been studied at the system level to evaluate the performance in terms of bandwidth and power consumption. The traffic in the data center and GPU interconnection is different from that in traditional BM links used in the passive optical networks (PONs), where, taking 25G/50G-EPON as an example [7], the payload can be as long as 1799 B. The minimum packet size in data center traffic is 64 B [8]. The burst nature and very short traffic require reduced preamble sizes, which are essential for maintaining high utilization of the system throughput, thereby necessitating a fast locking clock and data recoveries (CDRs). A CDR locking time of 4 ns already limits the utilization of the network throughput to around 75% [8].

Conventional closed-loop CDRs without fast phase offset detection have a locking time limited to tens of nanoseconds by the loop bandwidth [9], [10], [11]. To achieve fast phase locking, specialized BM-CDR is needed. In general, the BM-CDRs can be divided into two categories. Open-loop types as (a) and (b), shown in Fig. 1, and closed-loop type as (c) in Fig. 1. Phase controlling in Type-A can be done with multiple techniques such as gated-VCOs [12], [13], injection of extracted data edges into the clock source [14], [15], or phase interpolation on two reference phases using data edge sampling [16]. In Type-B, input data is over-sampled by the clock source, and then the bit decision logic is applied to select the correct bit [17], [18]. Thanks to the open-loop operation, these open-loop CDRs can offer shorter locking times but lack jitter filtering. Additional circuitry or data processing is implemented to achieve input jitter filtering in Type-B [17], [18]. An alternative approach shown in Type-C involves detecting the phase offset at the beginning of the packet with the loop opened, followed by shifting the clock

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to the optimal sampling position before closing the loop with the help of the phase controller. In this way, fast locking is achieved while the system can still benefit from the filtering properties of a closed-loop type CDR.

To detect the phase offset between the ideal sampling point of the incoming data and the local sampling clock with a bang-bang phase detector (BBPD), at least two samples per unit interval (UI, equals to a single symbol period T) are required. The accuracy of the detection can be improved by increasing the number of samples within 1 UI. The locking time of a closed-loop type BM-CDR can be expressed as the sum of the open-loop phase offset detection time t_{det}, open-loop to closed-loop switching time t_{msw}, and the closed-loop locking time t_{cl}

$$t_{\mathrm{lock}} = t_{\mathrm{det}} + t_{\mathrm{msw}} + t_{\mathrm{cl}}. \tag{1}$$

The phase offset detection time t_{det} is determined by the required accuracy. The mode switching time t_{msw} depends on how the switching from open-loop to closed-loop is realized. The closed-loop locking time t_{cl} is determined by the loop slew rate and the residual phase offset after detection. It is a challenge to achieve a t_{cl} less than 100 UI. By reducing the residual phase error to a level smaller than the half of eye-opening for error free data receiving, the impact of t_{cl} on data recovery is removed. As a result, the t_{lock} is dominated by t_{det} and t_{msw}. Unfortunately, with a limited number of sampling phases, the detection time increases since more time is needed to increase the samples to achieve the necessary accuracy. In [19] and [20], the phase offset detection is realized by sweeping a phase rotator, while in [21], it is done by introducing a frequency offset. The sequential phase acquisition process for phase offset detection in these designs results in a trade-off between the accuracy of the phase offset detection and the phase locking time. It is not hard to relate Type-B with Type-C architecture when a large oversampling ratio in Type-B is employed. The sample results in 1 UI in Type-B can be used for the input phase offset detection, and the bit decision is replaced by the closed-loop CDR part in Type-C.

This article proposes a new fast phase detector using duty-cycle switching (DCS) of the sampling clocks in a quarter-rate CDR, which effectively implements fractional oversampling of a periodic preamble. This overcomes the trade-off between locking time and phase offset detection accuracy and achieves 1/8 UI resolution with 4 UI detection time. A DCS multi-phase clock generator (MPCG) is introduced to expedite the transition from phase detection to phase tracking. Section II discusses the fractional oversampling method for phase offset detection. Details of the receiver architecture and the circuit implementations are described in Sections III and IV. Experimental results are presented in Section V, followed by a conclusion and comparison to prior works in Section VI.

II. PHASE OFFSET DETECTION-USING FRACTIONAL OVERSAMPLING

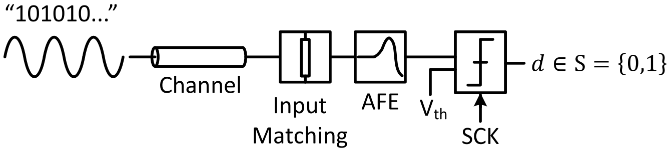


Fig. 2. Representation of the sampling on the preamble.

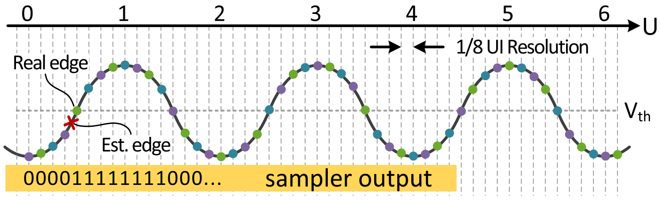


Fig. 3. Phase offset detection with 8x-oversampling.

In a BM receiver, the phase offset is detected during the reception of a so-called preamble, which is a customized pattern at the beginning of the burst. A clock pattern ("1010") is common in BM links. It has been demonstrated in the gain and dc offset calibration of a BM transimpedance amplifier (BM-TIA) [22], and the phase detection in a BM-CDR [19], [20], [21]. In this article, a "1010" C2 clock pattern is used in the preamble. Owing to the periodicity of the preamble, the same information can be obtained by sampling the preamble with multiple phases during 1 UI or by sampling it over multiple UIs with fewer phases. For example, using 8x-oversampling in 1 UI with eight phases realizes the same resolution as 8/3x-oversampling during 6 UIs with 16 phases. The proposed method uses such fractional oversampling implemented using the eight phases present in a quarter-rate CDR to achieve the same resolution as an 8x-oversampling configuration but over a 4 UI sampling window.

A. 8x-Oversampling

To show how the fractional oversampling works, it is worth looking at the 8x-oversampling first. Fig. 2 shows the sampling on a preamble with a "1010" pattern. The signal chain consists of a channel, an on-chip input matching network, an analog front end (AFE), and a sampler driven by the sampling clock. Since the clock pattern toggles every data period, the falling or rising edge can represent the edge position in the payload. The output of the sampler d is a series of 0 and 1, depending on the sign of the difference between the signal and the threshold voltage V_{th}. The edge can be represented by the position where the output changes from 0 to 1 or 1 to 0. In other words, the position of the edge is estimated in the middle of two consecutive sampling phases where the output data pattern has a transition. Fig. 3 shows the input clock pattern in 6 UIs and all the sampling positions of 8x-oversampling. The edge position (rising edge in the first UI in this case) occurs between 3/8 UI and 4/8 UI and is estimated at 3.5/8 UI. However, the real edge transition is at 0.5 UI. Thus, the phase offset detection with 8x-oversampling has a resolution of 1/8 UI, and the maximum detection error is 1/16 UI.

B. 8/3x-Oversampling

8/3x-oversampling on the predefined "1010" clock pattern is shown in Fig. 4. Since the sampling frequency is three times

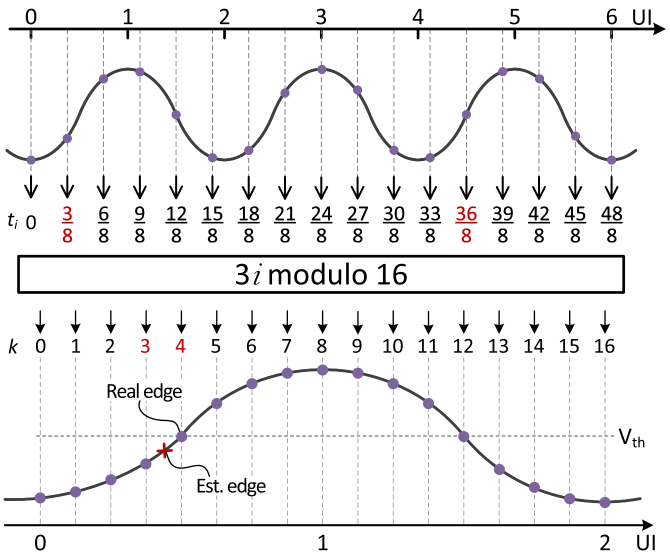


Fig. 4. 8/3x-fractional oversampling with timing re-ordering.

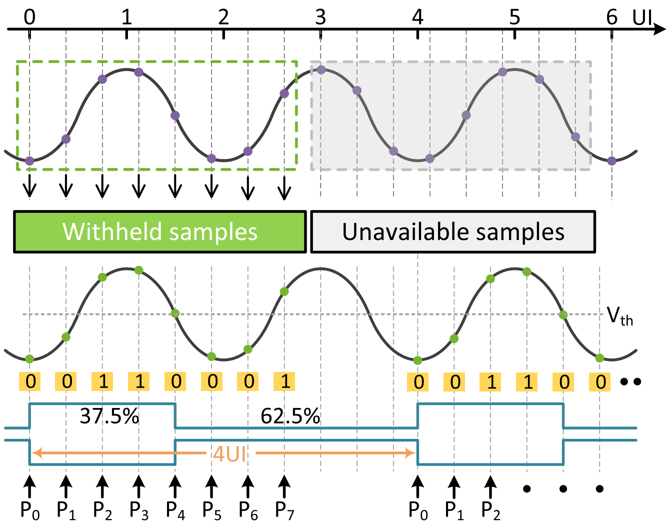


Fig. 5. Proposed 8/3x-fractional oversampling with limited phases.

slower than 8x-oversampling, the number of sampling phases in 6 UIs reduces from 48 to 16. The clock pattern in the preamble has a period of 2 T and the sampling clock has a period of 3/8 T. Since the least common multiple of 2 and 3/8 is 6, these 16 sampling instants are at different positions within a single clock pattern for 2 UI. To clarify this, the sampling instant of each phase is marked as t_i, where

$$t_i = \frac{3i}{8}, i \in S, S = \{z \in \mathbb{Z} \mid 0 \leqslant z \leqslant 15\}. \tag{2}$$

The residue of $3i$ divided by 16 forms an index set k_{index}, where k_{index} is defined as

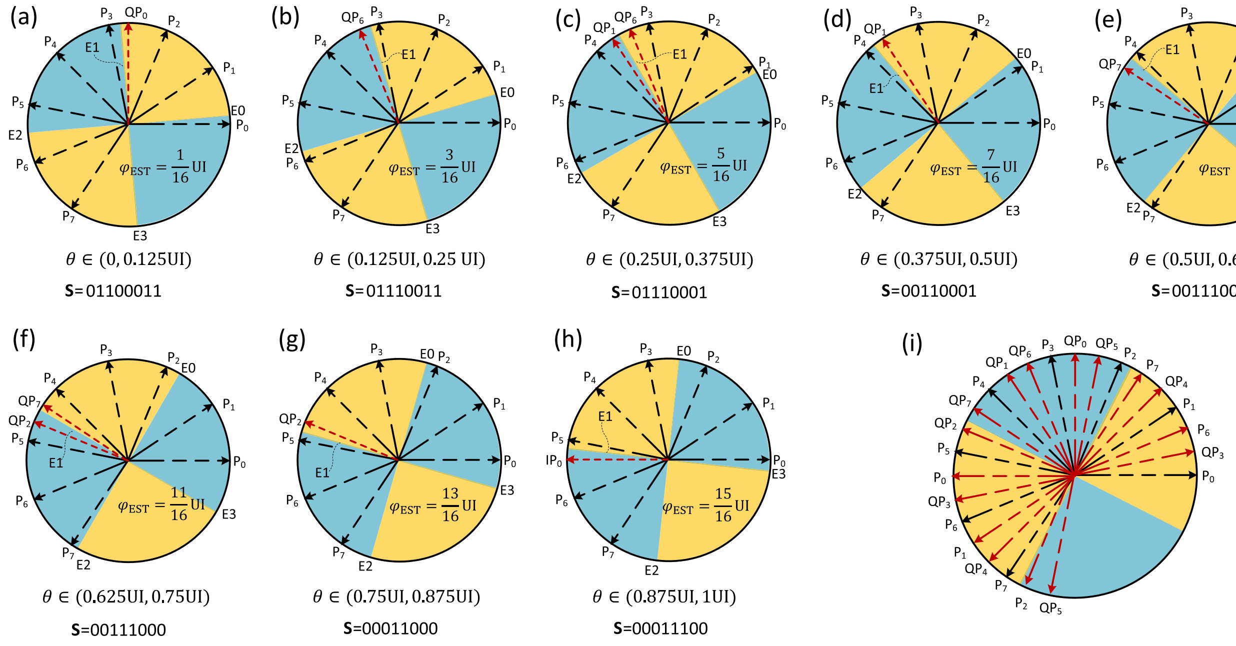
$$k_{\text{index}} = \{k \mid k = 3i \bmod 16, k \in S\}. \tag{3}$$

Within 6 UIs, each sampling point t_i uniquely corresponds to one element in k_{index} after the modulo operation, and the index k suggests the order of the samples in the reconstructed eye shown in the bottom part of Fig. 4. After the reordering, the transition of 1–0 or 0–1 in the reconstructed eye is used to estimate the edge position. Taking the rising edge, for example, the 0–1 transition happens when k equals 3 and 4, where t_i equals 3/8 and 36/8 UI, respectively. The estimation edge in the middle is 3.5/8 UI. Hence, the resolution and maximum detection error remain the same as 8x-oversampling, but the detection time increases to 6 UIs.

C. 8/3x-Oversampling in Quarter-Rate CDR

In the previous discussion, 16 samples are needed to reconstruct the eye of the input clock pattern in the general 8/3x-oversampling case. To implement such a scheme, eight different phases are required with a frequency of 1/3 of the data rate. A quarter-rate CDR already implements eight phases, however, their frequency equals 1/4 the data rate. To enable sampling of the data with 1/8 UI resolution and maximum estimation error of 1/16 UI similar to in the general 8/3x and 8x-oversampling, a duty-cycle variation is introduced on the eight phases of a quarter-rate CDR. As shown in Fig. 5, the first eight samples in the green dash box from the general 8/3x-oversampling are withheld by the available phases, while the other samples in the gray shaded box are not available due to the limited number of sampling phases. The reserved samples are denoted by eight phases (P0–P7) with a 3/8 UI incremental phase step, and the resulting pattern, 00110001 in this case, repeats every 4 UI. The 3/8 UI phase spacing is achieved by adjusting the duty-cycle of the four quarter-rate (C4) differential clock pairs available in a quarter-rate CDR to 37.5%. The following analysis shows that the input phase offset can still be detected using only the data acquired by these 8 phases.

The edge estimation using only eight phases is illustrated in the phasor diagrams in Fig. 6. When the sampling frequency is synchronized with the input data rate, the positions of P0–P7 are fixed in the phasor diagram with a 3/8 UI spacing, while the data edges (E0–E3), which represent the boundaries between the yellow (logic 1) and blue (logic 0) regions, can be anywhere in this circle due to the random phase offset between the incoming data and the sampling clock at the beginning of a burst. The phase between data edges is fixed at 90° (1 UI). For simplicity and without loss of generality, P0 is set at 0° with phase increasing counterclockwise. As the phase offset between P0 and E0 increases from 0 to 2 UI, 16 different cases can be derived; eight of them are shown in the figure. The data pattern 01100011 in Fig. 6(a) indicates that P0 samples logic 0; hence, E0 leads P0, and E1 leads QP0 (the quadrature phase of P0). On the other hand, P3 samples logic 0; thus, P3 leads E1. Consequently, E1 falls between QP0 and P3, resulting in an estimation of E0 at 1/16 UI. As the input data phase increases, the following data pattern is 01110011, as shown in Fig. 6(b), indicating that P3 samples logic 1, so E1 leads P3. Meanwhile, P6 samples logic 1, meaning QP6 (the quadrature phase of P6) leads E1. Therefore, E1 should fall between P3 and QP6, leading to an estimation of E0 at 3/16 UI. The complete analysis across 1 UI phase offset gives another six different patterns, as shown in Fig. 6(c)–(h). The pattern keeps changing from 1 to 2 UI, but



$\theta \in (0, 0.125\text{UI})$ **S**=01100011
$\theta \in (0.125\text{UI}, 0.25\ \text{UI})$ **S**=01110011
$\theta \in (0.25\text{UI}, 0.375\text{UI})$ **S**=01110001
$\theta \in (0.375\text{UI}, 0.5\text{UI})$ **S**=00110001
$\theta \in (0.5\text{UI}, 0.625\ \text{UI})$ **S**=00111001
$\theta \in (0.625\text{UI}, 0.75\text{UI})$ **S**=00111000
$\theta \in (0.75\text{UI}, 0.875\text{UI})$ **S**=00011000
$\theta \in (0.875\text{UI}, 1\text{UI})$ **S**=00011100

Fig. 6. Phase estimation utilizing pattern information. Here, θ represents the input phase offset, **S** denotes the detected pattern, and φ_{EST} is the estimated edge position. (a)–(h) Detected pattern as edge rotates from 0 phase offset to 1 UI phase offset. (i) Combination of all positions, indicated by the various detected data patterns.

it is simply the ones' complement version of the previous eight data patterns. Finally, the combined phasor diagram shown in Fig. 6(i) displays all positions indicated by the various data patterns, giving a resolution of 1/8 UI for any input phase offset.

D. Maximum Estimation Error

Because the phase offset is estimated using the combined information obtained using eight different sampling phases over 3 UI, the duty-cycle variation, frequency offset, and jitter will influence the phase offset estimation error by altering the sampling result.

1) Duty-Cycle: Denote the duty-cycle of the clock as α, where $\alpha \leq 0.5$, then the phase spacing between two consecutive sampling phases is α UI, and the oversampling ratio equals $1/\alpha$. The patterns shown in Fig. 6 give two conditions for the phase spacing to satisfy

$$\begin{aligned} 5 \cdot \alpha \cdot \text{UI} &< 2 \cdot \text{UI} \\ 3 \cdot \alpha \cdot \text{UI} &> \text{UI}. \end{aligned} \tag{4}$$

To solve these inequalities, the duty-cycle needs to satisfy the following conditions:

$$33.3\overline{3}\% < \alpha < 40\%. \tag{5}$$

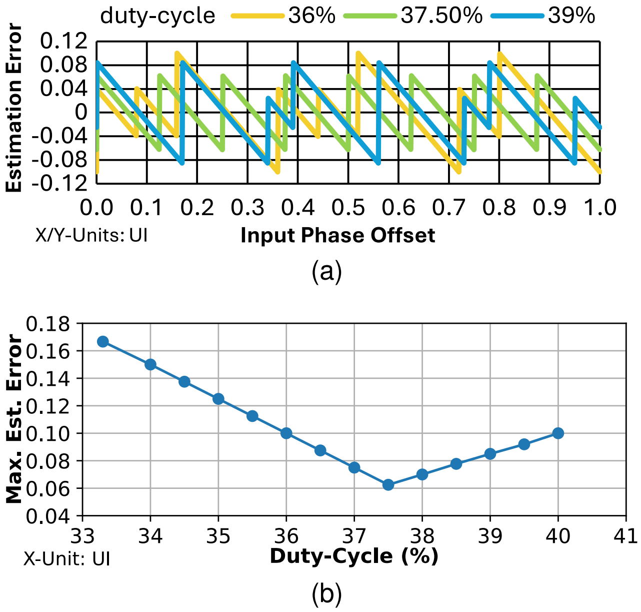
The set of the data pattern remains unchanged when the duty-cycle changes within the range in (5). But it does change the estimation position of the edge. The simulation result of the estimation error across input phase offset associated with three different duty-cycles is plotted in Fig. 7(a). The estimation error curves have sawtooth shapes and show up with different peak values in the cases of 36% and 39%. The duty-cycle of 37.5%, corresponding to an oversampling ratio of 8/3, has a maximum estimation error of 0.0625 UI (1/16 UI) shown in the green curve, which matches the previous analysis. The maximum estimation error across duty-cycle is plotted in Fig. 7(b), the maximum estimation error increases to 0.1667 and 0.1 UI for duty-cycle of $33.3\overline{3}\%$ and 40%, respectively. Notably, the duty-cycle distortion on the data has the same effect as the duty-cycle variation in the sampling clock. That indicates a potential solution of correcting the duty-cycle distortion in the data by tuning the duty-cycle of the clock.

2) Frequency Offset: As shown in Fig. 8, the sampling clock samples the preamble with an adjacent phase spacing T_s. When the START signal toggles to high, the look-up table (LUT) will latch the pattern and generate the corresponding offset code D_{OS} for the phase interpolator (PI). With a duty-cycle of α, and a clock period of T_{ck}, the phase spacing can be expressed as

$$T_s = \frac{\alpha T_{\text{ck}}}{4}. \tag{6}$$

When the clock frequency is synchronized with the input data, $T_{\text{ck}} = 4$ UI. If the duty-cycle equals to 37.5%, the phase spacing $T_s = (3/8)$ UI. It is clear from (6) that both duty-cycle and frequency can change the sampling phase spacing in the preamble mode. So, in terms of pattern sampling, frequency mismatch has the same effect as duty-cycle variation. It is equivalent to a duty-cycle of $(1+\beta) \times \alpha$ with a frequency offset of β.

Before the loop closes when switching from preamble to the normal mode. The clock is shifted by D_{OS}, and in the worst case, half period of T_{CK}. After the shifting, the rising edge of CK<0> has a $0.5\Delta T$ offset with the edge of data. The phase difference will further accumulate because of the



(a)

(b)

Fig. 7. (a) Estimation error at different input phase offsets. (b) Maximum estimation error across duty-cycle.

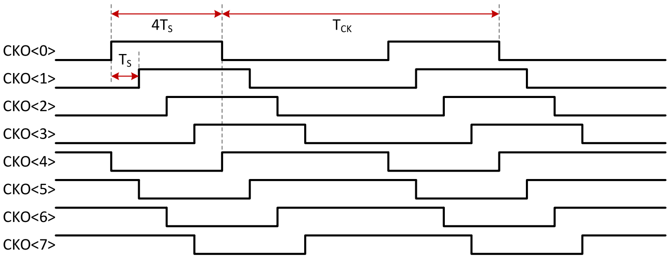


Fig. 8. Sampling clock waveform in the preamble mode.

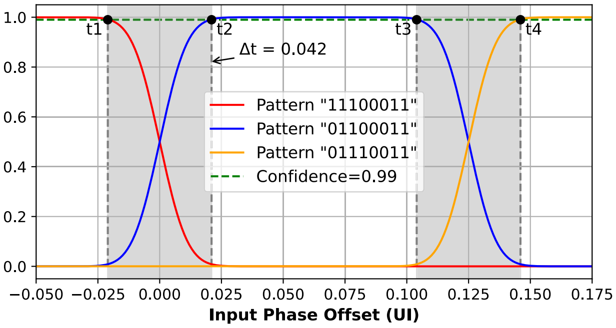


Fig. 9. Pattern probability when $A = 100$ mV and $\Delta t_i = 300$ fs.

frequency difference until the loop closes. Calculation shows a frequency offset from −735.7 to 749.7 ppm resulting in a maximum phase error less than 0.1 UI. After the loop is closed, the CDR can track the frequency variation on the transmitter side. To track a larger initial frequency offset, a closed-loop with an on-chip oscillator is needed.

3) Sampling Clock Jitter: The jitter in the sampling clock can introduce sampling error when the sampling happens at the position where the signal swings close to the threshold voltage of the sampler. Suppose the eight phases located at t_i, where

$$t_i = \frac{3i}{8}T, \quad i = 0, 1, 2 \ldots 7. \tag{7}$$

T equals 1 UI, and each clock phase drives one sampler. The clock pattern in the preamble is represented by a sinusoidal waveform

$$x(t) = A \sin\left(\frac{\pi}{T}(t - t_o)\right) \tag{8}$$

where A is the amplitude of the clock and t_o is the input phase offset. The signal present at the ith sampler is

$$x_i = A \sin\left(\frac{\pi}{T}(t_i - t_o)\right). \tag{9}$$

The sampling of the data happens at different times for different sampling phases. To simplify the analysis without loss of generality, assume the clock jitter Δt_i follows a normal distribution with a mean value of t_i, $\Delta t_i \sim N(t_i, \sigma_j^2)$. The probability when the sampler output equals zero can be expressed as

$$p_i = P(x_i < 0) = P((2k-1)T < t_i - t_o < 2kT) \tag{10}$$

where $k \in \mathbb{Z}$. Furthermore, this can be expressed as

$$p_i = \sum_k \left(F_{\Delta t_i}(2kT + t_o) - F_{\Delta t_i}((2k-1)T + t_o)\right) \tag{11}$$

where $F_{\Delta t_i}(x)$ is the cumulative distribution function of Δt_i. The probability that a pattern of Fig. 6 is detected is

$$P(\text{pattern}) = \prod_{i=1}^{8} p_i^{1-s_i}(1-p_i)^{s_i} \tag{12}$$

$$s_i = \text{sign}\{b_i\} \tag{13}$$

where b_i is the ith bit in one pattern starting from the left. When t_o changes from −0.05 to 0.175 UI, the probabilities of three different patterns are shown in Fig. 9. Each pattern has a maximum probability of 1 in a different region. But when the input offset is close to the sampling phase position, such as 0 and 0.125 UI in this case, two patterns could show up at the output with a probability of P and $1 - P$, respectively. Since the phase offset detection is a one-time sampling, the expectation value is not applicable; the maximum error with a certain confidence level is used as the criteria for design choice. For example, a confidence level of 0.99 threshold line defines two gray regions with a width of Δt. The input phase offset at t_2 could result in a readback pattern of 11100011 with a probability of 1% and an edge estimation of $-1/16$ UI, increasing the maximum estimation error to $1/16\,\text{UI} + \Delta t/2$. The conclusion of the impact of clock jitter applies to the jitter from the input data as the independent assumption. To quantify the jitter requirement of the clock, the probability of the estimation error at different input phase offsets, sweeping from $-1/16$ to $1/16$ UI, with various clock jitter Δt is plotted in Fig. 10. For the zero jitter case, the decision uncertainty only happens when the input phase offset overlaps with the sampling phase when $t_o = 0$. The estimation error only changes the sign while the absolute value remains the same. Thus, the estimation error curve has a rectangle shape, and the decision uncertainty only happens at the edge. But in the non-zero jitter cases, the uncertainty expands from a straight

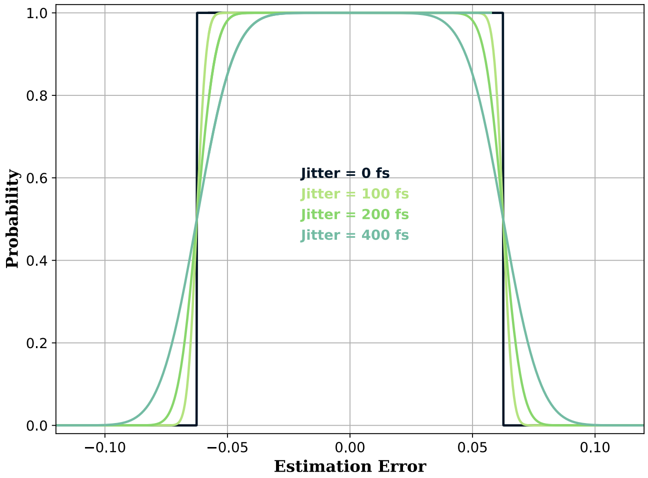


Fig. 10. Estimation error under different clock jitter.

line to a region, and the maximum estimation error increases with Δt. To achieve a maximum error below 0.1 UI with the confidence of $1 - 10^{-5}$ when the input swing is 100 mV, the jitter should be less than 293 fs.

III. RECEIVER ARCHITECTURE

The BM phase alignment is performed in three steps: fast phase offset detection, switching from open-loop detection to closed-loop, and closed-loop phase tracking. In the phase offset detection part, four differential quarter-rate clocks with a duty-cycle of 37.5% need to be generated by an 8-phase MPCG. In the second part, MPCG has to change the duty-cycle of the clock to 50% and it aligns all the edge clocks, namely ck0, ck2, ck4, and ck6, with the edge of the data, while all the data sampling clocks, namely ck1, ck3, ck5, and ck7, align with the center of the eye. Last, the CDR loop is closed to track the phase change with a bang-bang phase detection loop. To switch the duty-cycle in the clock between 37.5% and 50%, a DCS injection-locked ring oscillator (DCS-ILRO) is proposed in this article, which will be described in detail in Section IV-C. To shift the sampling clock based on the phase offset detection result correctly, a phase alignment scheme is applied to the proposed DCS-ILRO.

Fig. 11(a) illustrates the block diagram of the proposed receiver. The main part of the receiver includes an AFE, a sampler array, a clock path, an MPCG, and a digital block. The operation of the BM receiver is divided into two modes, as illustrated in Fig. 11(b): the preamble mode and the normal mode. An external START signal triggers the BM controller (BMC) in the digital block, initiating the phase offset detection state from the idle state. At the system level, this signal can be generated either by an activity detector or a scheduler. It aims to ensure phase detection occurs when the preamble is present at the input. Once triggered, the BMC manages the mode switching via its output signals, FIRE and MODE. During the inter-burst gap, just before the preamble, the receiver remains idle with no input. The CDR_BBPD and the digital loop filter (DLF) are disabled and have zeros at their outputs. The external START remains low, forcing both FIRE and MODE low. MODE controls the configuration of the DCS-ILRO, and when it is low, the four differential quarter-rate clocks P0–P7 at the output have a duty-cycle of 37.5%, resulting in a 3/8 UI phase spacing. When the "1010..." clock pattern in the preamble is presented at the input, it is fractionally over-sampled by P0–P7 successively. The synchronized eight samples move to digital directly waiting for further processing.

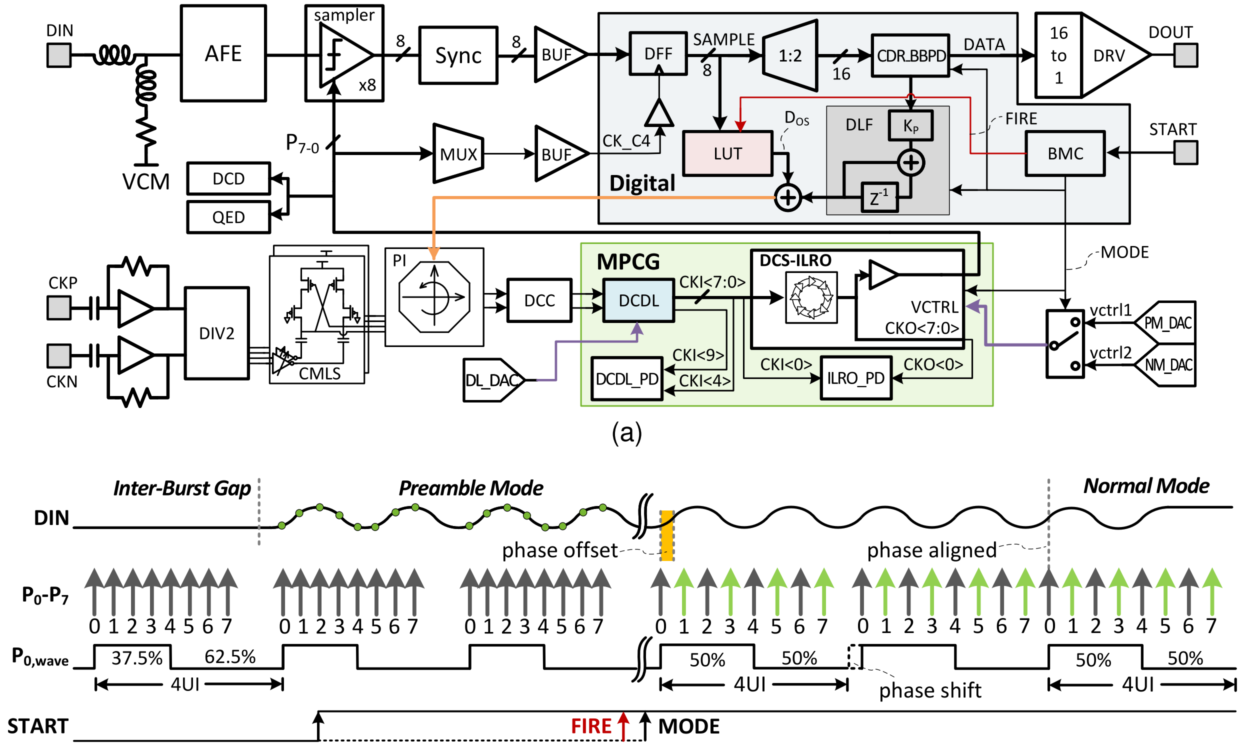
The input of MPCG is generated from a half-rate (C2) differential reference clock, CKP, and CKN, through a clock path [23]. The operation and phase of the clock path and the digital controlled delay line (DCDL) do not change between the operation modes. Furthermore, the proposed DCS-ILRO has a feature, detailed in Section IV-C, which ensures the phase alignment between CKI<0> and CKO<0> in both the preamble and normal modes. This is essential to ensure that the phase difference that is detected in the preamble mode can be reused in the normal mode. The rising edge of START sets FIRE high, enabling the LUT to latch the 8-bit SAMPLE that contains the phase offset information. The corresponding PI code D_{OS} stored inside of LUT presents directly to PI input from the adder since the other input of the adder is zero. The phase at the output of PI shifts with the estimated phase offset, ph_os, according to D_{OS}. This aligns P0 to the edge of the incoming data. After this, the output duty-cycle of DCS-ILRO switches to 50% in the normal mode when MODE toggles to high after FIRE, resulting in a 1/2 UI phase spacing in P0–P7. Consequently, P0, P2, P4, and P6 are aligned with the edges, while P1, P3, P5, and P7 are aligned with the center of the eye. The loop is closed by rotating the PI with the sum of the feedback phase errors and D_{OS} after MODE enables the CDR_BBPD in digital and releases the DLF reset.

By generating the clock in this way, only the DCS-ILRO needs to switch the mode quickly, while the other blocks remain in the same state across both modes. Furthermore, as shown in Fig. 8, switching the duty-cycle to achieve the 3/8 UI phase spacing in preamble mode does not disrupt the differential property of the clock signals, as in the case in normal mode when the duty-cycle is 50%. This characteristic ensures minimal disturbance on the power line, accelerates the switching time, simplifies clock delivery to the samplers, and reduces interference with other blocks.

IV. CIRCUIT IMPLEMENTATION

A. Clock Path

The input differential clock running at half rate with a frequency of 15 GHz is converted by an on-chip ac-coupled buffer to a square wave differential clock. A CMOS latch-based frequency divider similar to [24] generates four quadrature phases at a quarter rate. To drive the current mode PI, the input common-mode voltage from the CMOS divider needs to shift by a common-mode level shifter (CMLS). As shown in Fig. 11, the inverter output is ac-coupled to a cross-coupled pair consisting of PMOS transistors with two 60-fF coupling capacitors. A similar topology can be found in [25]. Here, cascode transistors are added to reduce the coupling between the gate and drain, effectively increasing the speed of the level shifter. Since the divider is shared between



(a)

(b)

Fig. 11. Architecture of the proposed receiver. (a) System block diagram. (b) BM operation sequence.

different channels, the PMOS transistors can be placed close to the PI while the inverters and the coupling capacitors are close to the divider. It is power-efficient to place the long trace in between since the signal on the long trace is not in full swing. The maximum output is fixed at supply, while the minimum output is tuned by changing the inverter strength. Such that the common mode shifts to 0.7 V and the swing is reduced to 0.4 V to maintain a good linearity of subsequent PI. The octagon PI [26] is implemented to improve the phase tuning linearity. The duty-cycle corrector (DCC) is realized by injecting current into a two-stage ac-coupled buffer. The duty-cycle of MPCG input is set to be 50% both in the preamble and normal modes.

B. Digital Controlled Delay Line

A delay-locked loop (DLL) together with a single stage of ILRO can generate a multi-phase clock with high accuracy more efficiently than other implementations [27]. The DCDL consists of 6 identical delay units and one dummy load as shown in Fig. 12. The eight input phases for the DCS-ILRO are generated from the outputs of the second to fifth stages. Each delay unit has two driving inverters with two cross-coupled inverters at the output. The driving inverter consists of one current-starved cell in parallel with a 3-bit binary weighted switchable inverter. The 3-bit switchable inverter provides coarse tuning of the delay while the current starved inverter provides fine tuning. The calibration on the delay starts with the smallest delay setting, and the phase offset between CKI<4> and CKI<9> is monitored by DCDL_PD [28]. The output of DCDL_PD remains high until the delay of the unit cell is increased to the value that zeros the phase difference. In this way, the input of the phase detector is always in the range of $[-\pi, 0]$, avoiding issues related to the limited detection range of DCDL_PD. After the calibration is done, the eight phases are spaced 1/2 UI. This is kept constant during both preamble and normal modes.

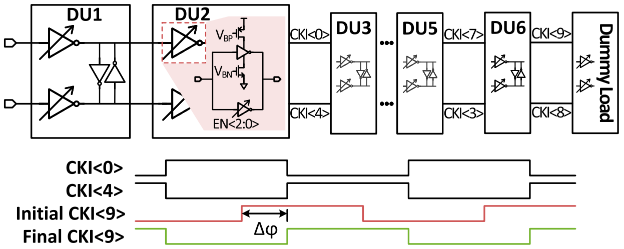


Fig. 12. Circuit of DCDL and the delay calibration scheme.

C. DCS-ILRO

The proposed DCS-ILRO circuit is shown in Fig. 13. It is the critical block of this BM receiver and it should generate four differential output clocks with a duty-cycle of 37.5% and 50% in the preamble and normal mode, respectively, enable fast DCS, and ensure that the input clock CKI<0> and the output clock CKO<0> are phase-aligned between the two modes.

A conventional ring oscillator consists only of delay cells D1–D4, CKO<3> with the output of D4 connecting back to the input of D1. The rising edge of CKO<0> experiences three unit delays, after which it appears at the output of D4

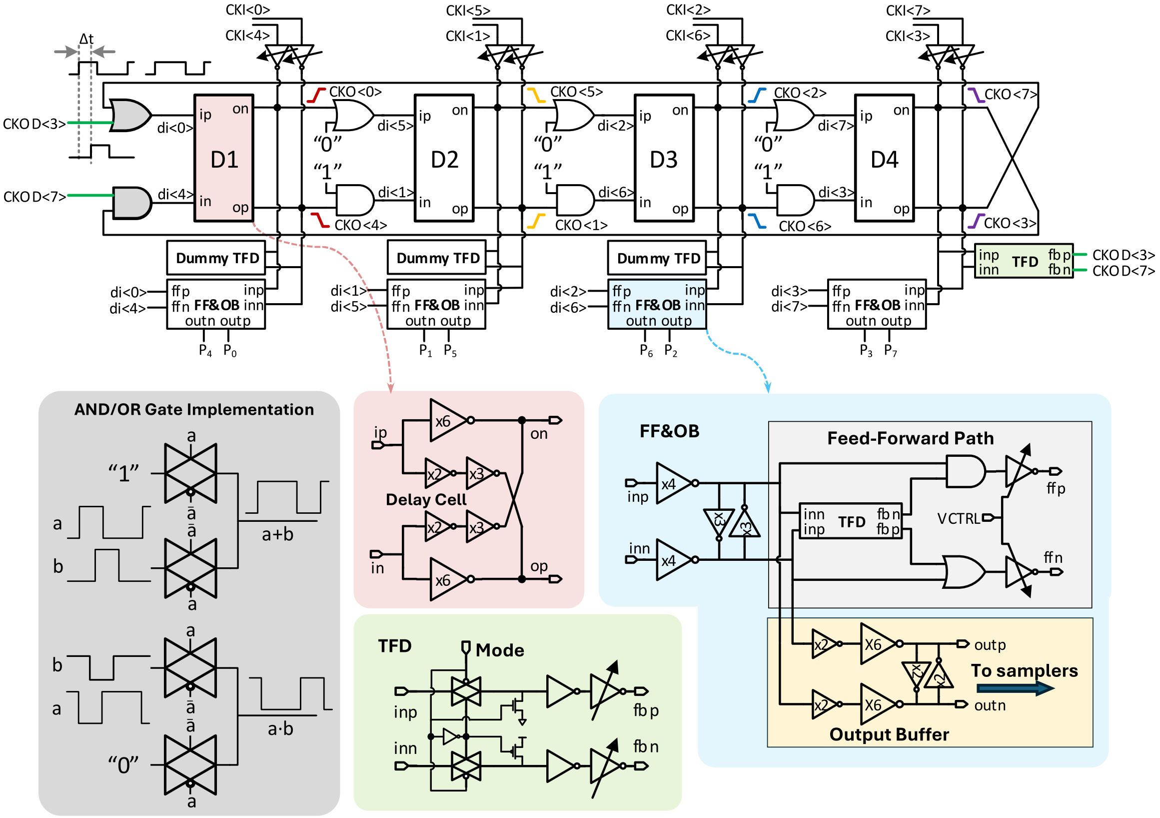


Fig. 13. ILRO with DCS.

as the rising edge of CKO<3>. After one more unit delay in D1, the rising edge becomes a falling edge in CKO<0>. The same thing happens to the falling edge in CKO<0>. If the rising edge and the falling edge experience the same delay, the signal is an equal amount of time high and low. So, in a conventional ring oscillator, CKO<7:4> and CKO<3:0> are four differential output clocks with a duty-cycle of 50%.

To change the duty-cycle of the output clock, for example, of signal CKO<0>, the delays of the rising edge and the falling edge have to be different. If an extra delay is only added to the falling edge and not to the rising edge before it reaches the input of D1, it is expected that the duration of the high pulse is smaller than the duration of the low pulse of the clock. Hence, the duty-cycle is reduced to a value smaller than 50%. To ensure that the operation of the loop remains symmetrical, an equal delay should be added to the rising edge of signal CKO<4>. If this extra delay is tunable, the duty-cycle of the clock can be controlled by changing the delay.

In the proposed design, this edge selective delay is implemented using the OR and AND gates added in front of delay cell D1. By applying a delayed version of a signal at the input of an OR gate, its falling edge is delayed. When a delayed clock is combined with the original version using the AND gate, its rising edge is delayed. Clearly, if a logic high or low signal is applied to the second input of the AND or the OR gate, respectively, both edges will experience the same delay and the duty-cycle of the ring will remain 50%.

The tunable feedback delay (TFD) block provides either a tie-high/low signal or adds an extra delay Δt to both falling and rising edge based on the MODE signal. To make sure each stage has the same delay, dummy OR/AND gates and dummy TFD cells are inserted to balance the loading. This way, four differential clocks with a duty-cycle of $(1 - \Delta t/T_{\mathrm{ck}})/2$ are generated from the ring in the preamble mode. The OR and AND gates use exactly the same transmission gate circuit; this ensures matched falling time and rising time at the output. When MODE toggles to high in the normal mode, the input transmission gates of TFD are disabled and the outputs, fbp and fbn, are fixed at the ground and supply, respectively. So, CKOD<3> changes to logic 0 and CKOD<7> changes logic 1 accordingly, making the OR and AND gates transparent in the first stage, the same as in the other stages. In such a way, four differential clocks with a duty-cycle of 50% are generated in the normal mode.

To maintain a matched rising edge and falling edge delay in the delay unit, it is implemented using two ×6 inverters and two local feed-forward paths (FFPs) consisting of cascaded ×2 and ×3 inverters. Input phases are injected from current-starved inverters with tunable strength. The delay introduced by TFD to create a non-50% duty-cycle reduces the self-resonance frequency of the ring oscillator in the preamble mode. The phase offset between the injection phase and the corresponding output phase is determined by the difference between the injection frequency and self-resonance frequency. To make sure the phase offset between CKI<0>

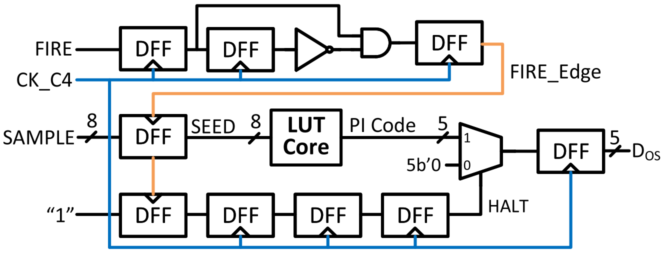


Fig. 14. Implementation of LUT logic.

and CKO<0> are the same in both modes, the frequency of the ring is tuned using a strength tunable FFP.

The DCS in the different modes must also be implemented in the FFP so that the phase accuracy is not disturbed. The FFP provides a tuning range of 3.6 and 5.1 GHz in the preamble and normal modes, respectively. VCTRL changes the bias of the current-starved inverters and is set by PM_DAC and NM_DAC in the preamble and normal mode, respectively. The DAC code is preset by monitoring the output of ILRO_PD. In this way, a fast switch from the preamble mode to the normal mode is achieved.

The jitter performance of the entire MPCG is evaluated in simulation using a 15-GHz input clock with 54-fs integrated rms jitter (measured from 10 kHz to 1 GHz) and a supply noise of 2 nV/$\sqrt{}$ Hz. The output clock jitter increases to 136 fs in the preamble mode and 119 fs in the normal mode. The DCS_ILRO contributes 62.72% and 51.94% of the total jitter in the preamble and normal modes, respectively.

D. Lookup Table

To enable efficient, flexible, and fast data processing, the 8-bit pattern detected in the preamble mode is converted to a phase interpolation offset code using an LUT. The LUT in the digital block operates at a quarter rate. When FIRE goes high after START is pulled high, a rising edge, FIRE_Edge, is generated from the trigger FIRE. This rising edge latches the 8-bit SAMPLE as the SEED for the LUT Core, as shown in Fig. 14. The 16 SEED patterns and their corresponding PI codes are stored in the LUT Core. Once the SEED is latched, the LUT Core outputs the corresponding PI Code, which is then latched by HALT for use in the subsequent normal mode. The PI Code D_{OS} is added to the PI controlling interface to shift the clock phase to the target position, which aligns with the incoming data.

E. Others

The data path includes an on-chip matching network and an AFE, which consists of a continuous-time linear equalizer (CTLE) stage followed by two variable gain amplifier (VGA) stages. The CTLE provides a 24.1-dB peaking tuning range at 24 GHz. The two VGA stages offer a gain tuning range of 11.5 dB, with a step of 1.64 dB. The AFE is designed to compensate for a test channel that exhibits a loss of 16.7 dB at 15 GHz and 24.5 dB at 30 GHz.

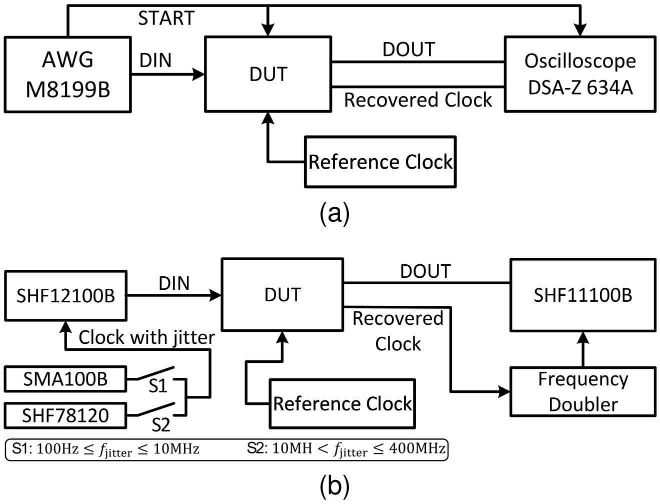


Fig. 15. Test setup. (a) BM locking. (b) Jitter tolerance.

V. EXPERIMENTAL RESULT

The test setup shown in Fig. 15(a) is used to measure the BM locking behavior. The burst bit stream and START signal are generated from the first and second data output channels of the arbitrary waveform generator (AWG), respectively. The half rate reference clock is generated from another frequency synchronized clock source. The input phase offset of the burst bit stream can be tuned by changing the output delay in the AWG with a step of 0.3 ps. The recovered clock is monitored by a real time oscilloscope. As shown in Fig. 15(b), the data generator SHF12100B with external 30G full rate clock from either SMA100B (when jitter frequency is 100 Hz∼10 MHz) or SHF78120 (when jitter frequency is 20 MHz∼400 MHz) is used to generate the data in the jitter tolerance measurement. The jitter is added to the clock through the frequency modulation function embedded in SMA100B/SHF78120. The output is checked by SHF11100B with the recovered clock from the CDR.

A. Phase Locking

Fig. 16 shows the locking time on a clock pattern at different input phase offsets without fast phase offset detection. It clearly shows that the locking time is proportional to the input phase offset since the phase increment is determined by the slew rate of CDR when a large phase offset is presented. The worst case happens at the edge when phase offset equals $+/-\pi$.

Fig. 17 shows the BM phase locking to a stream of consecutive packets, each separated by 32-bit gaps. Each packet contains either 32 736 bits of the "1010" clock pattern, corresponding to a half-rate clock, or a customized data pattern with 32 bits of the "1010" pattern preamble, 8 bits of zero, 8 bits of one, and 32 688 bits of PRBS-7 (limited by the memory of the AWG). A periodic synchronized signal from the AWG serves as the START signal, triggering fast PD on its rising edge at the beginning of each packet. The AWG output delay is adjusted by 0.3 ps per step to the most stressed case, where the input phase offset is 0.5 UI for both the "1010"

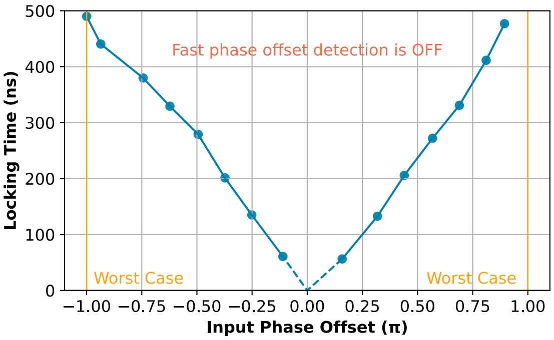
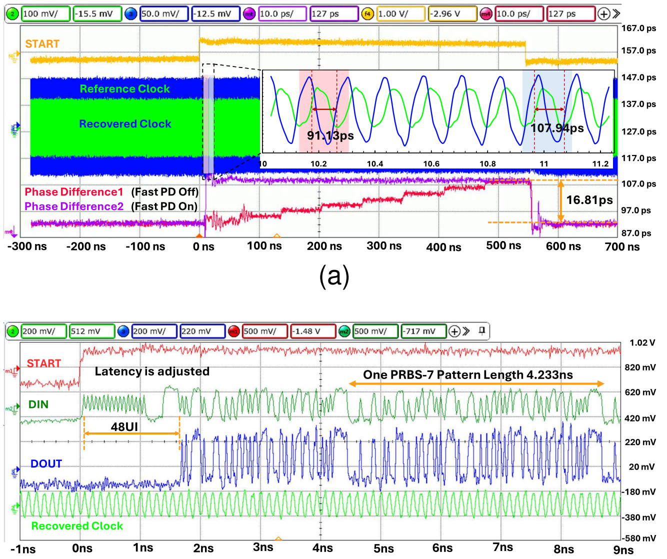


Fig. 16. Locking time without fast phase offset detection.



(a)

(b)

Fig. 17. BM locking behavior. (a) Phase locking to the clock pattern. (b) Phase locking to the data pattern.

and customized data pattern scenarios. For the "1010" pattern input, the phase difference between the recovered clock and a quarter-rate reference clock is measured in real-time, as shown in Fig. 17(a), where the Y-axis unit is ps for the measured phase difference, and the unit of the captured signal is ignored. Without fast PD, the CDR loop requires 467 ns to shift the phase by 16.81 ps to lock. It is interpreted that $t_{\mathrm{cl}} \approx 58$ ns for a phase offset of 1/16 UI. In contrast, with the fast PD, phase alignment occurs immediately after mode switching with the same DLF settings. From the zoomed-in waveform, it can be observed that the measured settling time including t_{det} is less than 0.8 ns. $t_{\mathrm{det}} = 4$ UI since only eight samples are needed. So, the t_{msw} is interpreted as 20 UI. In the case of the customized data pattern, the recovered data from the on-chip high-speed test driver output matches with input data after 48 UIs at a data rate of 30-Gb/s corresponding to a lock time of 1.6 ns. The latency of DOUT is adjusted to make a bit-to-bit comparison between DIN and DOUT convenient. The 48 UI preamble is the shortest length for zero missing bit data recovery due to the delay of some internal digital controls. Further optimization can reduce the preamble length.

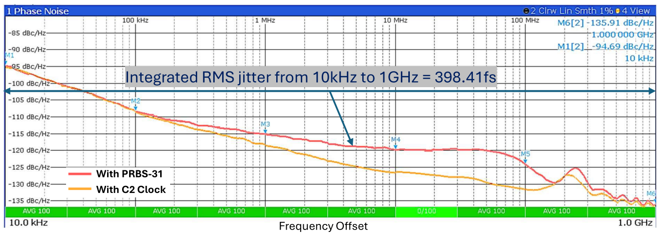


Fig. 18. Phase noise and integrated rms jitter of the recovered clock at 7.5 GHz.

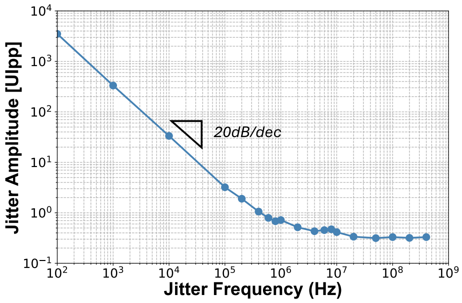


Fig. 19. Jitter tolerance with PRBS-31.

B. Phase Noise and Jitter Tolerance

Fig. 18 displays the quarter-rate recovered clock phase noise in the normal mode with the "1010" pattern and PRBS-31 inputs. The integrated rms jitter is 398.4 fs at 7.5 GHz from 10 kHz to 1 GHz. Jitter tolerance measurement reveals a corner frequency of 20 MHz and 0.3 UI tolerance up to 400 MHz as shown in Fig. 19.

VI. COMPARISON AND CONCLUSION

A. Summary and Comparison

Fig. 20 shows the die micrograph of the chip fabricated in a 28-nm CMOS process with an area of 0.148 mm^2. The CDR core takes 0.052 mm^2, including decoupling caps and sampler DCOC and EOM DACs. The power consumption of each part in different modes is summarized in the power breakdown plot in Fig. 21. The power consumption of this CDR in the normal mode is 75.53 mW from a 0.9-V supply. The FFP in the DCS-ILRO consumes an extra 3.68 mW to speed up the ring in the preamble mode. Table I summarizes performance metrics and comparisons. The proposed CDR locks in 48 UIs without jitter and 82 UIs with 0.2 UI peak-to-peak jitter, which shows an improvement of more than two times in locking time.

B. Conclusion

A traditional closed-loop BM-CDR provides jitter filtering and robust data-receiving compared to an open-loop BM-CDR. However, the locking time is limited by the input phase offset detection at the beginning of the burst due to the trade-off between the detection resolution and detecting time. The proposed 8/3x-oversampling method and circuit implementation breaks this trade-off and demonstrates that locking time can be improved by manipulating the duty-cycle in the sampling clock. The fast switching between different duty-cycles ensures the transition from open-loop detection

TABLE I
COMPARISON TABLE OF PRIOR PUBLICATIONS AND THIS WORK

Reference	ISSCC'23[29]	ISSCC'11[16]	ISSCC'16[15]	JSSC'20 [21]	ISSCC'15 [19]	ISSCC'18 [20]	**This Work**
Technology	28nm	65nm	28nm	65nm	32 nm SOI	14 nm	28nm
Signaling	PAM-4	NRZ	NRZ	NRZ	NRZ	NRZ	NRZ
Data Pattern	PRBS-7	PRBS-7	PRBS-9	PRBS-31	PRBS-7	PRBS-7	PRBS-31
BER	1E-12	1E-12	1E-9	1E-12	1E-12	1E-12	1E-12
Data Rate [Gb/s]	52	6	1-12	12	25	56	30
Supply Voltage [V]	N/A	1.2	0.9	1.1	N/A	0.9	0.9
Reference Clock	On-chip	External	On-chip	On-chip	External C2	External C2	External C2
CDR Type	Baud-Rate	Phase Interpolation	Injection Locking	Baud-rate	2x oversampling	2x oversampling	2x oversampling
Phase Offset Detection Method	-	No	No	Frequency offset	adaptive phase step searching	metastable condition shifting	duty-cycle switching
Phase Offset Detection Time [UI]	-	N/A	N/A	24~400	463	96~160	**4**
Phase Resolution [UI]	-	N/A	N/A	1/12~1/200	1/16	1/32	**1/8**
With Start Signal	-	No	No	Yes	Yes	Yes	Yes
Closed-Loop After Locking	-	No	No	Yes	Yes	Yes	Yes
Locking Time w/o jitter [UI]	-	1	1	120 (10ns)	775 (31ns)	384 (6.8ns)	**48** (1.6ns)
Locking Time w/i jitter [UI]	-	N/A	N/A	N/A	N/A	N/A	**82*** (2.73ns)
RMS Jitter [fs]	430	N/A	N/A	377	N/A	N/A	398
JTOL [MHz]	10	N/A	>100	30	10	N/A	20
Power Cycling	-	No	No	Yes	No	Yes	No
Power Efficiency (CDR Only) [pJ/b]	0.64	3.67	0.9	N/A	N/A	N/A	1.68
Power Efficiency (Receiver) [pJ/b]	0.83	-	2.8	3.8	4.4	2.2	2.52
Area [mm^2]	0.011	0.0175	N/A	0.45	0.06	0.06	0.148

* inject extra 0.2UI peak-to-peak jitter from AWG.
**[29] is not a burst-mode CDR.

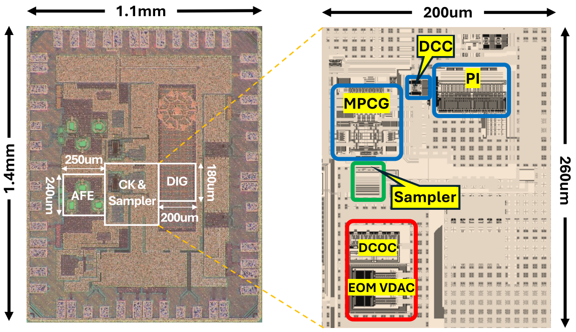


Fig. 20. Die micrograph.

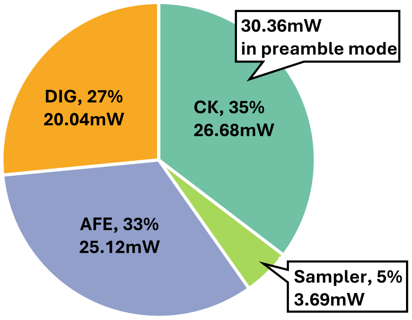


Fig. 21. Power breakdown in the normal mode.

and closed-loop phase tracking. The 4 UI detection time with 1/8 UI resolution enables fast locking BM links in the future for non-blocking optical packet switching networks in data centers and reconfigurable interconnection of multiple computing cores.

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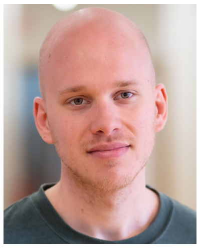

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