Design Considerations of High-speed Analog De-multiplexer

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***Abstract*—To overcome the bandwidth and sampling rate limitations of the CMOS ADCs, a high-speed analog de-multiplexer (ADEMUX) offers scalability for the future heterogeneous ADC and the wireline receivers. We discuss the design considerations of high-speed ADEMUX, including architecture comparison, and circuit design.**

***Index Terms*—de-multiplexer, sampler, SiGe BiCMOS**

I. Introduction

Next-generation optical transceivers are approaching to operate at a 200 GBd or higher symbol rate, posing a significant challenge for electronic and photonic integrated circuits. In the past few decades, the performance of data converters has been continuously increasing, in part because of the development of advanced CMOS technologies. However, with the node size of the transistors in CMOS-FinFET technologies close to their physical limit, this advance is becoming increasingly difficult to continue. Compared to CMOS technologies, silicon–germanium (SiGe) and indium phosphide (InP) offer core devices with higher current density, higher cut-off frequency, and breakdown voltage, enabling the analog circuit to achieve higher bandwidth. Recently, analog multiplexers [1] (AMUX) and demultiplexer [2] (ADEMUX) in SiGe or InP have demonstrated their abilities to significantly reduce the analog bandwidth and sampling rate requirements for data converters.

II. Voltage-Mode Sampler

A 1-to-N ADEMUX is usually implemented as an N-way interleaved sampler, which can be implemented either in voltage-mode sampling or current-mode sampling. Voltage-mode sampler is widely used in CMOS analog-to-digital converters (ADC) and exhibits great advantages in terms of power consumption and chip area. However, the dynamic performance of the heavy interleaved scheme is limited by the mismatches among the huge number of interleaved channels, i.e., the 256-way interleaved sample-and-hold layer, in a 200 GS/s ADC [3].

To improve the speed of a single subsampler, the switched emitter follower (SEF) based voltage-mode sampler has been widely investigated [4]. Fig. 1 shows the schematic of a SEF-based voltage mode sampler, and its tracking bandwidth can be improved by increasing the tail current of the SEF. However, it suffers from the input signal feedthrough in the hold mode, caused by a high-frequency low-impedance path created by the parasitic base-emitter capacitor, represented by C_p in Fig

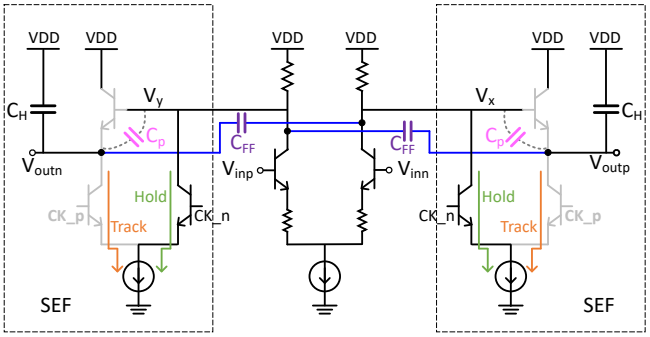

Fig. 1. Schematic of the SEF-based sampler.

.1. A feed-forward capacitor C_{FF} that transfers a part of the unwanted signal but with an opposite sign is usually employed to suppress the input signal feedthrough in the hold phase. Other techniques, like the switched pre-amplifier (SPA) based voltage mode sampler [4], aim to silence the signal at points V_x and V_y of Fig. 1 in the hold mode. These techniques are usually at the cost of tracking bandwidth and need more power.

III. Current-Mode Sampler

The time-interleaved current-mode sampler is an attractive solution for high-speed ADeMUX design. Recently published work [5] has shown its advantages regarding its capability of tracking high-frequency signals, low circuit complexity, low power consumption, less sensitive to the input signal feedthrough, and low cross-talk between sub-samplers. Fig. 2 shows a 4-way interleaved current-mode sampler from reference [5]. It operates by first converting the input signal from voltage mode into current mode before demultiplexing the equivalent signal current into four sub-samplers, controlled by 50% duty-cycle 64 GHz sinusoidal quadrature clocks at 256 GS/s. The signal current is then integrated onto a sampling capacitor and generates a sampled waveform.

The input signal tracking bandwidth of the current-mode sampler is determined by its integration time window length instead of the RC time constant in the voltage-mode sampler. Therefore, minimizing the on-resistance of the sampling switch, like increasing the tail current of the SEF in Fig. 1, is not necessary for the current-mode sampler. The power consumption of the time-interleaved current-mode sampler is inherently lower than the SEF-based voltage-mode sampler.

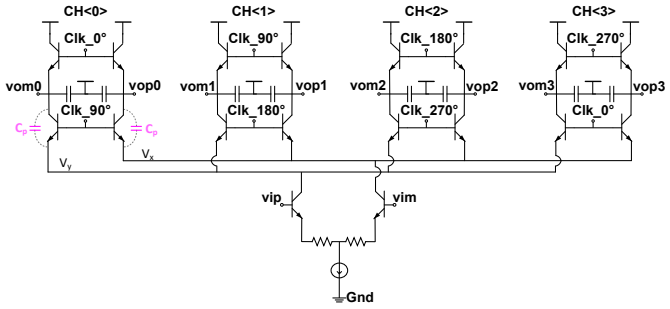

Fig. 2. Schematic of a 4-way interleaved from the reference [5].

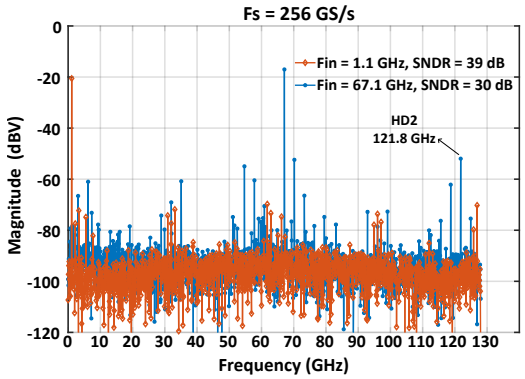

Fig. 3. FFT spectra with Fin = 1.1 and 67.1 GHz at 256 GS/s [5].

For example, the 4-way interleaved current-mode sampler in Fig. 2 requires only one tail current source, but a 4-way interleaved SEF-based voltage mode sampler in Fig. 1 needs at least 12 tail current sources.

On the other side, the current-mode sampler is less sensitive to the input signal feedthrough in the hold mode. For the current-mode sampler in Fig. 2, the input signal feedthrough is caused by the collector-emitter parasitic capacitance, represented by the C_p. Compared with parasitic base-emitter capacitance in Fig. 1, the C_p in Fig. 2 is much smaller. At the same time, the V_x and V_y are high-impedance points in Fig. 1, while they are low-impedance points in Fig. 2. Therefore, the input signal feedthrough is greatly reduced because of less signal variation at V_x and V_y and lower parasitic capacitance of C_p. Meanwhile, the time-interleaved current-mode sampler works on the principle that the sub-samplers compete for the input signal current. When the current mainly flows into one sub-sampler, the other three sub-samplers all have a high impedance as they lack bias current. In this case, the outputs of different sub-samplers are greatly isolated from each other by their high impedance, and the cross-talk is minimized.

Low slew rate sinusoidal clocks are typically unwanted in the CMOS voltage mode samplers, as the non-ideal on-off switching introduces input-dependent non-linearities in the track phase and aperture sampling error in the track-hold transition. Techniques like bootstrap switches are employed to alleviate the input-dependent nonlinearity issue. Fortunately, these issues are absent in the current-mode sampler shown in Fig. 2. As demonstrated in [6], the clocks with different slew rates apply different window functions to the input signal current demultiplexed to the sub-sampler without affecting the linearity of the signal captured.

A 4-way interleaved current-mode sampling front-end chip is designed in a 130-nm SiGe BiCMOS technology with a f_T/f_{MAX} of 350/450 GHz [5]. At 256 GSa/s, it achieved a 3-dB bandwidth exceeding 67 GHz, and a signal to noise and distortion ratio (SNDR) of 22 to 39 dB for input frequencies. Fig. 3 shows the measured FFT spectra with input frequencies at 1.1 and 67 GHz.

IV. Conclusion

Table I summarises and compares the CMOS, SEF-based, and current-mode samplers. The current-mode sampler has exhibited great performances, i.e., less sensitive to input signal feedthrough, no need for a bootstrap switch, and low sampler core power consumption.

TABLE I
A GENERAL COMPARISON OF DIFFERENT SAMPLER ARCHITECTURES.

	CMOS voltage-mode sampler	SEF-based voltage-mode sampler	Current-mode sampler
Sensitive to Input Feedthrough?	Yes	Yes	No
Need bootstrapped switch?	Yes	No	No
SNR due to Clock Jitter [5]	$0<f_{in}<f_s$, high $f_s<f_{in}<2f_s$, low	$0<f_{in}<f_s$, high $f_s<f_{in}<2f_s$, low	$0<f_{in}<f_s$, low $f_s<f_{in}<2f_s$, high
Sampler Core bandwidth	depends on RC	depends on RC	depends on integration time
Sampler core power consumption	low	high	low

V. Acknowledgments

The work was partly supported by Ghent University GOA and EU POETICS under Grant 871769.

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