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Chemical mechanical polishing for indium bond pad damascene processing

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We investigated chemical mechanical polishing (CMP) of indium, with the goal of obtaining indium bond pads for later cryo-3D integration of quantum computing-related chips, through bonding between these bond pads and indium bumps. Higher removal rates were obtained with soft CMP pads than with hard pads. The latter led to deep scratching, while this effect was much more limited for soft pad CMP. On patterned wafers, indium is cleared well in structured areas using soft pad CMP, leading to relatively high-quality indium surfaces inside bond pads, although corrosion might be of some concern. Pattern density uniformity was an important factor for within-die deviation in indium clearing time. Dishing was much more limited than in earlier work on indium polishing, while surface roughness was also found to be relatively limited. The obtained indium damascene bond pads may be suitable for 3D die-to-die and wafer-to-wafer bonding through indium pad-to-bump bonding.
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Supplementary material for this article is available online

1. Introduction

Indium (In) bumps have been considered as interconnects between chips in cryo-3D integration schemes for image sensors and quantum computing, as In presents several advantages: pure In sources are available,[1] it is superconducting below about 3.4 K,[2] stable at cryogenic temperatures, and bonding with In bumps through thermocompression is a proven technology.[3]

Indium can be deposited by thermal evaporation[1] or by electrochemical plating.[4] In the study of Shafahian et al. 2023,[4] plating of In bumps and trenches, etched in Si substrate, through a damascene-plating process, was demonstrated. For the In bond pad, the goal is to allow bonding with a top wafer through In bump-to-pad bonding at a later stage.

After plating, indium overburden and TiW barrier need to be removed from the wafer surface outside the In bond pads to avoid shorts. A pioneering 2008 study[5] used mechanical powder polishing of In pads for megapixel space imaging arrays to remove In overburden [in this study deposited through physical vapor deposition (PVD)] and obtained In bond pads with around 7.5 μm pitch, but dishing of the In pads was considerable (around 550 nm maximum).[5]

Chemical mechanical polishing (CMP) has hitherto been developed to allow metallization through damascene-like processes, consisting of etching of features in a dielectric layer, which next are uniformly filled with metal through PVD and plating, and where CMP is subsequently used to remove the overburden consisting of the plated metal plus possible barrier layers.[6,7] CMP has the advantage that through the combination of chemical and mechanical interaction across the full wafer, a good degree of within-wafer and within-die uniformity is achievable, in combination with relatively clean surfaces, in a relatively short processing time. For example, the Cu CMP plus TaNTa barrier back-end of line (BEOL) process technology is already well-developed, and also a host of alternative metals have been the topic of CMP experiments.[6,7]

However, to our knowledge, there have been no published studies on CMP of indium before. The present study focuses on development of such a CMP process for plated indium bond pads, to clear In and barrier above the Si field, leaving a good quality In pad surface, adequate for bonding with In bumps.

Indium is a relatively soft metal compared to most other metals applied in metallization processes[8] and therefore may present unique challenges for the set-up of a CMP process, which is known to be dependent on both hardness of the material and the CMP pad (either “soft” or “hard”), and on the properties of the abrasives in the CMP slurry.[7,9]

In Table I, different measures for a material’s hardness are compared between indium and some other metals for which CMP processes have been developed. We also give a few hardness values for soft and hard CMP pads. The Mohs’ hardness value[8] is lowest for In. The other types of hardness are based on indentation experiments with different indenters and measurement protocols, on either macro-scale samples (Brinell and Vickers hardness) or nano-indentation observations (Berkovich indentation) and are therefore not directly interchangeable.[10] Berkovich indentation values for indium are not available. However, one can still deduce from the Brinell hardness data that presumably the hardness values of Cu and Ta are between one and two orders of magnitude higher than these for indium.

The chemical mechanism at work in indium CMP chemistry is currently not yet fully established, but insights could be gained from the indium Pourbaix diagram for indium’s electrochemical reactions in contact with water.[15] In this diagram, it is found that within a pH range of about 4.5 to 11, the indium surface oxidizes into solid In_2O_3, which forms a passivation layer. Therefore, this part of the Pourbaix diagram is a “passivation” region, where the In metal underneath is protected against further corrosion and oxidation.[15] This formation of In_2O_3 occurs through the prior formation of intermediate In^{3+} ions at the surface, which can be driven by electrochemical reactions in the

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Table I. Overview of some available values for different hardness types (Mohs,[8] Brinell, Vickers, and Berkovich nanoindentation hardness) for indium and some other relevant metals for which CMP processes have already been developed. Also given are some indicative values for Berkovich indentation hardness of some commonly used "soft" and "hard" CMP pads. Values are mostly stated to be valid around room temperature.

Material	Mohs' hardness[8]	Brinell hardness[10,11] (MPa)	Vickers hardness[10] (MPa)	Berkovich indentation hardness[10,12] (MPa)
In	1.2[8]	8.83 (annealed),[8] 9.8[11]	—	—
Sn	1.5[8]	51 (annealed),[8] 292–441 (cast)[11]		—
Cu	3[8]	343–402 (at 293 K, annealed Cu at 872 K),[8] 520,[11]	343[8]	$1.64 \times 10^3 \pm 0.055$[12]
Ta	6.5[8]	441–1230 (annealed)[8]	873[8]	—
W	7.5[8]	2570,[8] 1960–2450 (annealed)[11]	3430[8]	—
Hard polyurethane "type 3" pad "IC1000"	—			41 ± 13.2[13] 56.3[14]
Soft poromeric "type 2" pad "H800"	—			0.90 ± 0.01[12]

aqueous environment.[15] In alkaline environments (from above about pH = 11), the solid indium oxide In_2O_3 can be transformed into soluble InO_2^-.[15] This means that above pH 11, the passivation layer can start becoming dissolved, exposing the underlying metallic In, which can then undergo a more continuous In corrosion process.[15,16]

Also, based on more established models for chemical interactions during CMP of other metals such as Cu,[17,18] Mo[18] or Al,[19] as examples, one could attempt to devise a tentative mechanism for some main reactions of the chemical part of the In CMP process. In the Cu-CMP model chemical mechanism of Paul et al. (2005),[17] the effect of the oxidizer H_2O_2 is added, which can enhance the electrochemical reactivity of Cu. In this model, Cu^+ ions cannot only be transformed into Cu_2O, but Cu_2O can also be further oxidized into CuO. Due to the mechanical component of CMP, which through abrasion continuously removes part of the formed passivation layers, the metallic Cu surface remains partially exposed, which allows Cu^+ ions to continuously dissolve into the aqueous slurry environment. There, organic complexifying agents can form complexes with the Cu^+ ions, further enhancing the chemical removal of the metal species. This process can also soften the metal surface which enhances the mechanical CMP component.[17]

A similar scheme might apply for a possible In CMP process, where, following again ideas present in the studies of Pourbaix (1974) and Paul et al. (2005),[15,17] under the influence of the mechanical action of pad and abrasives, the In_2O_3 passivation layer is continuously being removed, allowing part of the metallic In at the wafer surface to undergo enhanced dissolution (also promoted by the presence of H_2O_2), transforming more In into In^{3+} ions. These In^{3+} ions could then undergo competing reactions, either by still undergoing reaction towards In_2O_3, versus dissolution (enhanced by further complexification reactions), and a third possible route would be some form of mechanical removal through interaction with the abrasive or pad. Also, the dissolution of In_2O_3 is likely important.[15]

Several existing CMP damascene processes, such as for Cu, consist of multiple step processes where first a bulk removal step with a high rate (often on a hard pad) is used to remove the main fraction of the plated metal, sometimes followed by a Cu clear step, finally followed by a shorter timed barrier CMP step, sometimes using a soft pad, to allow for good final surface quality and minimal dielectric loss.[20] Moreover, endpoint systems are sometimes used to indicate the needed moment for transition between these steps.[20,21] Therefore we initially also investigated the possibility of a two-step In CMP process. In our current CMP tool set-up, the main metal bulk and clear CMP steps need to take place on hard pad-equipped platens, therefore we also include tests using a hard CMP pad on indium.

This article presents the exploratory development of a CMP process for 300 mm wafers with patterned indium structures. We first investigate the feasibility of such a novel CMP process with either hard and soft pads on blanket wafers and evaluate the obtained results with respect to surface quality and dishing of indium pad structures on patterned wafers. As tests on blanket wafers with hard pad CMP showed problems that were hard to solve, for patterned wafers we continued only with a one-step soft-pad CMP process to clear the full wafer, and the main results are obtained for this In CMP method.

This work contains much extended research and discussion with respect to the earlier submitted "Extended abstract" article for the SSDM2023 Conference.[22] With respect to this latter abstract article, the results and discussion for the development of a damascene CMP-process for patterned indium plated wafers have been largely extended. We show results for some further overpolish tests, and discuss new scanning electron microscopy (SEM), atomic force microscopy (AFM) and scanning electron microscopy-electron diffractive X-ray spectroscopy (SEM-EDX) results, which allow a better and more quantitative characterization of the post-indium CMP surface quality.

2. Methods: tools and materials, characterization

Indium CMP was performed on both blanket and patterned indium plated wafers, using an Applied Materials "Reflexion" CMP tool, which contains three platens, two of which are equipped with a "hard" CMP pad and one with a "soft" CMP pad. In its standard set-up, the tool is regularly used for more "standard" Cu CMP (with the hard pad, end point equipped platens) plus Cu barrier (such as TaNTa) CMP processing, using a soft pad.[20]

A large variety of different CMP polishing pads exists, for which a qualitative division into four different types, based on their composition, porosity type and hardness, was given by James (2004)[9] and updated by Lawing (2020).[23] In this qualification, the hard polyurethane CMP pad type "Visionpad 5000" (supplier: Dupont) used in our study, belongs to the class "Type 3" of hard filled polymer sheet pads with uniform porosity, which among other uses, are applied for metal

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damascene CMP processes such as copper CMP.[9,24] Such hard pads allow for higher removal rates and good planarization if used with suitable consumables and slurries.[9]

The porosity distribution of the "Visionpad 5000" was characterized in Lawing and Juras (2007) and shown to result in surface height variations of the order of a few μm.[25] This pad is customarily equipped with a conditioner. For this pad, the initial pad break-in and following suitable conditioning process with a diamond crystal conditioner, conditions the pad surface by cutting away worn pad material.[26] This is crucial in maintaining the desired porosity over the intended lifetime of the hard pad, by countering the effect of "glazing," which is the blunting of pad asperities by wear during CMP, which otherwise leads to lower and unsuitable porosity, which in turn can lead to undesired removal rates and profiles.[25,26]

The used soft CMP pad "Optivision 4548" (supplier: Dupont) belongs to the "Type 2" class of "soft" poromeric pads, which consist of a porous film with vertically oriented pores on top of a supporting substrate.[9,24] It contains softer polyurethane in combination with some other organic layers. Such CMP pads are suitable for barrier CMP and "buff" touch-up CMP steps, as they allow for lower surface scratch defectivity.[9] In our set-up, currently no conditioning is applied to the soft pad.

The hardness of CMP pads can also be quantitatively characterized using physical indentation testing protocols, such as the indentation of the material with a Berkovich diamond indenter, which consists of continuously measuring the deformation of the material under increasing and decreasing loading of the indenter.[12,13] Unfortunately, direct quantitative hardness assessments for our used hard or soft pads were not available to us. However, for a frequently used pad of hard "type 3," "IC1000",[24] Berkovich indentation hardness determinations found values of 41 ± 13 MPa[13] and 56.3 MPa[14] (see also Table I). On the other hand, for a soft pad of "Type 2," "H800," a value of 0.90 ± 0.01 MPa was obtained.[12] These values could at least inform on the expected order of magnitude of the hardness of the soft and hard pads used in this present study.

For the hard pad CMP blanket tests, five different slurries were tested (Table II), as is also indicated in Fig. 6, where they are classified by pH. These slurries have all been successfully used in some other hard pad CMP processes. The goal was to check whether some of these slurries might lead to acceptable material removal rates and to check the impact of the hard pad CMP with these slurries on the CMP-ed indium surface. The type of abrasive is indicated, along with the given weight percentage concentration range. The size distribution of the abrasives was unfortunately not yet studied or available from other sources. As an oxidizer, H_2O_2 was added, except for the acidic dielectric slurry. For the soft pad CMP, we have for now only tested the "non-selective alkaline barrier slurry," as this slurry type is customarily used on the soft pad for various barrier CMP processes. It should be noted that the full composition of these commercial types of slurries is not known and disclosed. But it is expected that they contain various other organic/inorganic compounds which can aid specific aspects of CMP processes, such as other oxidizers, metal ion complexing compounds (chelating agents), acidity regulators, corrosion inhibitors, surfactants, and biocides, among others.[18,24]

In Table III, the CMP rotation speeds for platen and head, slurry supply flow towards the platen and applied wafer head pressure in the center of the wafer are given. For the soft pad recipe, three different pressures regimes were tested for blanket wafers, while for the patterned wafers we only used 0.8 and 1.5 psi (1 psi = 6.894757 kPa). It should be noted that listed pressures are applied in the region within wafer radius 130 mm, while in the region corresponding to the outer 20 mm of the wafer radius, the applied pressure needed to increase and therefore deviates from the indicated central pressure. For the soft pad, these settings are also successfully applied for some barrier CMP processes. For the hard pad CMP recipe, the given settings were used for Cu CMP processes, except for the pressure, which we decreased in view of foreseen issues with scratching.

After the wafer polishing is finished, wafers are given a short diluted benzotriazole (BTA, corrosion inhibitor) rinse, followed by a mega-sonic clean and brush clean, followed by drying.

Blanket indium wafers were plated and characterized, and then used for CMP removal rate and surface quality characterization, while In bond pad CMP was tested on patterned wafers (see Fig. 1). These wafers were plated in an Applied Materials "NOKOTA" tool.[4] Blanket wafers plated for the tests contained 175 nm TiW liner and 25 nm Cu seed underneath, deposited through PVD, directly on Si. It should be noted that the 25 nm Cu seed layer, which aids the initial indium plating,[4] was presumably taken up into the In layer through diffusion, forming partial $CuIn_2$ intermetallic compound[23] regions at the bottom of the indium layer.[4]

The patterned wafers contain dies with squares consisting of large numbers of circular test and dummy trench bond pad structures, which lie close to each other, with pitches 5.0, 7.0, 10.0 and 20.0 μm (see Fig. 11). The trenches were directly etched into Si and trench depth was approximately 800 nm [see Fig. 1(b)]. For the patterned wafers, a next generation of In plating chemistry was applied. They were plated on 10 nm TiW liner and 25 nm Cu seed, which again presumably

Table II. Overview of used slurries along with some disclosed properties such as pH, abrasive type, abrasive mass concentration percentage range and added H_2O_2.

Slurry	pH	Abrasive type	Abrasive mass % range	Added H_2O_2 (mass %)	Tested with hard pad	Tested with soft pad
Acidic "dielectric" slurry	2.25	Amorphous silica	10%–20%	0.0%	yes	no
Cu slurry 1	4.2	Amorphous silica	<3%	1.5%	yes	no
Cu slurry 2	7	Silica	1%–5%	1.0%	yes	no
Selective barrier slurry	8.7	Aluminium oxide	<3%	2.7%	yes	no
Non-selective alkaline barrier slurry	11	Colloidal silica	4%–14%	0.4%	yes	yes

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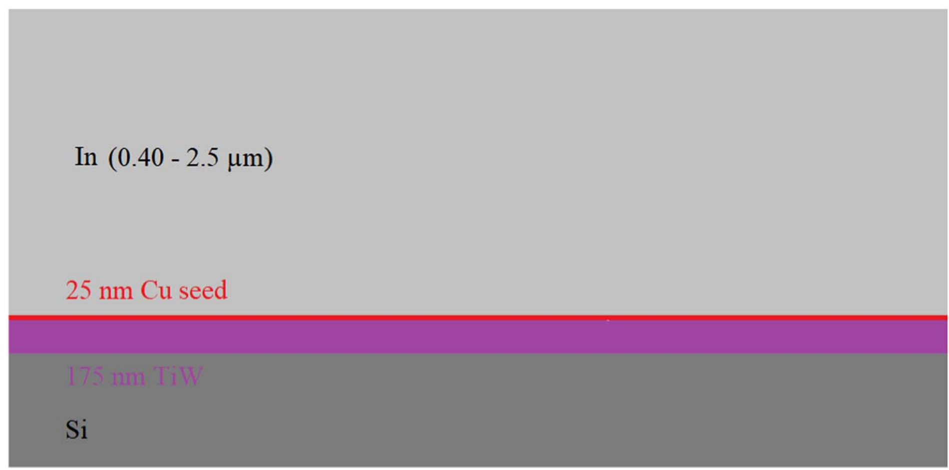
Table III. Experimental CMP settings applied during the soft and hard pad indium CMP processing.

CMP type	Platen speed (RPM)	Head speed (RPM)	Slurry flow (ml/min)	p in central wafer area (radius < 130 mm) (psi)	p at wafer edge area (psi)
"Soft pad" CMP	180	182	200	0.8	2.8
	180	182	200	1.5	3
	180	182	200	2.5	6.7
"Hard pad" CMP	59	61	300	1.5	3

(a)



(b)

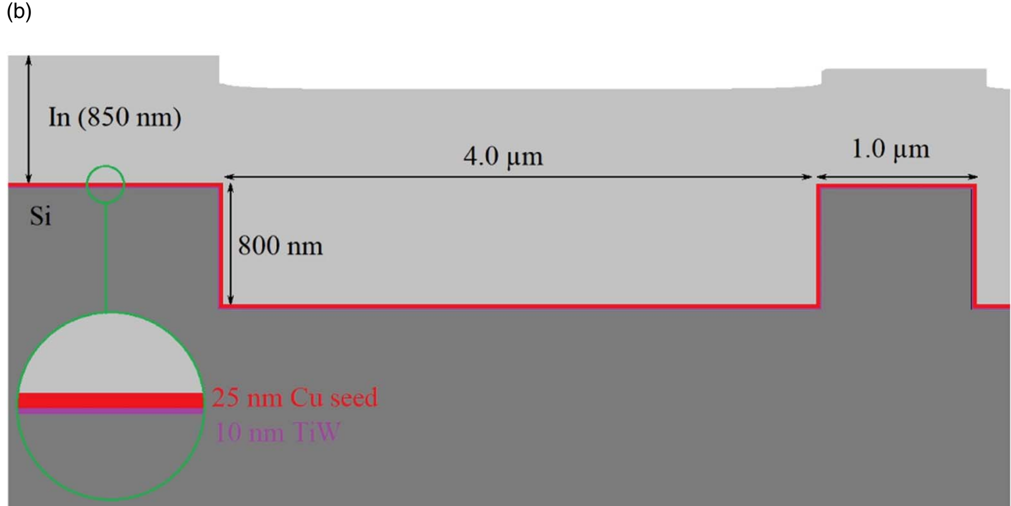


Fig. 1. (a) Sketch of the stack for blanket indium wafers tested in this work. The barrier was 175 nm TiW for these wafers, while 25 nm of Cu is added to aid plating. Plated In thickness for blanket wafers was varied between 400 nm to 2.5 μm. (b) Stack sketch for typical patterned wafers (see also Table IV), with In bond pads of around 800 nm etched in Si. The TiW barrier in this case is only 10 nm thick, while plated In layer thickness above the Si field was either around 300 nm, 850 nm or 1200 nm. Some local topography depression of the In layer is observed above In pads. Not shown is natural surface roughness.

diffused quickly into In. The lower thickness of TiW of 10 nm in combination with the Cu seed was found to be sufficient to allow for good quality and uniformity of In plating,[4] and also makes full clearing up to the Si level in the field easier during the CMP process.

For patterned wafers, we used soft pad CMP with only the non-selective alkaline barrier slurry. CMP pressure was either 0.8 or 1.5 psi (Table IV). Three different initial indium plating thicknesses were aimed for and estimated with the aid of sheet resistance (R_S) (see also Fig. 8).

Sheet resistance (R_S) was measured on a KLA Tencor RS metrology tool. We estimate In film thickness approximately based on R_S and a published value of bulk resistivity of In, $\rho_{In} = 8.37\ \mu\Omega$.cm.[27] This calculation will be less valid for very thin films, as resistivity for thinner metal films is known to increase above the bulk resistivity values. For example, for Cu there is a determination of ρ_{Cu} for thin films with thickness below 100 nm which shows that below that thickness, ρ_{Cu} (near RT) starts increasing from near to its bulk value 1.68 $\mu\Omega$.cm,[27] to about 10 $\mu\Omega$.cm around 10 nm Cu thickness,

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Table IV. Conditions for indium CMP experiments on 6 patterned indium plated wafers.

Wafer number	D07	D08	D09	D10	D11	D12
Initial average wafer thickness estimate in wafer center (nm)	322	314	861	867	1,190	1,189
Applied pressure at wafer centre (psi)	0.8	1.5	0.8	1.5	0.8	1.5
Time to clear indium near In bond pads (mins)	6	4	10	11.5	20	15
Extra CMP time applied to clear In in empty field (mins)	0	0	6	0	6	0

and further increases orders of magnitude for even thinner layers. Also, the uncertain contribution of the thin TiW barrier and Cu seed is neglected in this approximation. Therefore, thickness estimates and derived removal rates can be expected to become less accurate when the indium layer is already mostly removed.

In future, a more systematic study determining the ρ_{In} values for different In layer thicknesses could be considered, where the layer thickness of indium could be determined independently through for example TEM or cryo-FIB-SEM.[4] This could form the basis of a thickness-R_S calibration, such as is available for some other metals. Additionally, we could consider whether the R_S-based removal rate profiles cannot be rendered more accurate by constraining them with the help of mass determinations of the CMP-ed In plated wafers before and after In CMP, as determinations of mass might allow estimates of average wafer layer thickness reduction of order nm.

The In surface was inspected through optical microscopy and SEM. To check the filling of trenches and layer structure, SEM on cleaved wafer samples and focused ion beam (FIB)-SEM were used.[4] Cryo-FIB SEM is also considered suitable, as it limits melting of In.[4] Roughness and dishing were quantified with AFM.

Element analysis of the final CMP-polished surface in both the Si field area as on the In bond pad's surfaces was performed using SEM-EDX, in order to check the clearing of indium, Cu seed and TiW liner from the Si field, and check for possible contamination of the Si field or indium pad areas.

3. Results and discussion

3.1. Results for CMP on blanket In wafers

Post-plating, but pre-CMP, the indium-plated wafers present a rough surface with micron-sized lumpy features in both horizontal and vertical dimensions (see Fig. 2).

Hard pad In CMP was invariably found to lead to scratches with a depth of micron dimensions (Fig. 3), irrespective of the type of slurry applied. This strong susceptibility to scratching is most likely related to the low hardness of indium (Table I), whereas the hard pad is usually used on significantly harder materials, and therefore more adapted to these.

For soft pad CMP with an alkaline barrier slurry, scratching is much less prevalent. After 4 min of CMP, the In surface is planarized, and grain structure is visible (Fig. 4).

Figure 5 shows the sheet resistance (R_S) and estimated In thickness wafer diameter profiles after successive In CMP iterations, in this case for soft pad CMP on a blanket In wafer. Removal rate profiles for the same CMP experiments show that for the "$p = 0.8$ psi pressure in central area" In CMP condition, removal rates tend to have a profile where the removal rate is somewhat higher near the wafer edge.

Additionally, we have also added some typical CMP removal rate profiles, obtained with either the 0.8 psi, 1.5 psi or 2.5 psi pressure in the central wafer region, to a section of the Supplementary data. For the other two pressure settings, the removal rate at the wafer edge is relatively lower, and there is also a maximum removal rate in the center.

There can be quite some variability in obtained removal rate profiles, both for the average removal rate as for the removal rate profile along the wafer diameter. Such variations tend to occur even when processing with the same recipe, depending on factors such as the amount of In wafers already processed with the soft pad previously, where we see a lowering trend initially which leads to a stabilizing lower rate afterwards, as more and more In CMP takes place (see also evidence for this effect in the case of patterned wafers in Fig. 12). There is also a not-fully understood day-to-day removal rate tool variation (also observed for other CMP processes).

Therefore, the removal rate values for hard and soft pad CMP in Figs. 6 and 7 are only indicative of typical average removal rate values. The removal rates can be more completely described as time-dependent distributions of spatial removal rate profiles.

For hard pad CMP (Fig. 6), removal rates were highest for acidic or strongly alkaline slurries, but all rates are on the low side, not exceeding 30 nm min^{-1}. More neutral slurries gave the lowest removal rate. The indium Pourbaix diagram[15] indeed has a "passivation" region for pH between 4.5 and 11, which might lead to some lowering of CMP rates. However, the higher abrasive content of both the acidic slurry and alkaline non-selective barrier slurries may also play a role.

For the soft pad and alkaline slurry (Fig. 7), removal rates were higher (order 80 nm min^{-1}), while rates increased with pressure (from 60 nm min^{-1} up to 130 nm min^{-1}). For the higher pressure, a slight increase in scratching was observed, although still much better than with the hard pad.

3.2. Results for CMP on patterned In wafers

For the tested patterned In-plated wafers (see Table IV), indium layer thickness had been varied and was subsequently estimated based on sheet resistance measurements (Fig. 8). It was found to be on average approximately 300 nm, 850 nm or 1200 nm in the "field" area [Fig. 8(b)] in the central wafer area.

It should be noted that in Fig. 8, for the wafers with the lowest In thicknesses (around roughly 300 nm), the spread in obtained R_S is considerably higher than for the two other thicknesses. We have not been able to determine the cause of this larger spread with certainty, but hypothesize that for the lowest thicknesses, the presence of the patterned trenches may play a stronger role. Also possible is that during the measurement, the R_S-probes might more easily locally deform the relatively soft In layer for the lowest In thicknesses than for the higher thicknesses. This might lead to deviations from the R_S of originally undeformed plated In layers.

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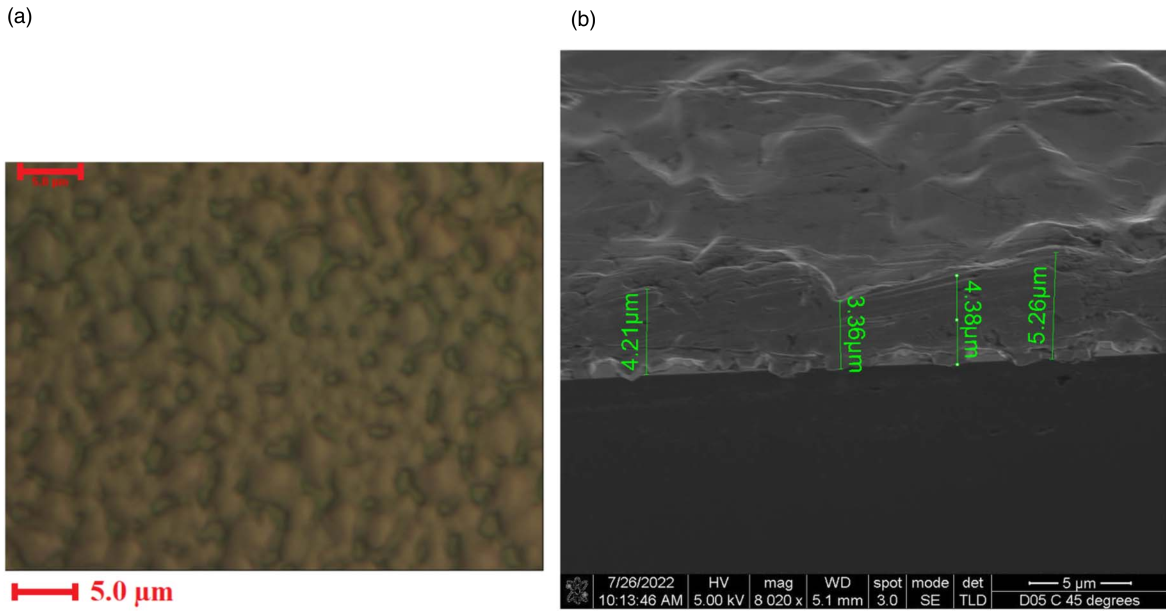

Fig. 2. Pre-CMP plated indium surface of blanket wafers. (a) Optical microscope images. (b) SEM image.

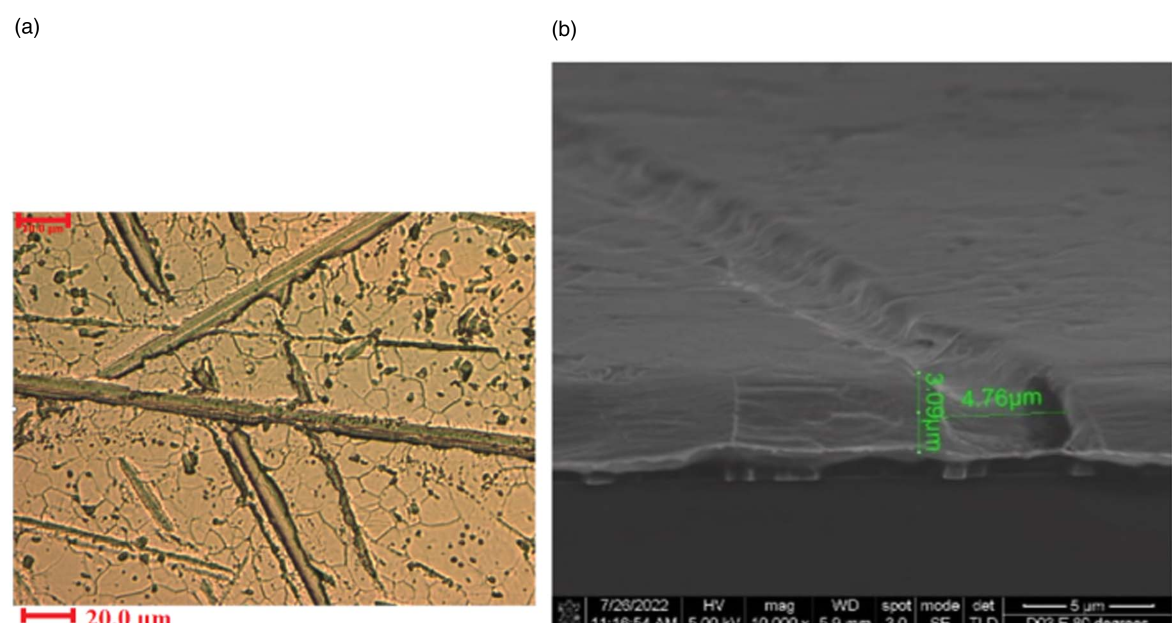

Fig. 3. Hard pad indium CMP (after 4 min, acidic slurry): (a) multiple scratches visible in microscope pictures in partially cleared plated In. (b) SEM image of a typical hard pad scratch.

SEM images of the patterned plated In wafers show that besides the inherent non-uniformity of the In plated surface, there is also non-uniformity between areas directly above or next to the indium trenches (Fig. 9). This phenomenon is stronger for the thinner initial plating thickness samples. This is presumably due to a non-uniformity during the plating process of transport and deposition of indium, where locally indium is still being deposited at a lower level inside the pad, while on the field already at the same time, indium is being deposited at the higher level of the Si field plus barrier. Ideally, an indium overburden of perhaps factor 2 times the trench depth (here 800 nm) can be chosen in order to lower the difference in final height of the In surface level above filled trenches, compared with the In surface above the Si field. Higher In overburden would however make the CMP process longer.

In Fig. 10, we show a SEM picture after cleaving of a patterned wafer. This shows the successful filling of the trenches and also the initial surface roughness after plating. In the cross section the non-uniformity above the trench is less visible due to some material alteration during cleaving. It should also be noted that this is an image of a patterned In plated wafer of a different patterning type than the ones processed during the In CMP, with more narrow-width (about 900 nm) trenches, and TiW was 175 nm thick here.

The six patterned plated wafers (Table IV) were subjected to a consecutive series of CMP polishes. Progress of indium removal was tracked through intermediate microscope inspection and sheet resistance measurement. This was continued until we observed that the Si field directly around the circular In pads became cleared (Table IV shows the sum of the CMP times of these iterations). As expected, the

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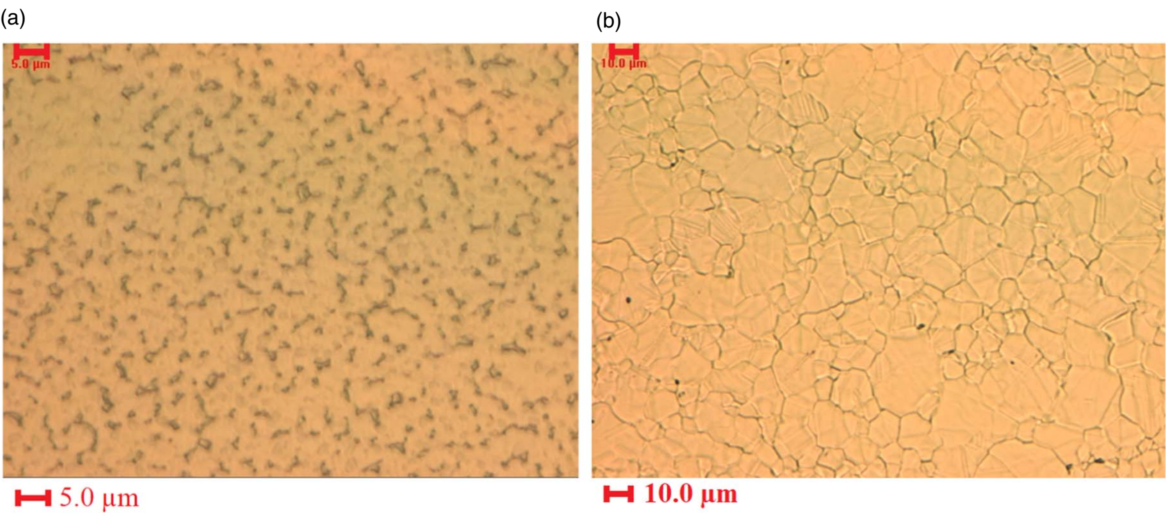

Fig. 4. Post soft pad CMP, alkaline slurry. (a) After 1 min, surface lumpiness is reduced. (b) After 4 min, planarization is strongly increased, and grains become visible.

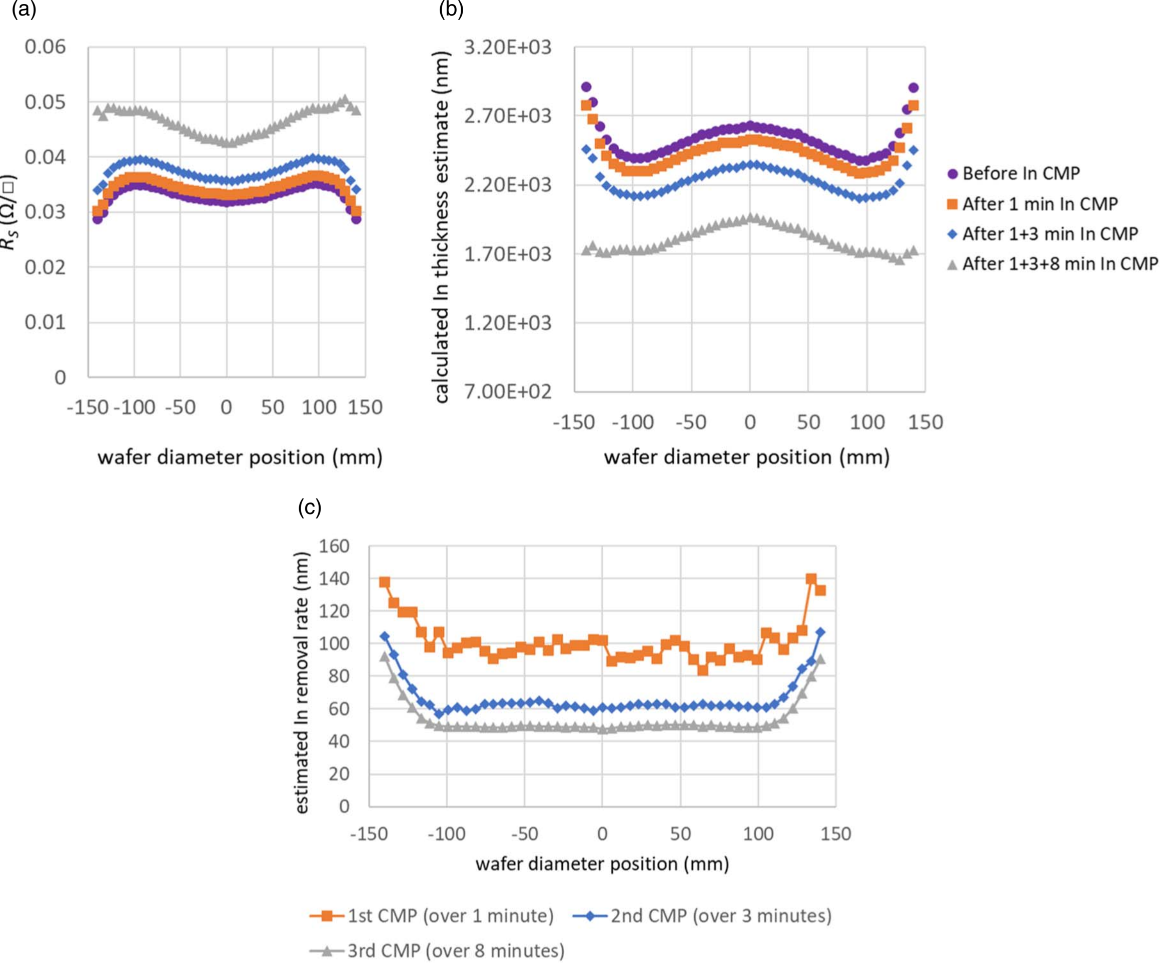

Fig. 5. (a) Sheet resistance (R_S) and (b) R_S-derived indium layer thicknesses (based on bulk indium resistivity estimate approximation) over several CMP iterations (1 min In CMP, followed by further 3 min and 8 min CMP processing) of soft pad CMP on blanket plated In wafers, with an alkaline barrier CMP slurry. (c) Corresponding removal rate profiles over iterative CMP processing for the 3 processing iterations leading to the measured wafer properties after CMP in (a) and (b).

higher pressure In CMP cases required less time to clear the indium.

However, at that point, an indium layer remained in empty field areas [Fig. 11(a)], a finding which was observed for all six tested conditions. For two test wafers, D09 and D11 (corresponding to the lower CMP pressure setting and the mid and higher initial In thickness), additionally it was found that about half of the dies (corresponding to the center of the wafer) still contained In structures that were not yet cleared of indium in the surrounding field area, while outer dies had fully cleared Si field around In structures. Subsequently, extra overpolishes were applied, of in total 6 min on these two

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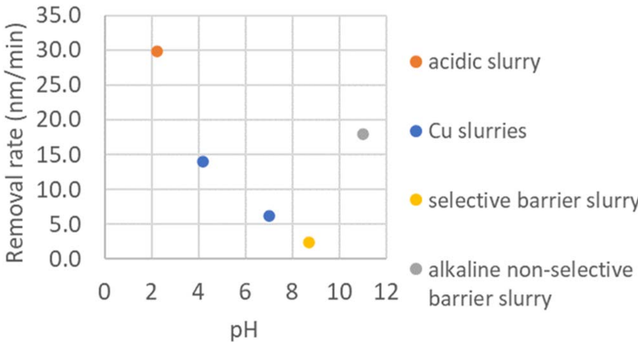

Fig. 6. Several average indium CMP removal rates for different slurries, using hard pad CMP on blanket indium wafers, in function of pH.

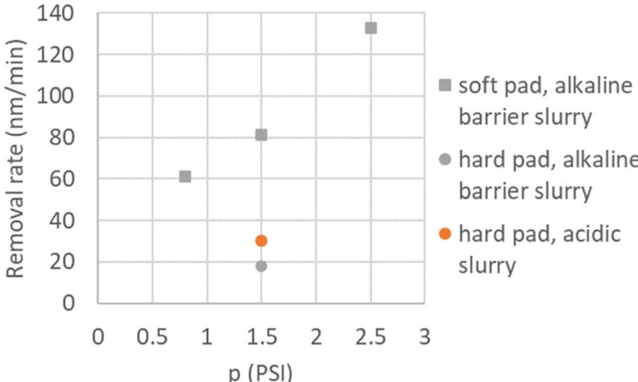

Fig. 7. Indium CMP average removal rates for soft pad CMP at different CMP pressures, compared with hard pad In CMP removal rates, both determined for blanket indium wafers. At equal head pressure, soft pad CMP rates are significantly higher than hard pad rates.

wafers (see Table IV), after which it was observed that for both of these wafers the Si field areas became fully cleared of indium everywhere, directly around In pads areas, as well as in empty field areas.

During the In CMP processing session on patterned In wafers shown in Table IV, it was also observed that indium CMP removal rates decreased as the indium processing session progressed (see Fig. 12). First, the 6 test wafers were CMP-ed for 1 min each, so by the time the 1st In CMP iteration on D12 started, the soft CMP pad had undergone 5 min of total previous In CMP processing on other wafers. The 2nd In CMP iteration on wafer D12 (for 3 min) was then preceded by in total 18 min of cumulative In CMP with the soft pad. The last iteration of In CMP on D12 was preceded by in total 42 min of cumulative In CMP. It can be observed that the removal rates over these progressive CMP iterations decreased significantly, from around on average 100 to 110 nm min^{-1} initially, to about 80 nm min^{-1} in the intermediate regime, stabilizing to about 70 nm min^{-1}. Removal rates could not be accurately determined anymore over the last iteration of 3 min of In CMP on wafer D12, as the wafer became already partially cleared of indium during the course of that iteration.

Observation of the soft CMP pad after the In CMP showed evidence of significant pad wear and also build-up of presumably In residues, which could explain the progressive decrease in In CMP removal rate. It was found that afterwards the used indium pad was no longer able to deliver expected removal rates for other processes such as Ta barrier CMP, necessitating pad replacement.

In optical microscopy (Fig. 11) and SEM inspection images (Figs. 13 and 14), the quality of the cleared In pads and Si field generally seems acceptable. There seems to be very little defectivity impact of scratching. Cleared bond pads overall seem to have a relatively limited dishing and surface roughness, which we will further characterize.

In Fig. 13, a comparison is made between the surface aspect of cleared indium pads of three wafers with different initial In field plating thicknesses and the higher pressure setting (see Table IV). For the smallest thickness of around 300 nm, we observe some crevices in the surface. We speculate that due to the limited overburden (only 300 nm of In plated on the field for trenches 800 nm deep) and the inherent "hilliness" of the initial plated In surface, that some of the initial topography of the In surface after plating, might have depressed features which might already initially reach the level of the Si field and therefore that of the final intended In pad surface level. These depressed features may then be revealed as crevices after In CMP removes the surrounding In

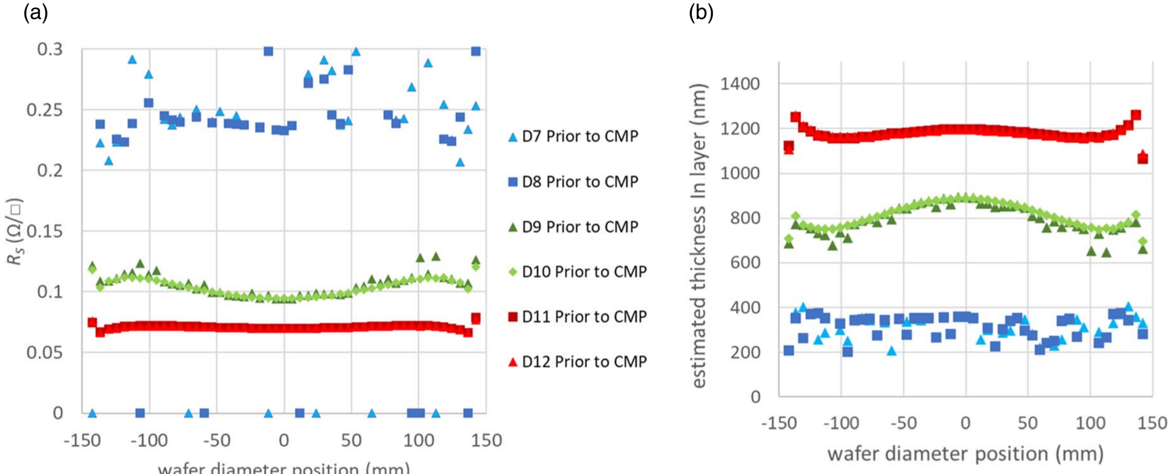

Fig. 8. (a) Measured sheet resistance (R_S) across a wafer diameter, for the 6 patterned wafers (with different intended initial indium plating thickness above the Si field), for the patterned In wafer CMP experiments specified in Table IV. (b) For these same wafers, the derived In thickness based on R_S and bulk In resistivity reference.

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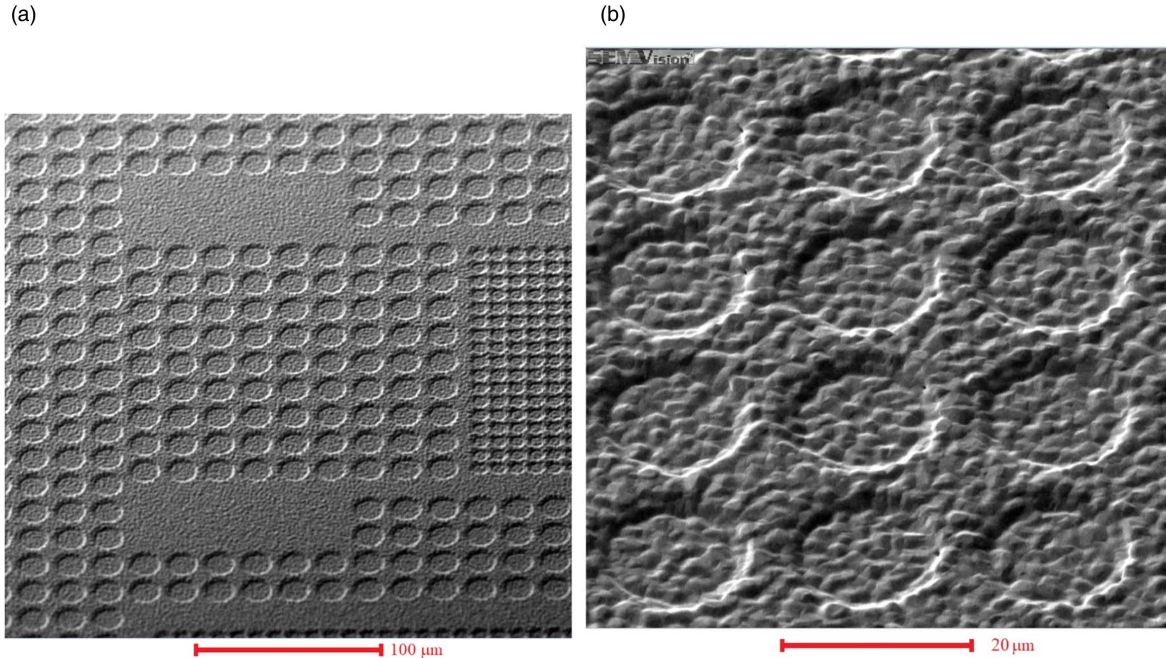

Fig. 9. (a), (b) View of a patterned wafer after In plating, showing non-uniformity between surface areas directly above circular trenches and Si field (for on average 780 nm initial plating above Si field).

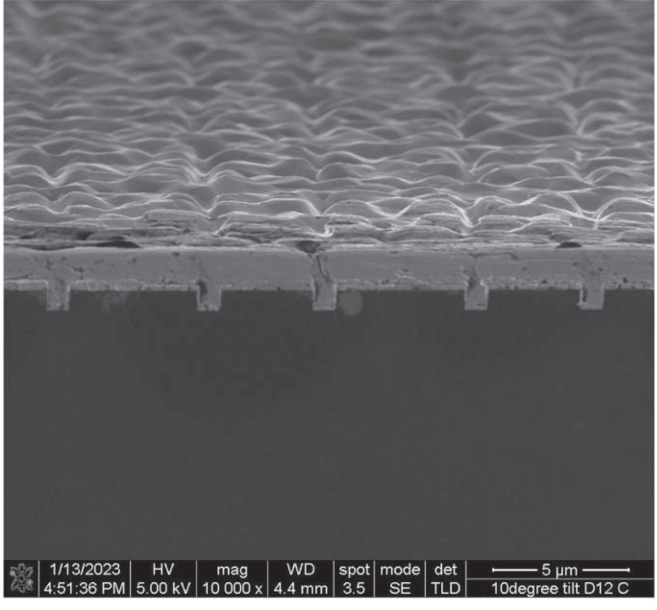

Fig. 10. Cleaved wafer SEM cross section image of a wafer section with patterned structures. Please note that this was an image from a patterned wafer not included in the patterned CMP-tests, with some differences, such as 175 nm TiW for the patterned wafer and trenches of about 800 nm width and depth.

plating overburden. On the In pads on the wafers with higher initial thickness, we do not observe such larger crevices.

Secondly, Fig. 13 shows that the wafers with 300 nm or 850 nm initial In thickness (D8 and D10), have a final cleared In pad surface after CMP which contains small scale pitting, and also some larger spots where grains seem to have been more uniformly etched. By contrast, the wafer D12 with higher initial plating thickness of 1200 nm does not show such pitting. For D12, there is also some larger scale surface roughness visible, which however might be more related to the natural grain structures of the plated indium. On the other hand, on wafer D12, some remaining particle contamination was visible, of which the precise nature is not yet clear.

Figure 14 shows that for the wafer D11, for which the In pads had been "overpolished" for several minutes in order to fully clear unstructured areas, in the center, some grains have undergone some etching. The In pads in the center do not show the small-scale pitting yet, however, but the outer dies of D11 do, as in D08 and D10.

Next, AFM is used to quantify bond pad dishing and roughness on 4 wafers from Table IV, with 3 different initial plating thicknesses, across the 4 mentioned bond pad pitches (5–20 μm) and at wafer locations corresponding to center, mid-diameter and edge dies (Fig. 15).

Figure 15 shows profiles across 10 μm pitch pads at the center die. Dishing can be seen to be of the order 40–50 nm

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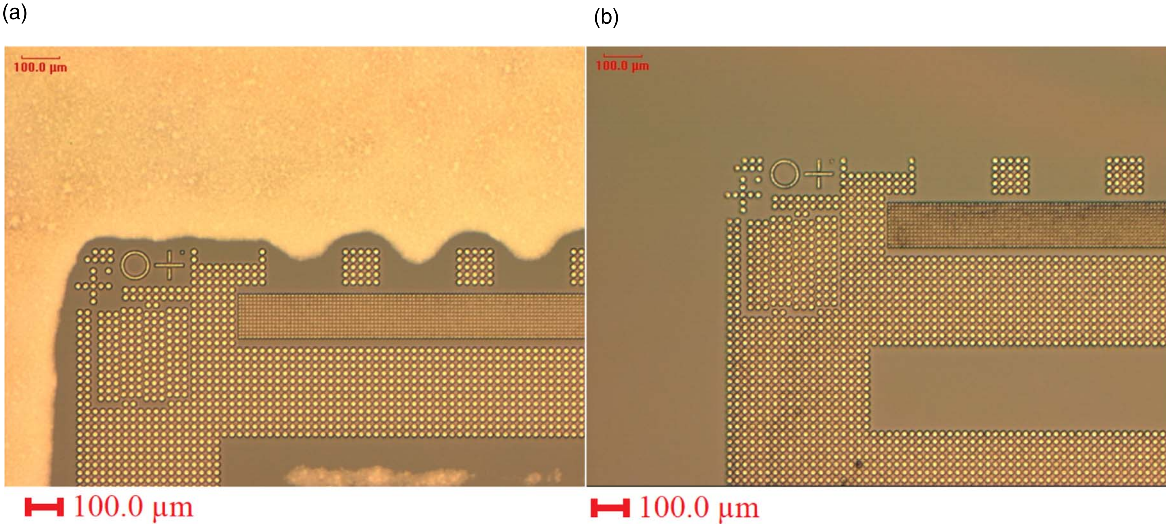

Fig. 11. (a) Optical microscope view of partially cleared wafer around the circular In pad structures, but with still indium left in areas without trenches (D12) (b) wafer D11 (see Table IV) after 6 min of overpolish, used to fully clear the open field areas not containing any structures.

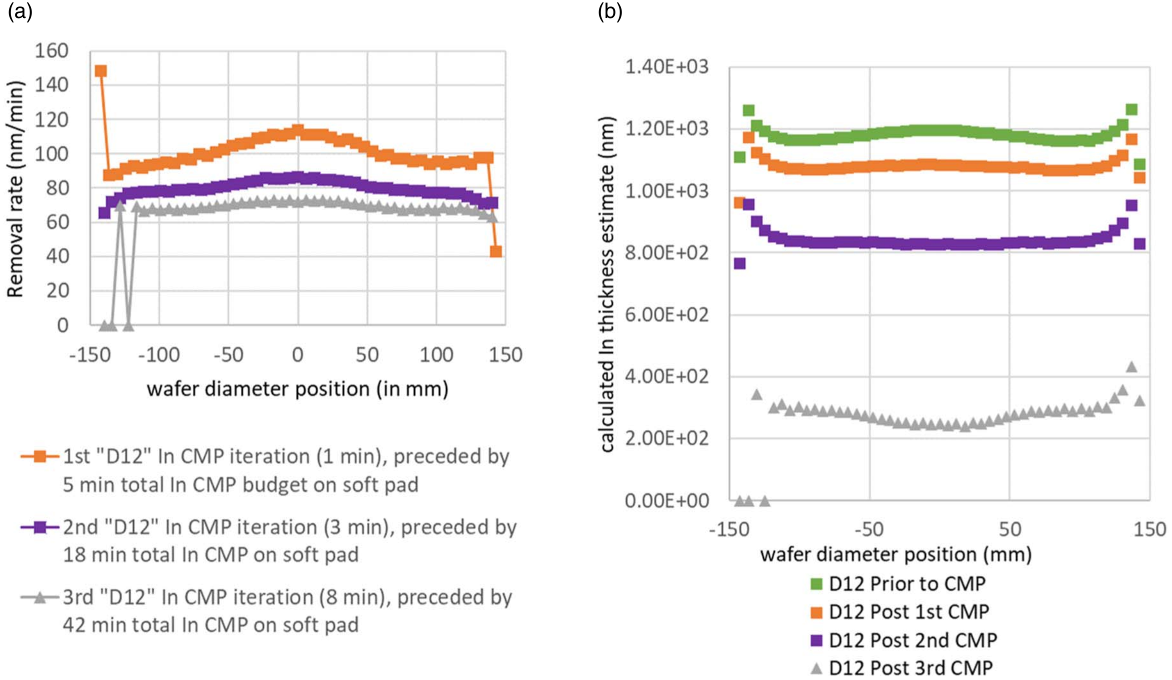

Fig. 12. (a) Average removal rates observed during successive In CMP processing iterations for patterned wafer D12 (1200 nm initial In thickness, 1.5 psi in wafer center, Table IV). The first removal rates are the average removal rates during the first 1 min of CMP, which was preceded by in total 5 min of In CMP on other wafers. The 2nd removal rates series are the average rates over the next iteration, consisting of 3 min of In CMP, preceded by in total 18 min of exposure of the soft pad to In CMP. The 3rd iteration consisted of 8 min of CMP, when before the soft pad had been used for in total 42 min of In CMP. Some outliers and unmeasurable sheet resistance values are present near the wafer edge. (b) Corresponding In layer thickness estimated based on R_S.

in this case. As was already noticeable from the SEM images, the wafers with the lower initial plating thickness (D8 and D10) have a higher frequency surface roughness pattern, corresponding to the small-scale surface pitting phenomenon, while the wafers with 1200 nm initial In thickness have a lower surface roughness frequency profile, more corresponding to the dimension of the In grains.

The range of the surface roughness across these samples (characterized through the range between maximum and minimum height inside the indium pad) is of the order 25 nm.

Figure 16 shows a calculated average dishing across several pads, averaged over a circle with diameter 90% of the full indium pad diameter. It can be observed that the wafer with lower initial plating thickness (850 nm), has lower average dishing than the two wafers with 1200 nm initial In thickness. Also of note is that dishing ranges from about 40 nm for the pitches up to 10 μm, to about 70 nm for 20 μm pitch structures. Many earlier experimental works and models have established the general trend of increasing dishing with larger pitch, and these models are able to predict these through modelling for some other CMP processes.[28–30]

The overpolished wafer D11 does not have a significantly higher dishing than wafer D12, on which In was just cleared around the structures. Other results also show that the edge die In bond pads are slightly more dished, probably due to within-wafer non-uniformity of the plating and the CMP

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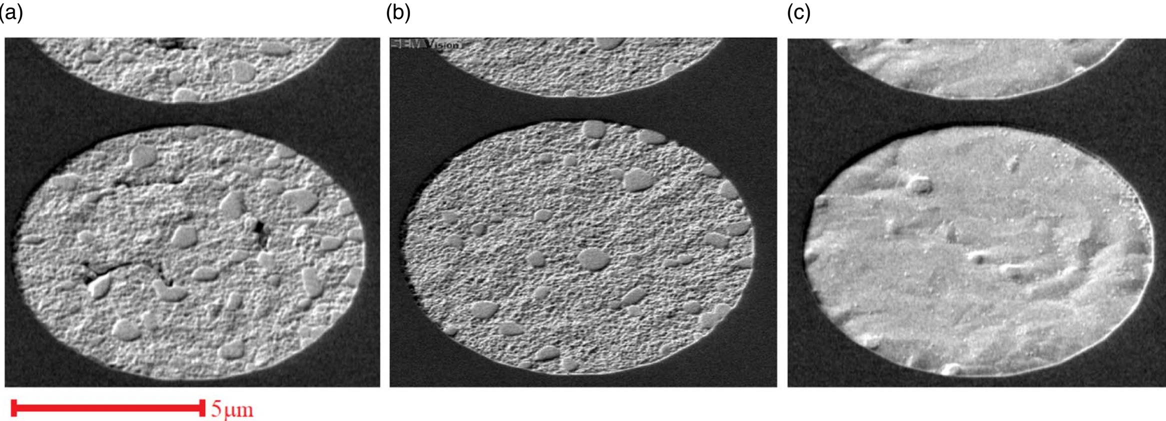

Fig. 13. Scanning electron microscope images of cleared circular In pads with 10 μm pitch and about 9 μm diameter after indium CMP cleared the immediate surrounding Si field, but not yet fully cleared the indium from large open Si field spaces. (a) For a wafer with initial In plating thickness ≈ 300 nm (D08, center) after 4 min CMP (b) initial In plating thickness ≈ 800 nm (D10, edge) after 11.5 min CMP (c) initial In plating thickness ≈ 1200 nm (D12, center) after 15 min CMP (see also Table IV).

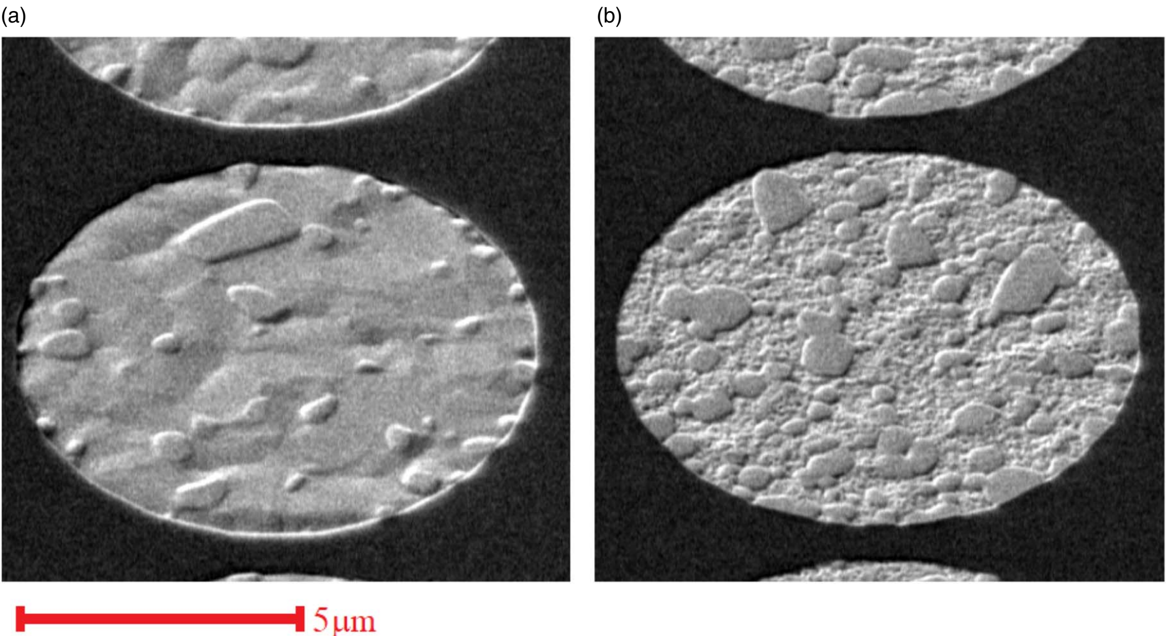

Fig. 14. SEM images of 10 μm pitch In pads in center (a) and near the wafer edge region (b) for a wafer to which 15 min of In CMP was first applied to clear In closely around the In pads, but In remained in die areas without structures and in wafer center also around structures. A following 6 min of In CMP to fully clear In also in the latter regions was applied, after which above inspection images were taken.

process. There, calculated average dishing goes up to 80 nm at the edge die for the larger structures.

In Fig. 17, AFM scan maps of in this case 7 μm pitch In bond pads are shown. For tests on D10 (850 nm initial In, 1.5 psi), we again see pitting corrosion patterns as in the SEM images (Fig. 13). For D11 (center location) and D12, which have the 1200 nm initial In plating, we do not observe the small-scale pitting patterns seen on D10, but more a pattern related to grain roughness. Dishing ranges between about 50–100 μm. However, careful examination shows that many of these last two wafers instead show some evidence of local depressions near the indium bond pad edge, which may likely be caused by some galvanic corrosion effect. In a few pads we also see some larger local erosion near the pad edge up to about 200 nm. More AFM scan maps for different In pad structure pitches and wafer locations can be found in the Supplementary data.

The SEM-EDX analysis (Fig. 18) showed that inside the indium pad surfaces, the main EDX peaks correspond to indium, but there is also a significant peak for Cu (see example for wafer D11, Fig. 18). We assume that this Cu comes from the Cu seed which was applied after TiW barrier deposition, to aid plating. It is known that Cu in proximity of indium will rapidly diffuse into indium and contribute to intermetallic regions and might spread through it towards the revealed surface. Another possibility is that Cu atoms removed during the CMP process from the barrier area, might have dissolved into the slurry and have been taken up by the CMP-ed In surface. The peaks from C and N might be due to some remaining organic compounds present on the In surface, either related to the slurry, corrosion inhibitor or cleaner. The SEM-EDX analysis of the cleared Si field shows only a peak for Si, showing that both In and the TiW were cleared well.

3.3. Discussion

In this work we reported on investigations into possible CMP processes for indium, capable of clearing indium around

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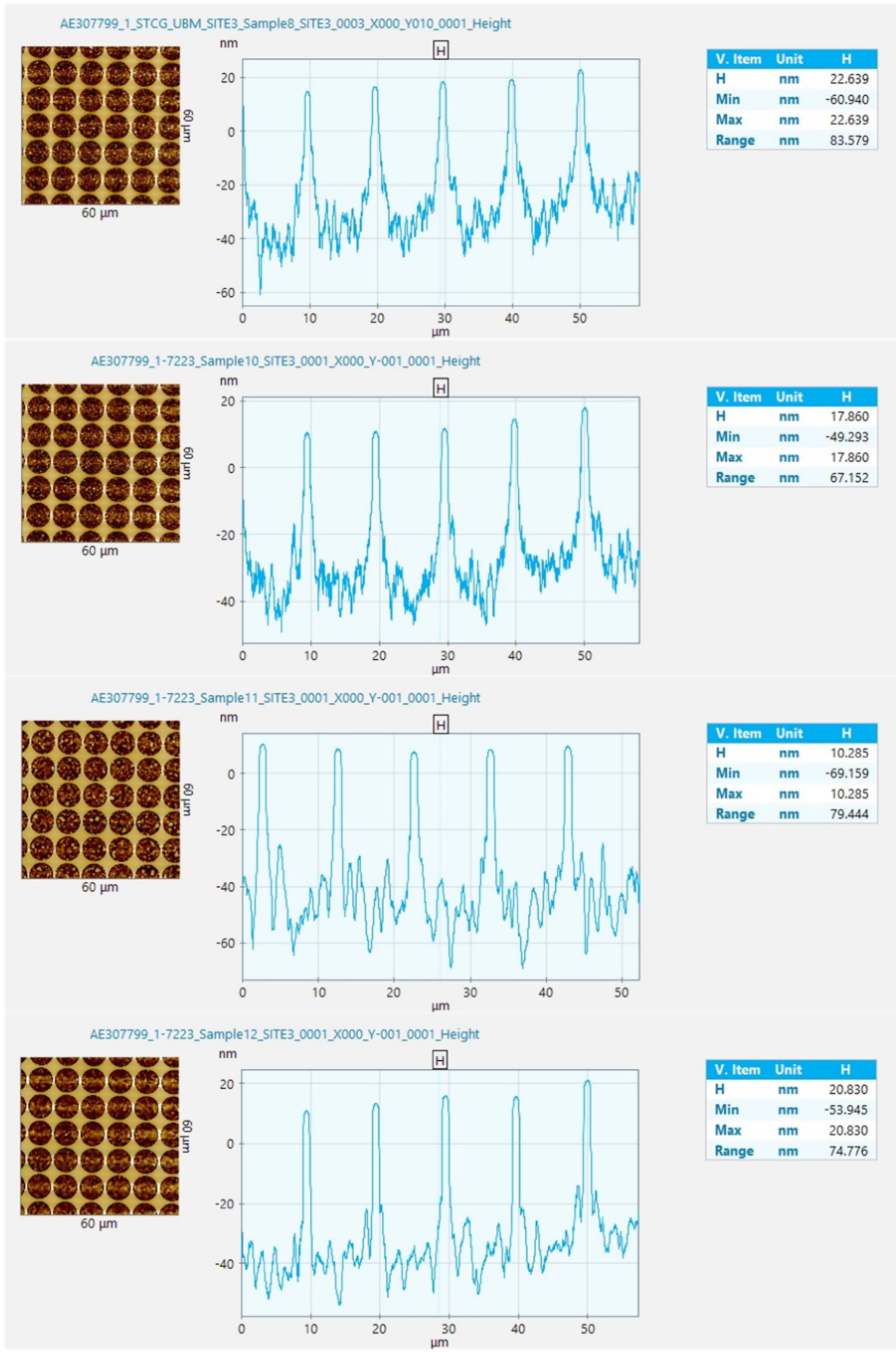

Fig. 15. AFM-scans for 10 μm pitch In pads after indium CMP. Shown samples are for the center dies, and for respectively, from top to bottom: the ≈ 300 nm (D08), ≈ 850 nm (D10), ≈ 1200 nm initial In wafers, with overpolish (D11) and 1200 nm without overpolish but higher CMP pressure (D12).

plated indium bond pads, leading to fairly good quality of indium bond pads and surrounding silicon field.

The finding that a typical copper CMP hard pad leads to severe scratching can be understood from a hardness comparison between indium and the hard pad (Table I). Although in principle, hardness values obtained with different methods are not directly comparable,[10] we can still deduce that the hardness of the used hard pad is very likely several times higher than that of indium. In that case, it is predicted that when the harder asperities of the hard pad are pressed against

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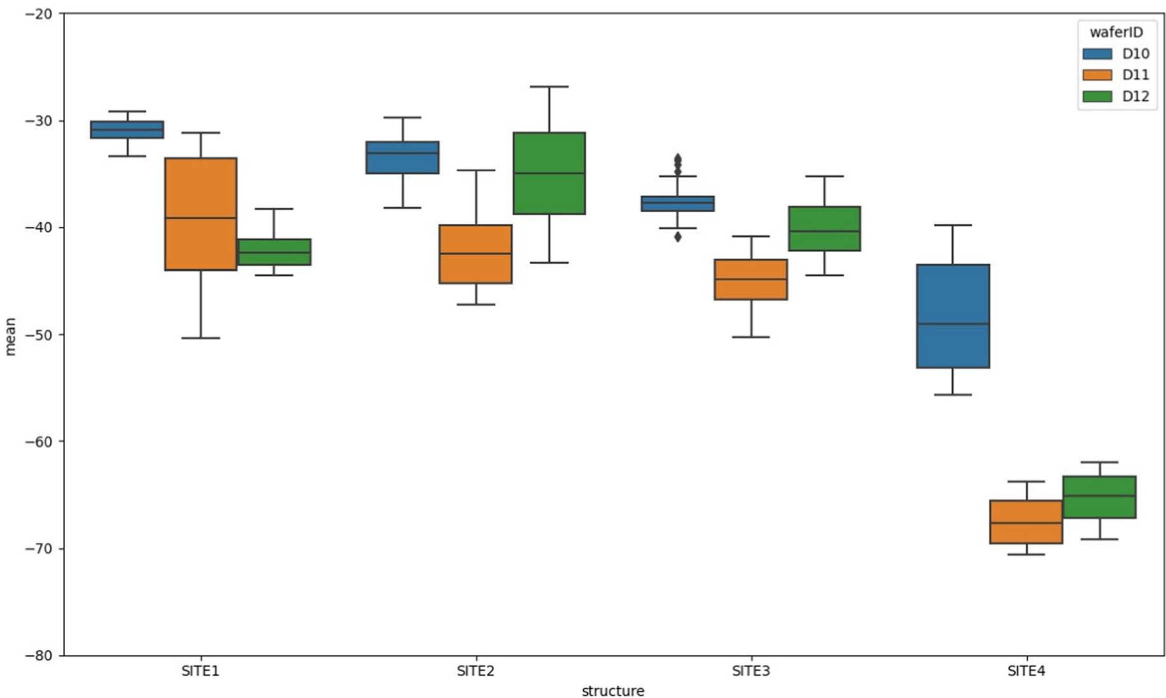

Fig. 16. Mean In pad dishing (in nm) for samples of In pads, for 3 different wafers (D10: initial plating thickness 850 nm, higher pressure), D11 (initial In: 1200 nm, lower pressure, overpolished to fully clear In in empty field), D12 (initial In 1200 nm, higher pressure, only cleared In directly around pads). The four sites correspond to circular pad areas with pitch 5.0, 7.0, 10.0 and 20.0 μm, respectively. Results are shown here for the center dies. The dishing was determined as the difference between the Si field height and the average height of the In bond pad, limited to a circular area with diameter 90 percent of the full pad diameter.

and rubbed along the softer indium surface with sufficient pressure, the indium surface will yield, which will then lead to plastic deformation scratches in the indium surface.[31,32] Given that we know that the used hard pad has porosity of about a few microns, then the pad asperities are probably also of this size order. The largest scratches after hard pad In CMP are indeed a few μm wide (Fig. 2). Furthermore, it seems that such hard pad CMP within a large scratching regime is not beneficial to the material removal rates, as can be observed from the low hard pad removal rates obtained.

Therefore, there are two important arguments against the use of such hard pads for indium CMP. This should certainly not be considered as a sign of general malperformance of the hard pad, as these pads were instead designed for CMP of harder metals such as copper. It shows that one should preferentially choose pads which have a well-adapted, lower hardness than the material to be polished.

The currently achieved removal rate with soft pad CMP is sufficient for obtaining reasonably qualitative results in an acceptable polishing time. The present investigation was still partially exploratory, and further increases in obtained removal rates might still be achievable. So far, only an alkaline barrier slurry has been tested on the soft pad. Further tests might be able to reveal other suitable slurries. Slurry composition is probably also further optimizable towards In CMP. More detailed mechanistic insight into the chemical and mechanical components of the In CMP process may in future lead to such improvements through choices of the most appropriate slurry and pad.

The applied CMP pressure profiles and other earlier discussed processing settings have themselves not yet been further optimized against experimental data. In future, efforts could be made to tune the pressure profiles further in order to obtain higher within-wafer uniformity of the In CMP.

The exact mechanisms affecting the surface quality of indium bond pads deserve further investigation beyond the visual observations collected here. As shown in the Results section, there is evidence of two different types of corrosion. Firstly, there is small-scale pitting corrosion (horizontal scale of tens or hundreds of microns) across the In bond pad surface. It is mostly present on the wafers with the lower initial In plating thickness, and partially on the longer overpolished edge regions of wafer D11. This pitting corrosion introduces some roughness of order 25–50 nm depth (overall depth below the Si field is usually not more than 100 nm). Such local pitting corrosion could be driven by interaction of the In surface with the slurry. Under the pH 11 and present H_2O_2 oxidizer conditions, according to the Pourbaix diagram of In[15] the surface might still be in a partially passivated state and therefore containing a thin layer of In_2O_3, but at this pH it is already near the transition zone of the passivation towards corrosive regime.[15] Therefore, conditions for local attack of the passivating film might exist, for example near In grain boundaries or other types of defects, which could also be introduced by the mechanical CMP abrasive regime. This would then lead to local penetrations of the passivating film, allowing local corrosive dissolution of the In surface below, which is a known corrosion pitting mechanism.[18,33]

The wafers D12, and less-overpolished parts of D11 show no such small-scale pitting corrosion across the full indium bond pad, but instead here there is evidence of local corrosion near the bond pad edge, which leads to some local deeper depressions of depth sometimes exceeding 200 nm below the

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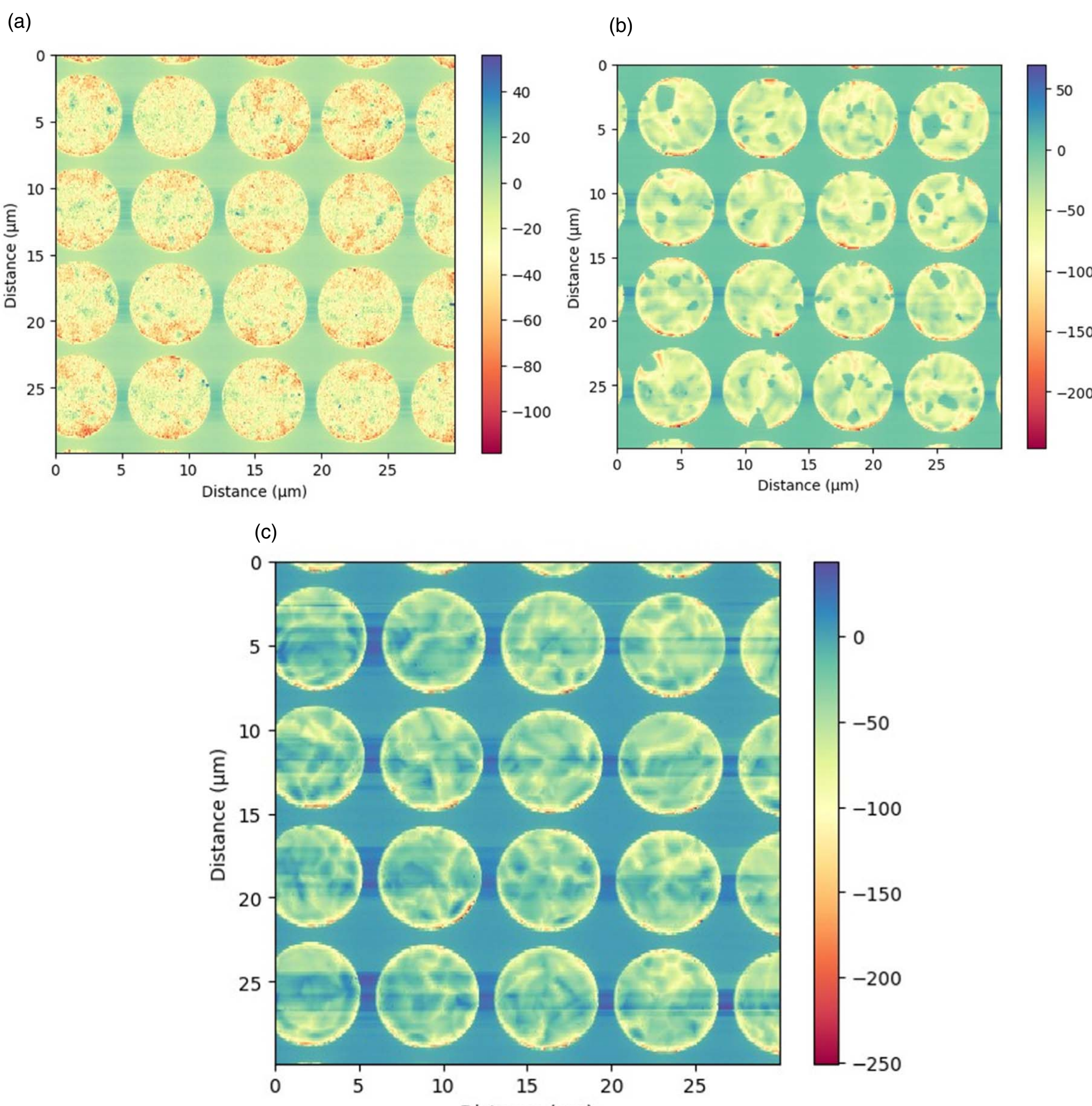

Fig. 17. AFM images of indium damascene bond pad structures of 7 μm pitch after In CMP, showing evidence of either local pitting corrosion or possible galvanic corrosion near In bond pad edge. Die locations are at mid-wafer diameter. (a). For wafer D10 (initial 850 nm In above Si field, CMP pressure 1.5 psi regime in central wafer regio) (b). For wafer D11 (initial 1200 nm In above Si field, CMP pressure 0.8 psi regime in central wafer regio, applied overpolish to remove In in empty field). (c). For wafer D12 (initial 1200 nm In above Si field, CMP pressure 1.5 psi regime in central wafer regio).

Si field level. Such damage might be caused by a local bi-metallic galvanic corrosion reaction,[18] in this case presumably involving possibly the indium metal on the one hand, and the TiW barrier or still present Cu in the Cu–In intermetallic present near the bond pad edge, on the other hand. It should also be noted that in the wafers which show the pitting corrosion across the indium pad, the possibly deeper galvanic corrosion damage near the In bond pad barrier does not seem to be present, so these two types of corrosion might be competing processes. On the other hand, without further investigation we should also not yet exclude the possibility that some of these local depressions might be related to trench filling issues during plating.

We hypothesize that the small-scale pitting and bond pad edge erosion might be promoted by the level of "overpolish" that is applied. Due to the initial non-uniformity in surface height above and next to In pads on small scale, and also large density differences for structures in the used mask design, indium right above the pads is cleared first, and some extra polish which in some cases could take up to more than 5 min, is needed to clear the field area. During the overpolish phase, some dishing of the In pads may occur, but after some degree of dishing, the lower height would somewhat prevent further increase of the dishing.

However, during this period, the chemicals in the slurry are still in contact with the freshly polished In surface and may cause oxidation and corrosion effects. But in this case the chemically reacted surface material is no longer as quickly removed as during the earlier more efficient In CMP phase. This might create conditions for noticeable corrosion impact to originate in the surface, while the surface material is no longer quickly removed. It is however well possible that still other factors determine the difference in indium pad surface appearance.

In the wafers with 300 nm and 850 nm initial thickness, we expect that the In surface depression above the In trenches is larger than in the 1200 nm initial plated In wafers. This might

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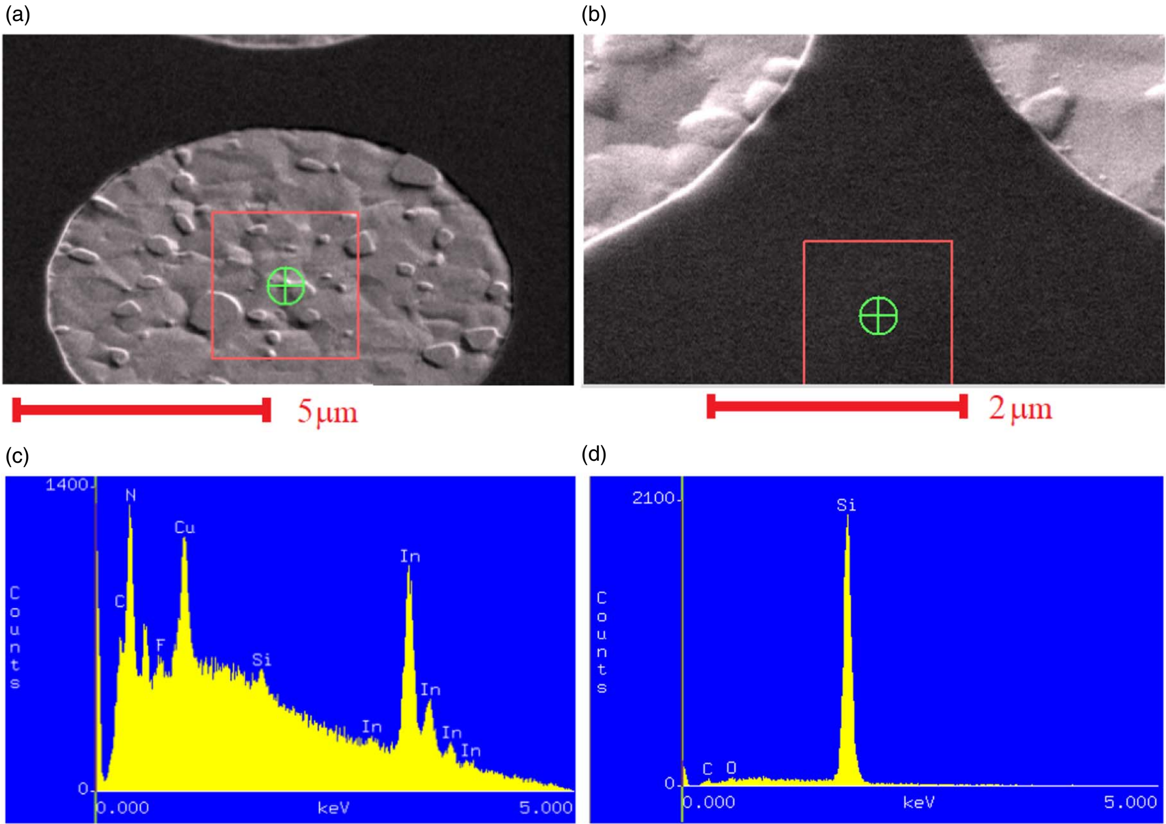

Fig. 18. SEM-EDX element analysis for the indium pad surface (a) and (c) and cleared Si field area surface (b) and (d) for a wafer with around 1200 nm initial In plating thickness, after having been fully cleared both directly around In pads as in the Si field areas without structures (D11, see Table IV).

increase the period during which the already cleared In surface is exposed to the slurry without sufficient further material removal due to mechanical friction. This could then explain why in these wafers (D08 and D10) and in the overpolished parts of wafer D11 we see the pitting corrosion appearing, and not in D12.

The exact mechanisms behind the observed pitting and galvanic In bond pad edge corrosion mechanisms remain unclear, and would require further study of the indium/slurry or indium/TiW/slurry systems, using electrochemical lab techniques such as discussed for example in Roy (2016).[18] Reducing the overpolish regime by increasing CMP uniformity, and introduction of more corrosion-preventing additives[18,34] might allow reduction of the corrosion effects. As stated in the "Methods" section, we already apply a BTA-rinse after polishing and before cleaning of the wafers, but perhaps this protocol could be improved. A recent study investigated the use of three corrosion inhibitors to prevent pitting corrosion on indium/In_2O_3 through potentiometric and polarization studies and found that the compounds 1(H)-naphthotriazol (NTA), 1H-BTA, and 1H-1,2,3-triazole, in this particular given order, are increasingly effective in delaying the onset of pitting corrosion.[16]

From the patterned wafer tests, it can be deduced that the larger tested thickness of 1200 nm may lead to better surface quality, except for the local edge galvanic corrosion. But the AFM measurements also showed that overall dishing was larger in the case of the largest initial plating thicknesses.

Although through AFM we have characterized the achievable dishing, erosion was not yet clearly quantifiable based on current results. A larger scan area would be needed to compare the height loss of Si field and In in different areas and quantify it reliably. The CMP removal rate of Si field material and TiW barrier for the used slurry could also be characterized.

For increasing the understanding of the variability of dishing, erosion and corrosion across the different bond pad pitch structures, wafer locations and for different initial In plating thicknesses, set-up of a model for the indium CMP process would be very beneficial. A first step into modelling In CMP could be work towards calibrating so-called step-height models, such as these of Chandra and Fu (2003).[28] In simulations of the CMP process, these models can describe the height evolution of metal (here indium) in trenches, versus the height evolution of the material in the field (in this case, Si). They require as input the knowledge of the removal rate of the metal and field material (thus, also the removal rate selectivity). This model can also describe effects of elastic deformation of the pad which can cause increased pressure on elevated areas and decreased pressure inside already dished areas. However, they do not explicitly represent other mechanical and chemical aspects. Instead, such models usually require a number of data points on dishing of structures with different pitches over several stages of the CMP processing to allow their callibration.[28]

The simple step-height models do not explicitly take into account effects of within-wafer variability or the more precise details of interaction between slurry abrasives, pad, chemicals and the wafer surface.[28,29] Whenever such interactions are more complicated and not fully uniform across the wafer, more advanced models may be needed to be able to reliably

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predict dishing and erosion across structures and wafer locations. More advanced models consider wafer/abrasive/pad interactions more explicitly.[29,35] Even more advanced models will also incorporate chemical effects explicitly together with the modeling of the mechanical processes.[19,29,30]

Such more detailed models for In CMP would be useful in order to allow informed actions towards reducing the non-uniformity of the current In CMP process, and more in-depth understanding of dishing, erosion and corrosion effects. The set-up of such models falls outside the scope of the current study, however.

The achieved dishing presents a marked improvement over the previous mechanical polishing study.[5] An important question remains whether the currently achieved level of dishing and surface roughness would be sufficient for the foreseen goal of indium bump-to-pad bonding. The indium bump in such a bonding would be slightly smaller than the In bond pad, and fit inside the In bond pad area. During bonding, the bump and pad may also slightly deform, possibly countering the currently present surface roughness. Therefore, some tolerance to dishing and surface roughness is possible, and the current level of dishing might be acceptable for some successful indium bump-to-pad bonding. Proof of concept implementation and studies on the impact of bonding quality on qubit operation and decoherence times might have to be tested in future.

The variability of the removal rate is also still a matter of some concern. The decrease in removal rate might be due to a combination of wear of the pad material and clogging of the soft pad pores. Indium's softness may make it more prone to accumulation in pad pores than other often CMP-ed materials might do, for which a pad quality related decrease in removal rate is usually much slower. This pad removal rate degradation was not yet reversible, and for Ta barrier, test rates also became abnormally low after a long In CMP session, necessitating a polishing pad replacement. In future, tests could be conducted to check whether introduction of pad conditioning for the soft pad might partially remedy the pad deterioration effect.

4. Conclusions

In the present study, CMP of blanket and patterned plated indium wafers is demonstrated. It was found that soft pad indium CMP is preferential: it causes less scratching and allows reaching higher removal rates, compared to the use of the harder pad process. For the soft pad, removal rates were found to increase with pressure, up to 130 nm min^{-1}, using an alkaline barrier slurry. For this same slurry and at the same pressure, the removal rate was much lower for the hard pad ($\approx$20 nm min^{-1} versus $\approx$ 80 nm min^{-1} at 1.5 psi downforce pressure).

For patterned indium wafers, we find a large difference in indium CMP clearing time for indium on top of the Si field directly around indium trench structures, and on the other hand, in the larger empty areas not in proximity of any pad or dummy indium trench structures, for which an extra overpolish of several minutes was needed to polish away the indium up to Si.

After indium CMP, indium bond pad surface roughness (expressed as range between maximum and minimum with a pad) was found to be of the order $\approx$25–50 nm, and average dishing mostly $\approx$40–80 nm. This presents a significant improvement over previous results with purely mechanical polishing.

After indium CMP, the indium bond pad surface quality was best at the highest tested initial In plating thickness (1200 nm). For the lower initial thicknesses, corrosion pitting takes place, which contributes to the small-scale roughness of the In bond pads. On the other hand, for the wafers with In bond pads without much corrosion pitting, some localized corrosion near indium bond pad edges is tentatively observed through AFM. Further electrochemical investigations would be needed to enhance understanding of these corrosion effects and how to possibly counter them.

The In CMP overpolish needed to fully clear the empty die areas does not lead to a strong increase in surface roughness or dishing, but may in some cases increase the occurrence of corrosion pitting.

EDX shows that Si areas are cleared from TiW and indium, but may contain some trace amounts of organics and low levels of contaminants in a few cases. The In pads show the presence of some Cu atoms in addition to indium.

4.1. Outlook

The obtained results in this work, it being an explorative first experimental study on indium CMP, should not yet be considered definitive and optimal. Further process improvements and more thorough characterizations of the indium CMP process will be needed in future. Also, the level of investigation is not yet sufficient to allow one to elucidate in detail the underlying chemical and mechanical processes at work during the In CMP process. Further studies could certainly shed more light on the chemical and physical fundamentals, through either more detailed experimental work (on electrochemical interactions such as pitting corrosion or bi-metallic corrosion) and more systematic study of dishing and erosion.

The set-up of an indium CMP model which would integrate aspects of known chemical and mechanical aspects of the In CMP, might be needed to gain more fundamental understanding and could aid in the optimization of the In CMP process. Effective models would probably need to include wafer non-uniformity and chemical effects on the surface quality. Set-up of such more advanced models would also require more knowledge on consumables (pad and slurry properties) and more detailed understanding of removal CMP mechanisms for indium, but also for Si and TiW.

Future improvements on the currently presented experimental CMP methodology could also include transfer to a multiple-step process with different platens, all equipped with soft pads suitable for indium CMP. In that way we could also consider the usage of endpoint detection in order to avoid unnecessary overpolishing, stopping near the transition to barrier or Si substrate.

Further "dummification" of the mask design to avoid the large structure density differences in the current test mask would be beneficial,[36] in order to improve the uniformity of the indium plating and CMP processes.

Some further points of quality improvement were identified in the current study, such as reduction of In pad surface pitting, bond pad edge corrosion and prevention of particle

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defectivity. Improvement of CMP uniformity can be expected to aid in quality improvement.

We speculate that possibly the achieved parameters for surface roughness and dishing may already be near-sufficient for indium bump to indium pad bonding trials, as during such bonding tests, there may be some tolerance to a limited dishing, as during bonding the indium may still plastically deform, due to its inherent plasticity. Tests for the proof of concept of In bump to CMP-ed In pad bonding for cryo-3D integration of quantum computing qubits are still needed to prove whether the obtained quality and yield of the bonding would be acceptable. The present work could serve as a starting point for obtaining the required In bond pads.

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