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Sub-pJ/b 28 nm CMOS Inverter-Based Direct-Drive Optical Tx Using 1060 nm SM VCSEL Enabling 60 Gbaud NRZ Transmission Over 5 km SMF

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***Abstract*—This article presents a direct-drive optical transmitter (Tx) using common-cathode (CC) type single-mode (SM) 1060 nm vertical-cavity surface-emitting laser (VCSEL) suitable for medium-reach transmission ($<$ 5 km) for linear pluggable optics (LPO)-based inter-cluster datacenter interconnect. The VCSEL driver featuring 4 channels is implemented in 28 nm bulk complementary metal-oxide semiconductor (CMOS) technology and co-designed with a GaAs-based 1060 nm VCSEL array. A VerilogA-based VCSEL device model with self-heating-induced voltage and optical power adjustments is introduced to facilitate co-design and (co-)optimization electro-optical interface. Two CMOS inverter-based equalizers, based on an active inductor and a T-coil, are used to enhance the driver bandwidth. A group-delay compensator is added to compensate the VCSEL group-delay variation and improve in-band gain flatness. The VCSEL features an optimal -3 dB BW of 31 GHz with 6 mA current bias. The optical Tx successfully demonstrated 60 Gbaud non-return-to-zero (NRZ) transmission with a SM 1060 nm VCSEL over 5 km single-mode fiber (SMF) using a 10-tap feed-forward-equalizer (FFE) with a record-high FEC-corrected bitrate-distance product of 283.47 Gb/s.km. For the electro-optical transmission experiment, the optical Tx achieves a Tx energy-efficiency of 0.94 pJ/b with a 6 mA current biased VCSEL having -2.7 V supply at the CC terminal.**

***Index Terms*—1060 nm, continuous time linear equalizer (CTLE), common-cathode, linear pluggable optics (LPOs), direct-drive, optical transmitter (Tx), single mode, VCSEL, voltage-mode driver, VCSEL driver.**

I. Introduction

The exponential growth of artificial intelligence (AI) workloads, particularly the training and inference of large language models (LLMs), has led to an unprecedented surge in data traffic throughout AI clusters across hyperscale datacenters [1]. As distributed training, real-time data sharing, and extensive LLM synchronization between AI accelerators become more common, there is a growing need for optical datacenter interconnects (DCIs) that support higher baud rates [2] and medium-reach (MR) transmissions up to 5 km. As data rate rises, conventional retimer-based optical transceivers (OTRx) become increasingly complex, requiring advanced on-chip equalization and digital signal processing (DSP) to address significant signal deterioration, which in turn significantly increases power consumption. As a result, next-generation DCIs must deliver high BW, low-latency, as well as energy-efficient optical links to sustain these hyperscale datacenters while keeping overall power consumption and operational costs within practical limits. In comparison to DSP-based OTRx, linear pluggable optics (LPO) offer a low-power, low-latency alternative by transferring DSP functions to computing hosts or switching ICs as depicted in Fig. 1(a). To achieve sub-pJ/bit energy efficiency, LPOs get rid of on-chip serializers/deserializers, retimers, and clock recovery circuits. However, the absence of DSP reduces the modules' tolerance to signal impairments, requiring low-loss electrical interconnects and careful electro-optical (EO) co-design to maintain link integrity [3]. While LPOs are useful in reducing power and latency for DCIs, ongoing integration trends are extending these benefits toward co-packaged optics [4]. Although co-packaged optics offers higher BW density and energy efficiency, it introduces greater challenges in reliability, thermal management, and serviceability. In contrast, LPOs maintain the flexibility of hot-swappable modules, providing a practical and lower-risk transition toward fully integrated optical interconnects [5].

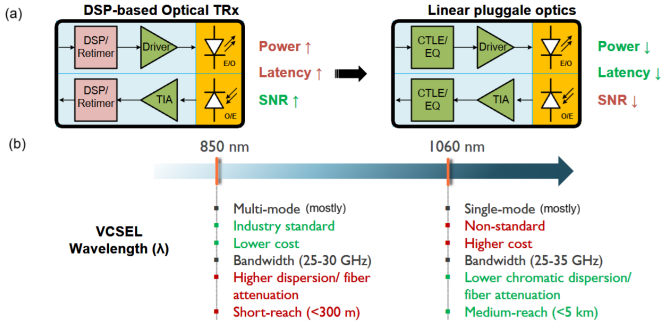


Fig. 1. Comparison between (a) DSP-based OTRx and LPOs, and (b) VCSEL wavelength 850 nm and 1060 nm.

Unlike an indirect modulator-based Tx, such as a Mach-

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Zehnder modulators [6] or microring modulators [7], [8], VCSELs enable low-power, direct-drive operation with reduced signal swing. Recent demonstrations in advanced nodes of CMOS technology have notably enhanced the performance of the OTRx [9], [10], [11], [12], [13], [14], [15], in particular, enabling energy efficiencies approaching the sub-pJ/bit regime and validating their suitability for low-power linear direct-drive EO interfaces. However, sub-1V CMOS-based modules encounter signal integrity issues, especially with high-order modulation formats like four-level pulse-amplitude-modulation (PAM4) due to stringent signal-to-noise (SNR) margins. Despite doubling the data rate, PAM4 incurs a 9-10 dB SNR penalty compared to NRZ modulation, and it requires additional on-chip circuits for linearity enhancement, consuming more power. For similar baud-rate PAM4 requires almost 33% more BW than NRZ [16]. Consequently, NRZ modulation appears to be the optimal choice for ultra-low energy-per-bit transmission through direct-drive Tx modules.

Traditionally, 850 nm VCSELs [17], [18], [19] have been widely adopted as the benchmark technology for low-power short-reach optical DCIs. These lasers with a small footprint support low drive voltage with low bias current, enabling high data rates supported with on-chip BW-extension techniques [11], [13], [14]. 850 nm VCSELs typically utilize multi-mode fiber (MMF), offering cost-effective, high-BW optical transmission suitable for short-reach transmissions up to 300 m, which can be extended with up to 2 km with DSP techniques. However, as data rates for VCSEL-based links are estimated to increase to 200 Gb/s [20] and the optical link extends beyond the 2 km range for hyper-scale inter-cluster DCIs [21], the inherent limitations of 850 nm VCSEL links become increasingly apparent. In particular, significant modal dispersion and high MMF attenuation (around 2-3 dB/km) pose serious challenges to achieving efficient data transmission over longer distances [22]. To overcome these challenges, 1060 nm SM VCSELs appear as a more effective alternative for MR optical links ($<$ 5 km). A brief comparison of 850 nm VCSELs with 1060 nm alternatives is illustrated in Fig. 1(b). Operating over SMF, 1060 nm VCSELs offer lower fiber attenuation ($\sim$1 dB/km) and negative chromatic dispersion enabling a higher bitrate-distance product [22].

This article, which is an invited extension of our work [23], details the development of a direct-drive optical Tx comprising a 4-channel driver in 28 nm CMOS process, co-designed with an SM 1060 nm VCSEL array for MR DCIs ($<$ 5 km). The VCSEL driver leverages several CMOS-inverter-based BW enhancement techniques, including additive CTLE with active inductors [24], [25], T-coil-coupled resistive feedback with gate-peaking CTLE [26], and a single-ended driver with Q-shaping shunt-series inductive peaking [27]. Beyond these established techniques, this work introduces three novel contributions. Firstly, a novel, negatively-coupled transformed-based series peaking is introduced for the input buffer. Secondly, it has proposed a GDC circuit to equalize the low-biased underdamped VCSEL response. Thirdly, a compact dynamic VerilogA VCSEL device model featuring self-heating effects is proposed to facilitate co-simulation of the optical Tx interface. Notably, the optical Tx successfully demonstrated 60 Gbaud NRZ optical transmission using a SM 1060 nm VCSEL over a 5 km SMF with estimated BER $<$1e-12 after forward-error-correction (FEC). The optical VCSEL-based Tx showcased a record-high FEC-corrected [17] bitrate-distance product of 283.47 Gb/s.km, and exhibited a Tx energy efficiency of 0.94 pJ/b among integrated drivers using 1060 nm VCSEL-based optical links.

The rest of the article is structured as follows: Section II presents an overview of the co-designed VCSEL-based Tx module. Section III and IV detail the driver circuit and the proposed VCSEL device model, respectively. Section V summarizes the measurement results, including 1060 nm VCSEL characteristics, driver response, and time-domain EO transmission, with a comparison to the current state-of-the-art solutions. Section VI concludes with a summary of the main contributions.

II. Overview of Optical Transmitter Using Single-mode 1060 nm VCSEL

The integrated CMOS-based driver comprises four parallel differential input channels, as illustrated in Fig. 2(a). Each channel delivers a single-ended output that directly drives the anode of a 1060 nm VCSEL within a CC array. Typically, the VCSEL's forward voltage (> 1.5 V) exceeds the nominal $0.8-1$ V supplies for the sub-micron CMOS technologies. A negative bias at the CC terminal enables the required forward voltage to be achieved with a sub-1 V anode voltage. This allows the CMOS driver to operate at its nominal supply without high-voltage devices, stacked transistors, or large output swings, enabling an energy-efficient inverter-based driver architecture and reducing overall Tx power consumption. The anode bias currents for the VCSELs are generated on-chip. Furthermore, the driver incorporates an SPI interface and an associated digital register bank, enabling programmable configuration of multiple circuit-level parameters (gain, peaking, current bias, etc.).

Fig. 2(b) provides an overview of the architecture of a single channel interfaced with a VCSEL. A wideband buffer with digitally tunable gain at the input of each channel provides input impedance matching, differential to single-ended conversion, and compensates for input channel loss. The differential inputs of the buffer are matched to a differential 100 ohm resistance with impedance-controlled transmission lines. A single-ended CMOS inverter-based output driver provides the digitally tunable bias current to the VCSEL and modulates the anode voltage. Between the stages, two cascaded continuous-time-linear-equalizers (CTLEs) based on CMOS inverters provide digitally tunable pre-equalization to extend the baudrate-to-VCSEL-bandwidth ratio. Notably, the VCSEL BW is strongly bias-dependent and decreases significantly at lower bias currents, posing challenges for low-power modulation. As shown in Fig. 2(c), the first CTLE introduces a real zero to provide low-frequency equalization, while the second CTLE contributes a pair of complex zeros that offer high frequency, narrow-band peaking. Together, these CTLEs compensate for the limited VCSEL BW across various bias conditions. The optical output power of the

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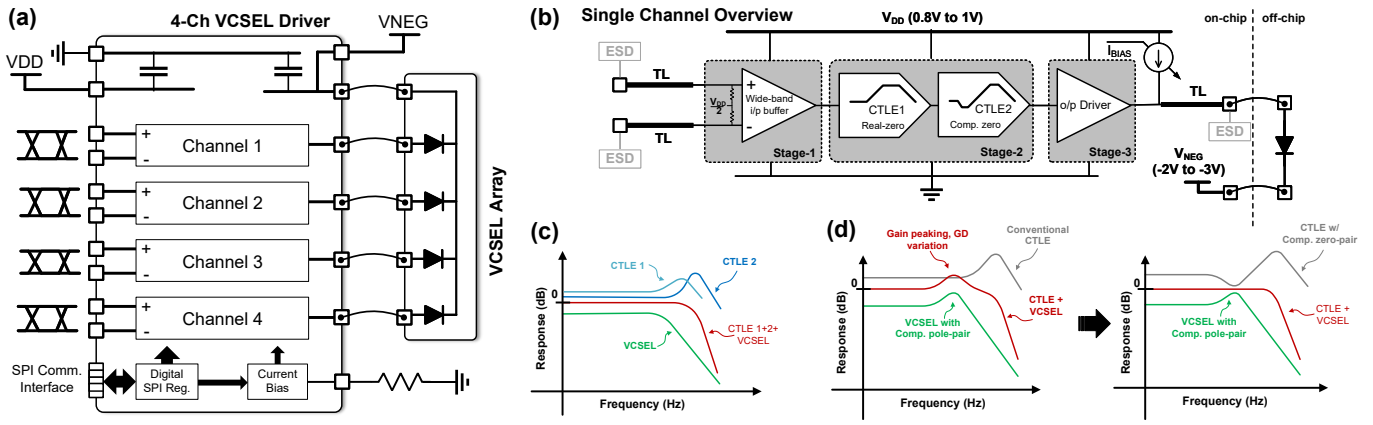


Fig. 2. (a) Overview of the CMOS-based 4-channel VCSEL driver with 1060 nm common-cathode VCSEL array, (b) top-level overview of a single channel, (c) combined CTLE response for BW extension, (d) the proposed technique for compensating VCSEL low frequency peaking.

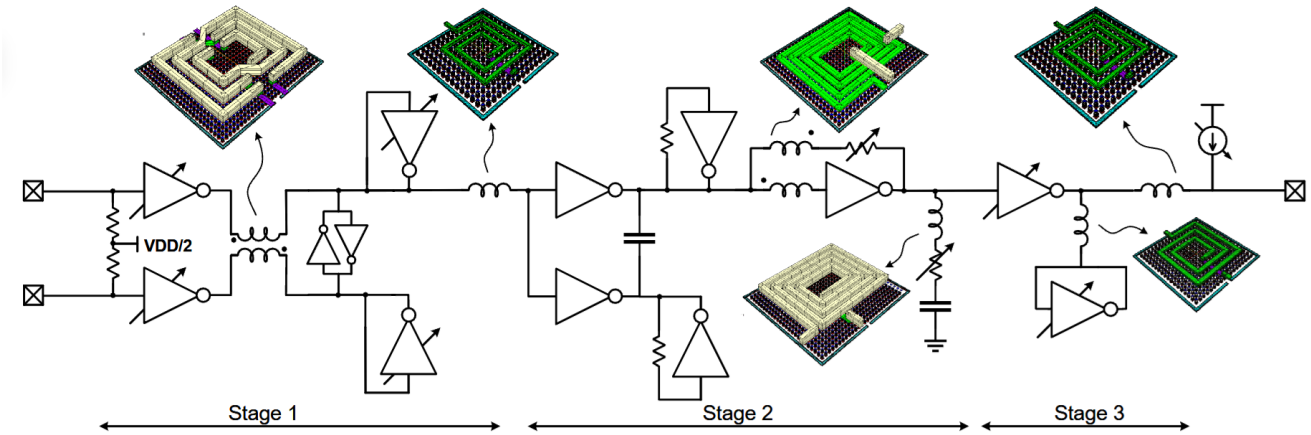


Fig. 3. Schematic overview of the 4 identical channels of the single-ended CMOS-inverter-based driver.

VCSEL is proportional to the modulating current, and at high frequencies, it is limited by the single-pole interface of electrical pads of cathode or anode terminals [28]. Challenges arise at low bias, while the optical output also showcases an underdamped modulation response with reduced damping and sharp second-order roll-off. The resulting in-band peaking associated with significant group-delay variation leads to time-domain overshoots and a closed eye diagram. As illustrated in Fig. 2(d), an additional pair of complex zeros with reduced damping ($< 1/\sqrt{2}$) helps to create a passband droop to compensate for the VCSEL gain variation. Accordingly, the second CTLE features a group-delay compensator circuit (GDC) to pre-distort the driver's frequency response in order to flatten the overall EO modulation response of the Tx. The differential 100 Ω termination to VDD/2 sets the input bias and self-biased 1/gm loads maintain subsequent nodes at VDD/2. For fine tuning of bias adjustments SPI-controlled PMOS/NMOS pull-up/down switches were employed at each stage's output.

III. VCSEL Driver Circuit Design

The 4 identical channels of the driver are used to drive the array of 4 CC-type VCSELs. A circuit-level overview of CMOS-inverter based single-ended channel is shown in Fig. 3. Each channel consists of 3 cascaded stages. Stage-1 uses a series-coupled transformer for BW extension and a differential 100-ohm resistor biased with VDD/2 in the middle for input matching. Stage-2 comprises a low frequency CTLE and a high frequency narrow-band peaking CTLE with a GDC circuit. A series inductor between Stages 1 and 2 compensates BW loss from on-chip interconnects. Stage 3 implements a single-ended output driver featuring shunt–series inductive peaking for enhanced high frequency performance.

A. Stage-1: Differential-to-Single-ended Input Buffer

The driver receives differential data from DAC-based host interface for improved common-mode noise immunity, then preferably converts it on-chip to single-ended signal to facilitate low-power equalization. The schematic of the CMOS-inverter-based input buffer for differential-to-single-ended conversion is shown in Fig. 4. This work proposes a series transformer-based BW extension for the programmable-gain-amplifiers [29]. The outputs of the inverter-based transconductors, gm_{b1} and gm_{b2} are coupled in series with a transformer (L_1, L_2) having a coupling factor of k_{12} with magnetic flux opposing each other. While inverter-based transconductors exhibit higher nonlinearity, this is of less concern in NRZ

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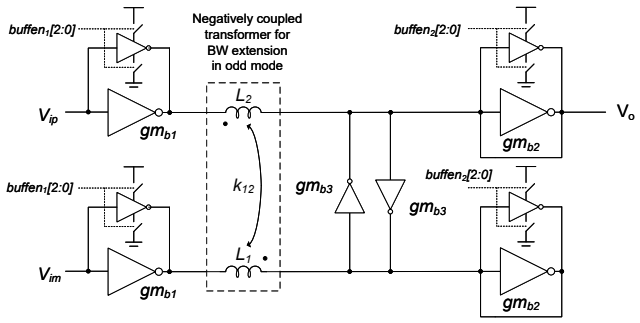


Fig. 4. Overview of the schematic of the input buffer.

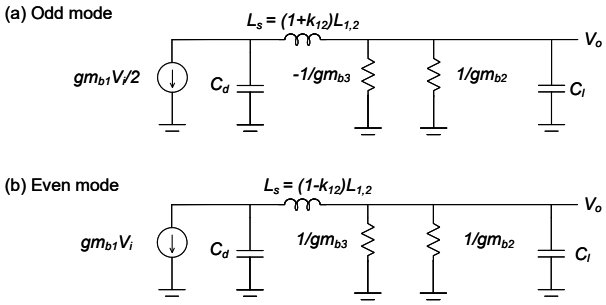


Fig. 5. Linearized equivalent circuit for the input buffer for (a) odd mode (differential) and (b) even mode (common-mode) analysis.

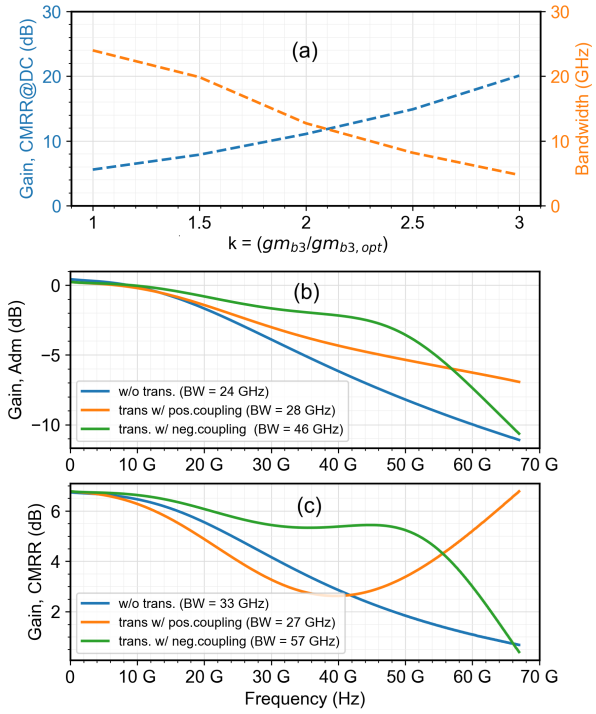


Fig. 6. (a) Simulated tradeoff between CMRR and bandwidth of the input stage, (b) post-layout simulated gain A_{dm} and (c) post-layout simulated CMRR variations of the input buffer with different transformer settings.

compared to PAM4 modulation [15]. However, the pseudo-differential input stages suffer from a limited common-mode rejection, which is mitigated through the use of cross-coupled inverters. The cross-coupled pair creates a latching action that reinforces differential switching while opposing common-mode variations and thus introduces a positive feedback to generate a low frequency negative resistance of $-1/gm_{b3}$.

Now for the series transformer with negative magnetic coupling the effective series inductance L_s in odd-mode increases to $(1+k_{12})L_{1,2}$ where $L_{1,2} = L_1 = L_2$. However, for even mode with common-mode inputs, L_s reduces to $(1-k_{12})L_{1,2}$. The equivalent circuits of the input buffer for differential and common-mode analysis can be derived as shown in Figs. 5(a) and (b) respectively. At low frequencies, the differential-to-single-ended gain, A_{dm} and the common-mode gain A_{cm} can be derived as, $-gm_{b1}/2(gm_{b2}-gm_{b3})$ and $-gm_{b1}/2(gm_{b2}+gm_{b3})$ respectively. The common-mode rejection ratio, CMRR = A_{dm}/A_{cm}, can be improved by increasing gm_{b3}. However, the dominant pole in odd-mode, $\omega_p = (gm_{b2}-gm_{b3})/(C_d+C_l)$ decreases, resulting in decreased BW. A tradeoff is achieved between the CMRR and the BW of the circuit by choosing the optimum, $gm_{b3,opt} \approx gm_{b2}/4$. Fig. 6(a) shows the impact on the CMRR and BW as gm_{b3} is varied by a factor of k over $gm_{b3,opt}$. Now the voltage gain of the input buffer, normalized to its low frequency gain, can be derived as,

$$H_b(s) = \frac{1}{1 + R_l C_t s + L_s C_d s^2 + R_l L_s C_d C_l s^3} \quad (1)$$

where $R_l = 1/(gm_{b2}-gm_{b3})$ is in odd mode and $C_t = C_d + C_l$. Then the dominant pole can be approximated as [30], $\omega_{p,o} \approx 1/R_l C_t$ while the inductive peaking due to the pair of complex-conjugate poles (CCPs) occurs at the resonant frequency, $\omega_n = 1/\sqrt{L_s(C_d||C_l)}$. For $\omega_{p,o} < \omega_n$, the odd mode frequency response exhibits a roll-off beginning at $\omega_{p,o}$ followed by a peaking centered around ω_n. Increasing L_s shifts the series-resonance peaking at ω_n closer to the dominant pole $\omega_{p,o}$, making the BW extension more effective and compensating for the 3-dB gain loss due to the dominant pole. However, excessive peaking from reduced damping can introduce large group-delay variations and time-domain overshoot [31]. To avoid this, the inductors L_1, L_2 are preferred to be designed with a sufficiently low Q-factor.

Fig. 6(b) and (c) show the post-layout simulated variations of the differential gain A_{dm} and CMRR of the input buffer without a transformer and with positively or negatively coupled transformers. In odd-mode with a negatively coupled transformer in series, the effective series inductance L_s increases, shifting the pair of CCPs closer to ω_p, thereby extending the BW. As illustrated in Fig. 6(b), the series transformer ($L_1 = L_2 = 125$ pH) helps to extend the BW of the input buffer, and with a negative magnetic coupling and k_{12} = 0.44, the effective BW can be extended up to 1.9 times. For similar values of L_1, L_2 and k_{12}, but with a positive magnetic coupling, the BW extension is less effective. However, for even-mode analysis (see Fig. 5(b)), the dominant pole, $\omega_{p,e} \approx (gm_{b2}+gm_{b3})/C_t$ increases compared to that in case of odd-mode analysis, i.e, $\omega_{p,o} \approx (gm_{b2}-gm_{b3})/C_t$. Since the effective series inductance L_s decreases in the case of even-mode analysis, the inductive peaking moves further away from the dominant pole, causing less BW extension

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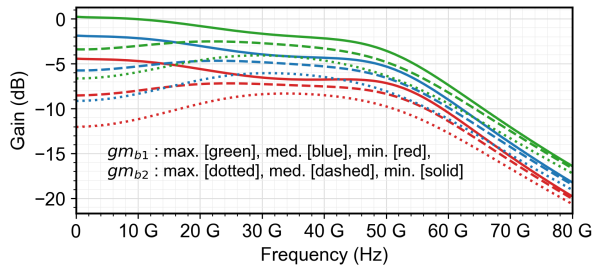


Fig. 7. Post-layout simulated magnitude responses of the differential-to-single-ended gain (A_{dm}) of the input buffer.

(1.2 times) compared to the odd-mode response. Overall, the common-mode rejection at higher frequencies improves, as evident from the frequency responses of the CMRR shown at the bottom of the Fig. 6(c). The high frequency improvement is more pronounced, and the BW extends further in the case of a negatively coupled transformer compared to its positively coupled counterpart.

The transconductors, gm_{b1} and gm_{b2} are programmable using 3-bit binary control-words gmen_1[2:0] and gmen_2[2:0] respectively. Fig. 7 shows post-layout simulated differential-to-single ended gain's magnitude responses of the input buffer for different settings of gm_{b1} and gm_{b2}. The low-frequency gain can be set to 0 dB for 600 mVpp differential input signals from the host interface with DSP/DAC and can be reduced down to -12.5 dB to accommodate larger signal swings.

B. Stage-2: CTLEs and Group Delay Compensator (GDC)

The stage-2 comprises two CTLEs with a series RLC resonance-based GDC circuit Z_{gdc}. A comprehensive network model of the stage-2 is shown in Fig. 8. The first CTLE is modeled with a voltage gain of H_{ctle1} and output impedance Z_{o1}. The second CTLE is represented using the input impedance Z_{in} and a voltage gain of H_{ctle2} with output impedance Z_{o2}. For the voltage dividers, H_t=$Z_{in}/(Z_{in}+Z_{o1})$ and H_{gdc}=$Z_{gdc}/(Z_{gdc}+Z_{o2})$, the total gain of stage-2, $H_{stage2} = H_1H_2$ where $H_1 = H_{ctle1}H_t$ and H_2=$H_{ctle2}H_{gdc}$.

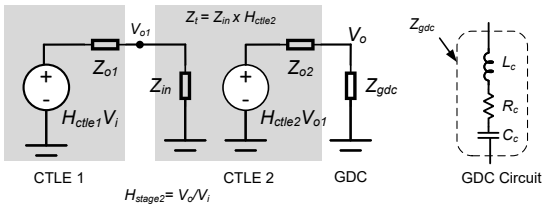


Fig. 8. Linearized equivalent circuit model of the combined CTLE stage.

1) First CTLE: Fig. 9(a) shows the architecture of the first CTLE with its linearized equivalent circuit in Fig. 9(b), which is based on the inverter-based additive type CTLE [25]. Bulzacchelli et al. in [24] originally proposed this additive architecture with differential current-mode architectures. However, the source-degenerated CTLEs limit the affordable signal swing for low-VDD (< 1 V) supplies. Zheng et al. in [25] proposed an alternative using inverter-based circuits with a

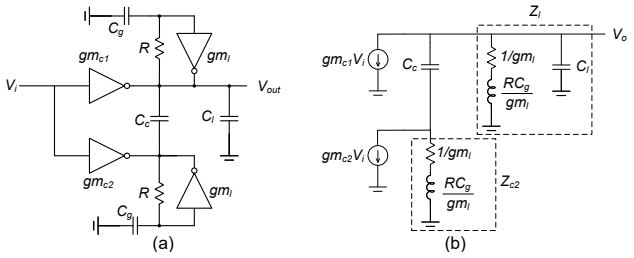


Fig. 9. (a) Schematic of the additive CTLE, and its (b) equivalent circuit.

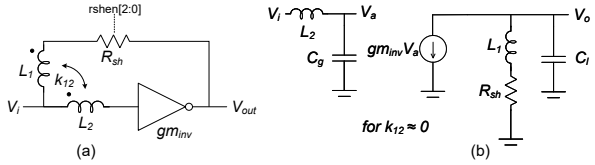


Fig. 10. (a) Schematic of the second CTLE, and its (b) equivalent circuit.

single-ended architecture featuring active inductors to improve the high-frequency roll-off. As illustrated in Fig. 9(a), the transconductor gm_{c1} with inverter-based load $1/gm_l$ generates the low frequency gain of $-gm_{c1}/gm_l$. At high frequencies, when the ac-coupled capacitor C_c is shorted, the voltage gain increase to $-(gm_{c1}+gm_{c2})/2gm_l$. The voltage gain of the first-stage CTLE can be derived from Fig. 9(b) as,

$$H_{ctle1}(s) \approx H_{ctle1}(0).\frac{1+sC_cZ_{c2}(gm_{c1}+gm_{c2})/gm_{C1}}{1+sC_c(Z_l+Z_{c2})} \tag{2}$$

where $H_{ctle1}(0)$ is the gain at DC, $Z_{c2} = (1+sRC_g)/gm_l$ and $Z_l = Z_{c2}||(1/sC_l)$. Without the active inductor (i.e, $R = 0$) the left-half-plane (LHP) zero can be estimated for large ac-coupling capacitor $C_c >> C_l$ as, $\omega_{z1} \approx gm_{c1}gm_l/[C_c(gm_{c1}+gm_{c2})]$ and the LHP poles can be approximated as $\omega_{p1} \approx gm_l/2C_c$ and $\omega_{p2} \approx 2gm_l/C_l$. Now, with the help of the active inductor such that $R >> 1/gm_l$, an extra LHP zero ($\approx 1/RC_g$) is introduced, which compensates the effect of the dominant pole, ω_{p1}. The active inductor also helps to delay the high frequency roll-off by converting the pole at ω_{p2} into CCPs similar to the shunt-inductive peaking as mentioned in [32].

2) Second CTLE: The first CTLE primarily compensates for low/mid-frequency losses; hence, a second CTLE is employed to enhance high frequency components near the Nyquist frequency and further extend the BW. In this work, a T-coil-based gate-peaking technique is used for the inverter with resistive shunt feedback [26], as shown in Fig. 10(a). While resistively fed back CMOS inverters can also extend BW, their inherent first-order response restricts their usefulness for CTLE functionality. Incorporating an inductor in the shunt feedback introduces a zero and a pair of CCPs, but the peaking remains constrained by the damping provided by the shunt resistor. Adding a series gate-peaking inductor enables resonance with the gate-source capacitance C_{gs}, achieving enhanced peaking at the resonance frequency. The linearized equivalent circuit for the CTLE with T-coil with positive magnetic coupling having a coupling factor k_{12} is illustrated

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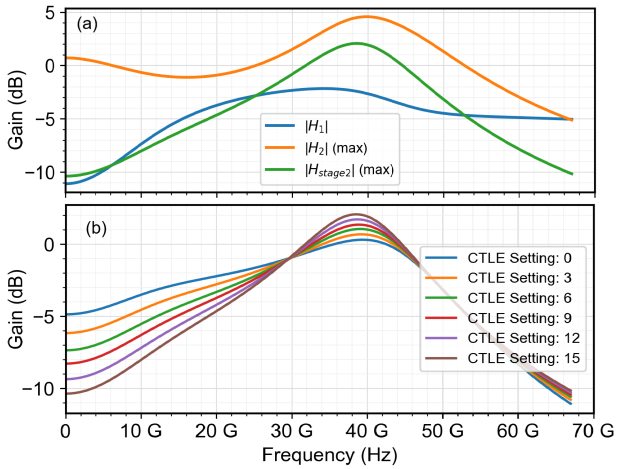


Fig. 11. (a) Post-layout simulated magnitude responses of H_1, H_2, and their combined response H_{stage2} without the GDC circuit. (b) Post-layout simulated H_{stage2}-peaking variation for settings 0 to 15.

in Fig.10(b), where the effective mutual inductance in the T-coil can be denoted as $M = k_{12}\sqrt{L_1 L_2}$. Without the mutual coupling, i.e, for $k_{12} = 0 \Rightarrow M = 0$, and the circuit simplifies to a shunt–series inductive peaking network, and then the voltage gain $H_{ctle2}(s)$ can be approximated as,

$$H_{ctle2}(s) \approx \frac{H_{ctle2}(0)}{(1+s^2C_{gs}L_2)} \cdot \frac{(1+sL_1/R_{sh})}{(1+sC_lR_{sh}+s^2C_lL_1)} \quad (3)$$

where $H_{ctle2}(0)$ is the DC gain. The transimpedance $Z_t(s)$ = $Z_{in}(s).H_{ctle2}(s)$ where the input impedance $Z_{in}(s) \approx (1+s^2C_{gs}L_2)/(gm_{inv}+sC_l+s^2gm_{inv}C_{gs}L_2)$. Without the coupling between the inductors, the circuit configuration creates a LHP zero, $\omega_z = R_{sh}/L_1$, a pair of complex poles with resonance frequency $\omega_{n1} = 1/\sqrt{L_2C_{gs}}$ and a second pair of CCPs with resonance frequency $\omega_{n2} = 1/\sqrt{L_1C_l}$. The damping factor for the second pair of CCPs can be expressed as, $\zeta = 0.5R_{sh}\sqrt{C_l/L_1}$. Now with positive magnetic coupling, the effective inductance of the T-coil branches increases by M, shifting the CCPs to a lower frequency but with reduced damping. Although narrowband, the peaking of the second CTLE increases, and when combined with the first CTLE, results in a broader overall magnitude response with enhanced high frequency boost. Fig. 11(a) shows the post-layout simulated magnitude responses of H_1 and H_2 with the CTLE peaking set at its maximum setting, and their combined response H_{stage2} without the GDC circuit. Fig. 11(b) further illustrates how the combined CTLE response varies as the shunt-resistor value of the second CTLE is swept digitally using 4-bit control word rshen[2:0] from 0 to 15 in steps of 3. Increasing the CTLE setting (i.e, reducing R_{sh}) strengthens the high frequency peaking by lowering the low frequency gain, enabling programmable compensation to tailor the required equalization level.

3) GDC: A low-biased VCSEL exhibits an underdamped modulation response with noticeable passband peaking, leading to sharp second-order roll-off, reduced BW, and significant group-delay variation that distorts the eye diagram. Prior work has addressed this problem using differential group-delay

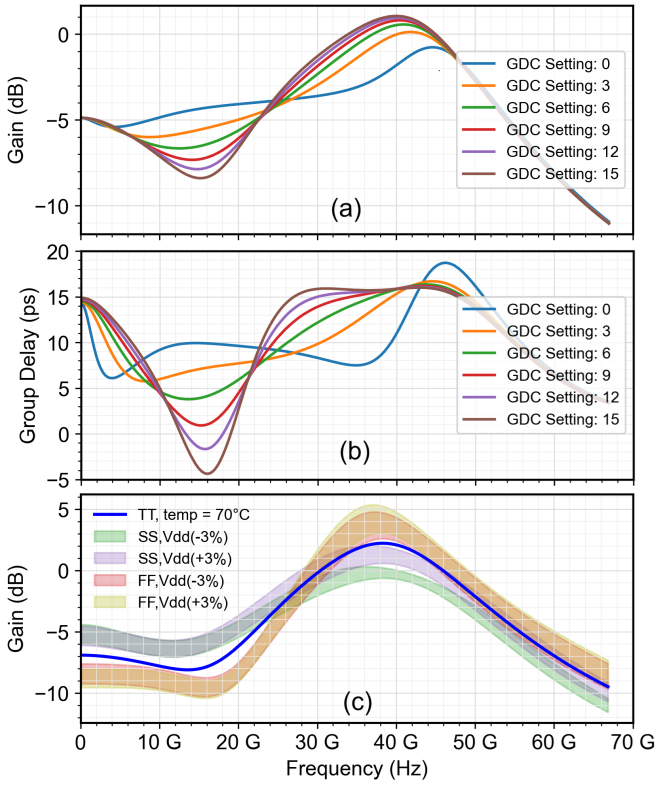


Fig. 12. Post-layout simulated stage-2 gain H_{stage2} responses showing (a) notch-depth, (b) group delay variation as the GDC setting is swept from 0 to 15 in increments of 3 and (c) gain variation across process corners and supply variations with 0–100 degC temperature range (denoted by shaded region)

equalizers. Tsunoda et al. [33] introduced a positive-feedback-based compensator to increase low-frequency group delay, and Bakhtiar et al. [34] proposed a current-mode differential complex-zero equalizer using parallel filter paths. However, these multi-stage differential architectures operate with high damping and are not well-suited for low-power single-ended designs. A single-ended complex-zero CTLE based on a parallel RLC degeneration network was later proposed in [14], but its asymmetric compensation limits linearity and effectiveness, and the improved complementary-drive in [15] enhances linearity but requires higher VDD to enhance signal swing in the presence of resistive degeneration. For the group delay compensation, Z_{gdc} is proposed as shown in Fig. 8. At frequencies lower than CTLE peaking within the passband, the output impedance $Z_{o2} \approx R'_{sh}$, where $R'_{sh} = R_{sh}||1/gm_{inv}$. Z_{o2} forms a voltage divider with Z_{gdc} with a transfer function $H_{gdc}(s)$ which can be derived as,

$$H_{gdc}(s) \approx \frac{1+sR_cC_c+s^2L_cC_c}{1+s(R_c+R'_{sh})C_c+s^2L_cC_c} \quad (4)$$

$H_{gdc}(s)$ introduces a pair of CCZs along with a pair of CCPs with the same resonance frequency, $\omega_n = 1/\sqrt{L_cC_c}$. However, for positive R_c and R'_{sh} the damping factor of the CCZs, $\zeta_z = 0.5R_c\sqrt{C_c/L_C}$ is lower than that of the poles, $\zeta_p = 0.5(R_c+R'_{sh})\sqrt{C_c/L_C}$. By digitally tuning R_c and R'_{sh}, ζ_z and ζ_p can be adjusted independently such that $\zeta_z < 1/\sqrt{2}$ and $\zeta_p > 1/\sqrt{2}$. With these settings, a controlled passband

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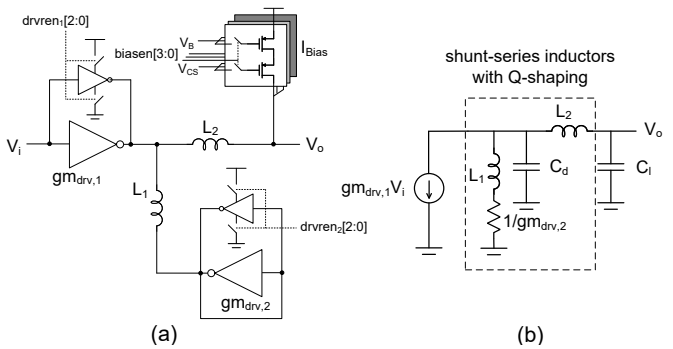


Fig. 13. (a) Schematic of the output driver with current bias, and its (b) linearized equivalent circuit.

droop can be produced, which helps in equalizing the passband peaking in the VCSEL.

Figure 12(a) and (b) show the post-layout simulated gain H_{stage2} and group delay variation of the complete stage-2, highlighting the digitally controlled tunability of the notch-depth introduced by the GDC circuit. However, for a fixed GDC setting, the notch and gain peaking frequency undergo a little variation across process corners, with supply and temperature variation as illustrated in Figure 12(c).

C. Stage-3: Single-ended Output Driver

The output driver modulates a CC-type VCSEL array with the CC-terminal biased at a fixed voltage. The anode terminals are driven by the driver, generating a forward voltage ($>$ 2 V) across the device. Grounding the CC-terminal [35], [13] requires the driver to operate with higher ($>$ 1 V) VDD supplies, resulting in increased power consumption. Alternatively, biasing the CC terminal at a negative voltage [11], [14], [15], [36] enables the driver to operate with nominal ($<$ 1 V) VDD supplies while maintaining sufficient modulation swing. Compared to current-mode differential drivers [37], [38], single-ended voltage-mode drivers [9], [14], [15] are energy-efficient, but prone to dc-wander at the internal nodes and supply switching noise. Therefore, challenges arise for simple CMOS inverters with higher output impedance and limited BW to drive the VCSELs effectively at higher data rates. Hecht et al. [9] used a switch-based voltage-mode driver with limited tunability, but its high nonlinearity makes it unsuitable for CTLE-based equalization and group-delay compensation. Kozlov et al. [39] proposed AC-coupled drivers to suppress DC wander, but at the expense of large series capacitors and area overhead. Mansuri et al. [11] proposed a voltage-mode driver with active shunt feedback, but the BW extension is limited, considering large ESD and pad capacitances. Mondal et al. [14], [15] improved the output swing over [11], but at the cost of tight stability margins and an extra zero for group-delay compensation. In this work, a single-ended inverter-based output driver based on [11] is implemented, featuring shunt-series peaking inductors with tunable Q-factor. Compared to output drivers with inductive shunt feedback [29], [40], the shunt-series peaking provides greater BW extension for a single-ended inverter-based output stage [27]. A detailed overview of the final output stage is shown in Fig. 13(a) with a linearized equivalent circuit presented in Fig. 13(b). A PMOS-based switchable cascode current source is used to bias the VCSEL. The current source is adjustable up to a maximum of 10 mA using a 4-bit digital control word. To reduce the output impedance and maintain the dc-bias of the output node at mid-VDD, an inverter-based low-impedance load ($1/gm_{d2}$) is attached to the driver output with a transconductance of gm_{d1}. Without the shunt-series peaking inductors, the linearized gain of the driver at low frequency can be derived as, $-gm_{d1}/gm_{d2}$ with a dominant pole at the output, $\omega_p = gm_{d2}/(C_d + C_l)$, where C_l comprises the total parasitic capacitances with output PAD, ESD diode and biasing MOS and C_d is the total driver-side capacitance at the drain terminal. With increased gm_{d2}, the BW can be extended further, but at the expense of reduced low frequency gain. A shunt inductor (L_1) with tunable Q-factor is used to mitigate the BW limitation due to the combined capacitance, $C_d + C_l$. In this case, the bridged-shunt peaking is suboptimal as the additional bridge capacitance increases parasitic capacitance at the output node, resulting in reduced BW [31]. Considering only the shunt inductor (L_1), the transfer function of the driver, $H_d(s)$ normalized to its low frequency gain can be approximated as,

$$H_d(s) \approx \frac{1 + sgm_{d2}L_1}{1 + s(C_d + C_l)/gm_{d2} + s^2L_1(C_d + C_l)} \quad (5)$$

The LHP zero, i.e, $\omega_{z1} = 1/gm_{drv,2}L_1$ with the CCP pairs in Eq. 5 helps to improve BW up to 1.8 times. The Q-factor of the parallel resonance tank with inductor L_1, i.e, $Q = gm_{d2}\sqrt{L_1/(C_d + C_l)}$, can be tuned independently by gm_{d2}, providing an extra degree of freedom to adjust peaking and group delay variation at the output. However, with C_{gd}, i.e, the capacitance between the gate and drain terminal of the devices from gm_{d1} transconductor-cell into consideration, a right-half-plane zero, i.e, $\omega_{z2} = gm_{drv,1}/C_{gd}$ is created. ω_{z2} tends to diminish the effective BW extension [30]. The additional series inductor L_2 in combination with L_1 creates a shunt-series peaking [30], [31] to mitigate the issue, offering higher BW extension more than 3 times. Intuitively, it can be explained that L_2 splits the capacitances C_d and C_l, thereby delaying the current through C_l, resulting in higher BW with faster transitions, but at the expense of increased latency.

The post-layout simulated voltage gain responses of the output driver are compared for different BW extension techniques at the top of Fig. 14. Without inductive peaking, the driver exhibits a BW of 23 GHz. Incorporating the shunt inductor L_1 extends the BW by 1.8 times, while the series inductor L_2 achieves a 2.4 times improvement. The proposed combined shunt–series inductive peaking technique further enhances the BW by up to 3 times, reaching 56 GHz. The trasconductors, gm_{d1} and gm_{d2} as shown in Fig. 13 are digitally programmable using 3-bit binary control-words drvren_1[2:0] and drvren_2[2:0] respectively. The post-layout simulated voltage gain responses of the output driver circuit for different settings of the transconductances (gm_{d1} and gm_{d2}) are shown at the bottom of Fig. 14. The green, blue, and red traces correspond to the maximum, medium, and minimum gm_{d1} values, while

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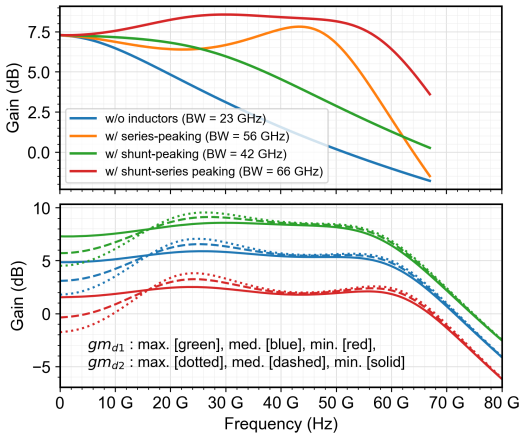


Fig. 14. Post-layout simulated voltage gain responses of the output driver for various bandwidth extension techniques (top) and different settings for transconductances gm_{d1}, gm_{d2} (bottom).

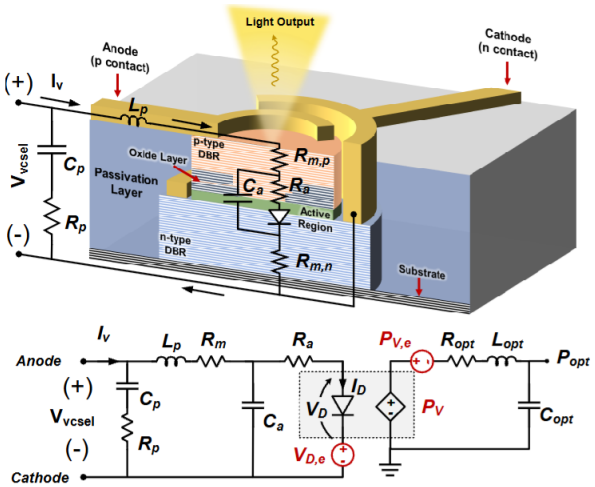


Fig. 15. The VCSEL circuit-equivalent model depicting the lumped elements.

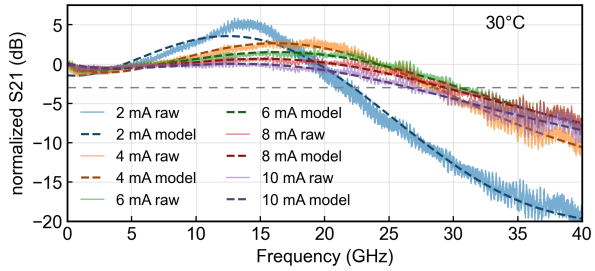


Fig. 16. Measured S_{21} vs fitted model response of the VCSEL model.

the solid, dashed, and dotted lines represent the minimum, medium, and maximum gm_{d2} settings, respectively.

IV. VCSEL Device Model and Co-Simulation

Accurate VCSEL device models are needed to co-design and optimize the driver circuits, considering the VCSEL bias-dependent electrical and electro-optical response and the thermal impact on device characteristics. The poor heat dissipation from resistive distributed Bragg reflectors (DBRs) raises the VCSEL's active region temperature. VCSEL self-heating raises the threshold current, reduces BW, and saturates the output power. As illustrated in Fig. 15, we present a VerilogA circuit-level model of VCSEL devices with proposed self-heating-induced error voltage ($V_{D,e}$) and optical power ($P_{D,e}$) components. Early circuit-level VCSEL models utilized hybrid rate equations [41], [42] or bias-dependent optical equivalent components [43] to capture non-linear dynamics, though often at the expense of neglecting thermal effects. While subsequent models introduced interdependent sub-circuits to address this [44], [45], the resulting complexity hinders intuitive device-circuit co-design. Mondal et. al. [15] developed the model and accounted for the thermal variation using the junction temperature as a function of ambient temperature, bias and thermal time constant. However, traditional thermal modeling relies on indirect thermal resistance measurements [46], [47], which fail to capture complex geometrical and electro-opto-thermal interactions, particularly in case of arrays [48]. Conversely, our model accounts for self-heating induced variations in device voltage ($V_{D,e}$) and optical power ($P_{D,e}$) using numerically fitted parameters based on higher-order polynomial functions of temperature and bias current. Compatible with SPICE-level simulators, this approach enables driver and VCSEL co-simulations with various temperatures and bias conditions. As shown in Fig. 15, the electrical n- and p-type contacts and DBR resistances form R_m in series with the active region. R_a is the junction resistance in series with a Shockley diode to model static I-V characteristics. C_a includes oxide capacitance, junction capacitance, and intrinsic layer capacitance. For a bias current of I_D, the small-signal resistance of the diode is $R_d(= nkT/qI_D)$. The model also incorporates the input parasitics containing the pad capacitance (C_p), leakage resistance (R_p), and series inductance (L_p). The device voltage (V_{vcsel}) can then be expressed as $V_{vcsel} = I_D(R_m + R_a) + nkT/q \times ln\,(I_D/I_{sat} + 1) + V_{D,e}$ where $V_{D,e}$ is the self-heating induced error voltage variation. In addition to the electrical input circuit, there is an equivalent electrical circuit showcasing the 2^{nd} order electro-optical response. This is composed of optical equivalent components R_{opt}, L_{opt}, and C_{opt} [43] and the optical power output, P_{opt}, is modeled as the output node voltage across C_{opt}. $P_V = \eta(I_D - I_{th})$ is a dependent voltage source where η is the slope efficiency of the electro-optical power conversion and I_{th} is the threshold current. $P_{V,e}$ is the self-heating induced error component which in series with P_V accounts for the total optical power P_{opt}. The VCSEL transfer function, $H_v(s)$ from the voltage $P_{V,Total}(= P_V + P_{V,e})$ to the output P_{opt} can be expressed as, $H_v(s) = 1/(1 + sR_{opt}C_{opt} + s^2L_{opt}C_{opt})$. The electrical model parameter (R_m, R_a, C_a, L_p, C_p and R_p) and the optical equivalent $R_{opt}, L_{opt}, C_{opt}$ components are fitted using the s-parameter responses using nonlinear polynomial function of I_D with temperature (T)-dependent coefficients such as $f(I_D, T) = \sum_{i=0}^{2}(\sum_{j=0}^{3} a_{ij}T^j)I_D^i$. The EO device parameters (n, I_{sat}, η, I_{th}) and the self-heating induced error in voltage and optical power components $V_{D,e}$ and $P_{V,e}$ are numerically fitted using the device's P-I-V responses as polynomial function of I_D with temperature (T)-dependent

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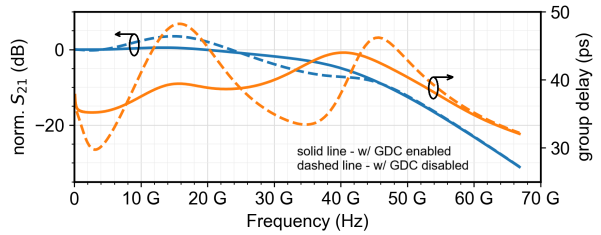


Fig. 17. Post-layout EO co-simulated responses (normalized S_{21} and group delay) of the driver with the VCSEL model.

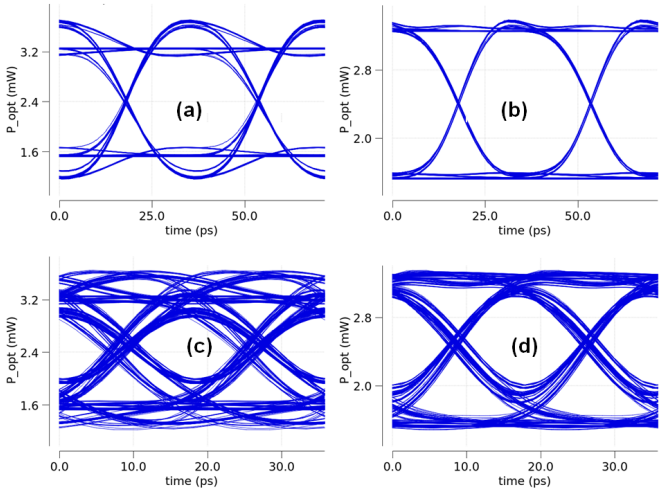


Fig. 18. Post-layout EO eye diagrams of the driver co-simulated with the Verilog-A VCSEL model: (a) GDC disabled at 28 Gbaud, (b) GDC enabled at 28 Gbaud, (c) GDC disabled at 56 Gbaud, and (d) GDC enabled at 56 Gbaud.

coefficients. Fig. 16 compared the measured S_{21} against fitted model response of the VCSEL model. Fig. 17 shows the post-layout EO co-simulated response of the CMOS driver combined with the VCSEL model with a -3 dB BW of 21 GHz. The normalized S_{21} response (left axis) indicates that GDC-enabled operation introduces a passband droop that suppresses VCSEL peaking, producing a flatter EO response. The simulated group-delay response (right axis) further shows that the GDC significantly reduces the large in-band delay variation present without compensation. Fig. 18 shows post-layout EO eye diagrams of the driver co-simulated with the VCSEL model at 28 and 56 Gbaud, with and without the GDC. At 28 Gbaud, the uncompensated case in Fig. 18(a) exhibits overshoot and noticeable eye closure, whereas enabling the GDC (see Fig. 18(b)) flattens the response and yields a cleaner, more open eye. At 56 Gbaud, the eye without GDC as shown in Fig. 18(c) is strongly degraded by inter-symbol-interference, while the compensated case (see Fig. 18(d)) recovers a significantly larger vertical and horizontal opening, demonstrating the effectiveness of the proposed solution at high data rates.

V. Experimental Setup and Results

The 4-channel driver prototype is fabricated in a 28 nm bulk CMOS technology. The total driver IC, including the

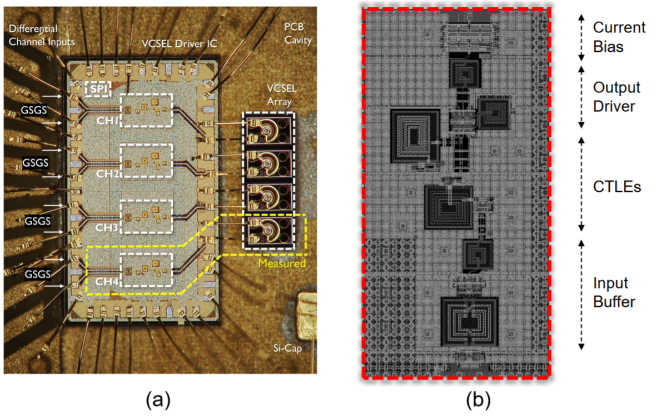


Fig. 19. (a) Overview of optical Tx assembly: VCSEL driver interfaced with 1060 nm VCSEL array, and (b) enlarged layout single channel of the driver.

pad, occupies an area of approximately 2.2 mm^2 (1.95 mm $\times$ 1.125 mm), and the per-channel core area occupies around 0.14 mm^2 (0.7 mm $\times$ 0.2 mm). The driver IC input signal pads follow a GSG configuration with 100 μm pitch. The output signal pads feature a pitch of 125 μm to match the VCSEL array, and the pads between the output signal pads provide the negative voltage bias to the CC terminal. An overview of the optical Tx assembly, including the driver IC wirebonded to the VCSEL array, is shown in Fig. 19(a). An enlarged view of the channel layout with corresponding circuit blocks is shown in Fig. 19(b).

A. VCSEL Device Characterization

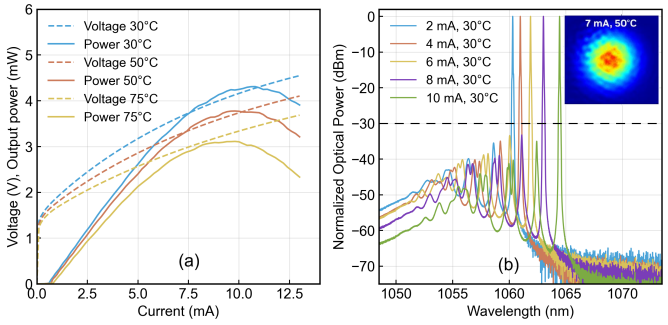


Fig. 20. (a) VCSEL static P-I-V characteristics for different temperatures, (b) optical spectra for different bias currents.

The static P-I-V characteristics of the co-designed GaAs-based 1060 nm VCSEL were characterized at 30°C, 50°C, and 75°C, as illustrated in Fig. 20(a). The device exhibits a threshold current of 0.63 mA and a slope efficiency of 0.58 W/A at 30°C. As the temperature increases, the optical output power gradually decreases, with a thermal roll-over due to self-heating initiating around 10 mA current bias. With a 6 mA current bias at 30°C, the VCSEL delivers an optical output power of 3 mW with a forward voltage of 3.2 V, demonstrating a stable SM operation. The modulation response of the VCSEL was measured at 30°C for bias currents ranging from 2 mA to 10 mA with increments of 2 mA, and the normalized S_{21}-responses are shown in Fig. 16. The

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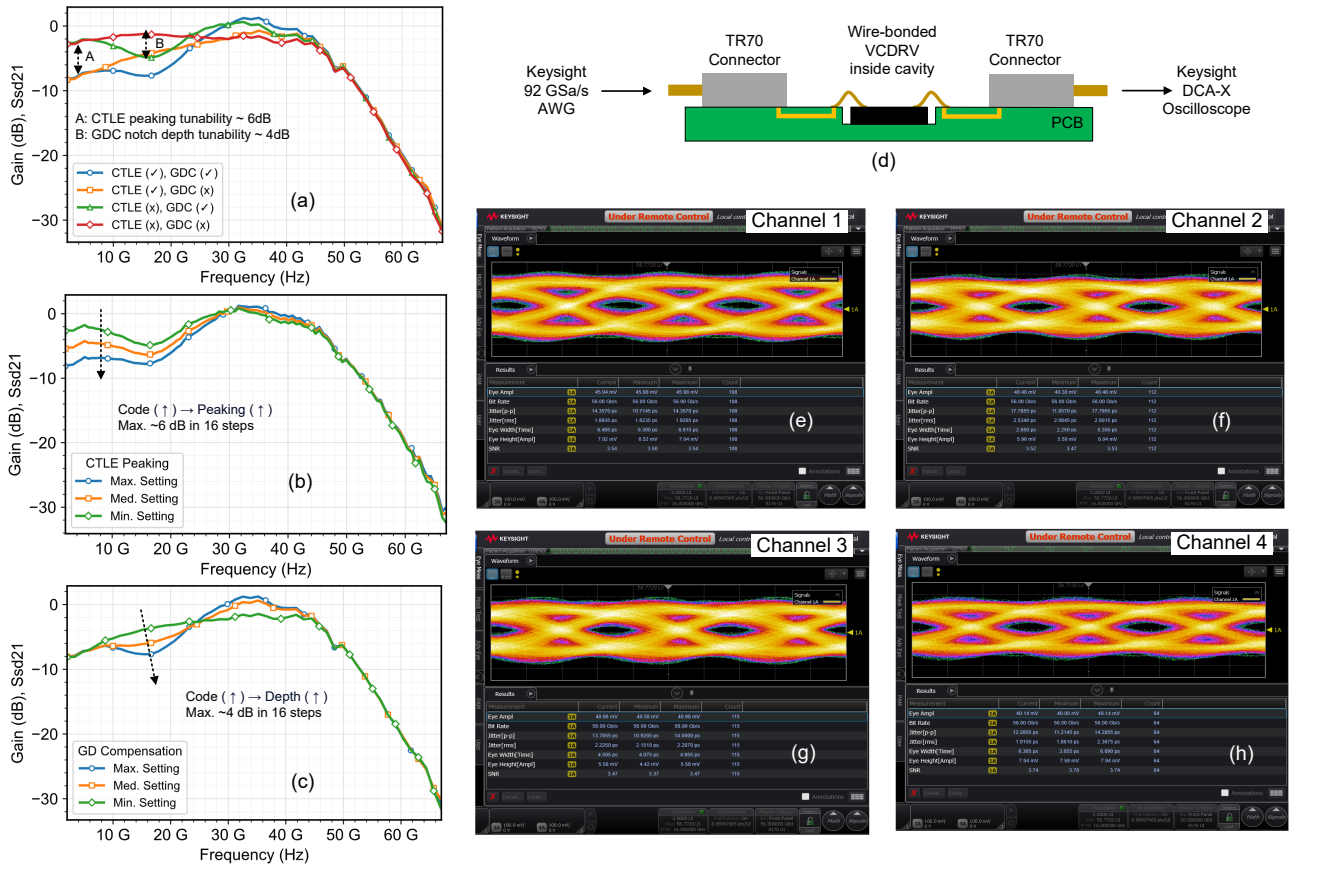


Fig. 21. (a) Electrical S_{21}-response of the driver measured using RF-probes; (b)-(c) Digitally tuned CTLE peaking and GDC notch-depth set at maximum, medium, and minimum settings respectively; (d) Measurement setup for electrical time-domain experiment; (e)-(h) 56 Gbaud NRZ electrical eye diagrams for all 4 channels respectively.

-3 dB modulation BW of the device increases with bias current, reaching a maximum of 31 GHz at 6 mA. At low bias currents, the VCSEL exhibits an underdamped response with increased peaking, which increases up to 5 dB at a current bias of 2 mA. The modulation response flattens as the bias current increases, reflecting improved damping and BW extension. The corresponding measured normalized optical spectra from the device are shown in Fig. 20(b). It reveals a stable wavelength across all bias conditions. Under a 7 mA current bias, the VCSEL achieves an optical power of 5.1 dBm with a side-mode suppression ratio exceeding 30 dB, and a beam divergence of approximately 18°, confirming high-quality SM emission suitable for MR transmission over single-mode fiber (SMF).

B. Electrical Driver Characterization

For electrical frequency-domain characterization, the driver die was mounted on a printed-circuit-board (PCB) with bond-wire connections providing the supplies and interface for SPI communication. The assembled driver was evaluated on an RF probing station, where a GSGSG probe contacted the differential input pads of a single channel and a GSG probe accessed the corresponding single-ended output. Three-port mixed-mode S-parameters were measured using a Keysight PNA-X N5247B vector network analyzer, and the input port power during the S-parameter measurement was maintained below -0.5 dBm, corresponding to an input swing of approximately 600 mV peak-to-peak, to ensure operation within the expected signal range. The measured S_{21} responses of the driver under various CTLE and GDC configuration settings are shown in Fig. 21(a). As illustrated, both the CTLE peaking amplitude and the GDC-induced notch-depth can be digitally adjusted through SPI register settings. For maximum-gain operation with the CTLE and GDC disabled, the driver exhibits a BW of approximately 48 GHz (see red curve, Fig. 21(a)). Enabling the two-stage CTLE increases the overall peaking up to 6 dB (see yellow line, Fig. 21(a)), thereby extending the electrical BW to approximately 55 GHz. The GDC introduces a notch in the pass-band near 17 GHz, with a depth tunable up to 4 dB. The programmability of the CTLE's low frequency gain and the GDC compensation, each controlled by a 4-bit digital word, is illustrated in Fig. 21(b) and (c), respectively, for maximum, medium, and minimum settings.

For electrical time-domain characterization, the driver die was mounted on a six-layer PCB fabricated using low-loss MEGTRON-6 dielectric material with impedance-controlled high-speed differential traces. The die was placed in a bottom-plated cavity etched into the PCB, and the pads were wire-bonded to the corresponding PCB traces, as illustrated in Fig. 21(d). Multicoax TR70 connectors with RF cables were

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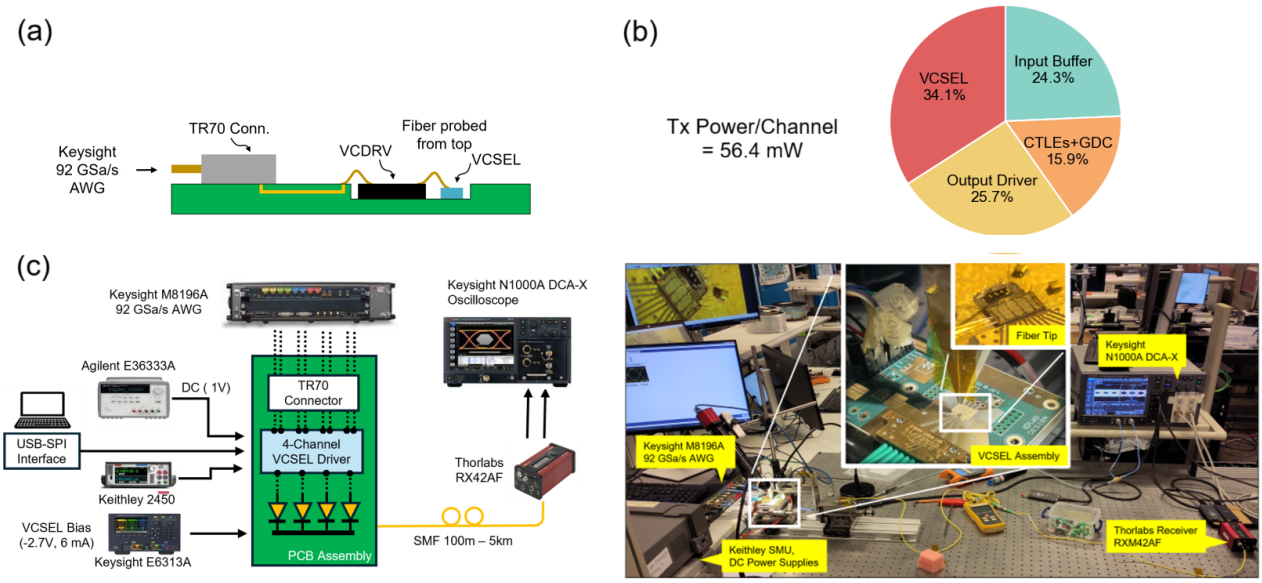


Fig. 22. (a) VCSEL–driver assembly on PCB, (b) power consumption breakdown for each block in a TX channel, and (c) measurement setup for the electro-optical transmission experiment with a photo of the lab configuration.

used to interface the driver to a Keysight 92 GSa/s arbitrary waveform generator (AWG) at the electrical input and a Keysight DCA-X oscilloscope at the output for signal capture and analysis. During the electrical time-domain experiment, PRBS11 test patterns at 56 Gbaud were used to evaluate the high-speed performance of the driver. The resulting NRZ eye diagrams for all 4 channels measured individually are shown in Figs. 21(e)–(h), demonstrating consistent eye opening and channel-to-channel uniformity. Notably, no external DSP or link loss de-embedding was applied during the measurement, and the captured results reflect the raw output performance of the driver. Only the on-chip CTLE-based pre-emphasis was used to compensate for the total electrical link loss (RF cables, TR70 connectors, and PCB traces) over 6 dB at the Nyquist frequency of 28 GHz. These results confirm that the on-chip CTLE block effectively compensates for high frequency attenuation, enabling efficient NRZ signaling at 56 Gbaud without additional post-processing.

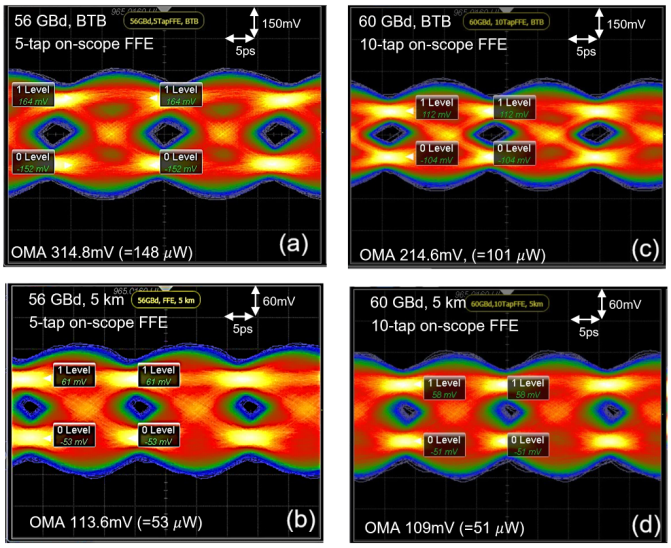


Fig. 23. Electro-optical NRZ eye diagrams for 56 GBd over (a) BTB, (b) 5 km SMF, and 60 GBd over (c) BTB, (d) 5 km SMF.

C. Electro-Optical Transmission Measurement

For the EO transmission experiments, the driver was co-integrated with the VCSEL array within a bottom-plated PCB cavity, as illustrated in Fig. 22(a). The driver dies were thinned to 250 μm to align with the height of the VCSEL array and subsequently wire-bonded to both the PCB traces and the corresponding VCSEL terminals to ensure short, low-inductance electrical interconnection. The 1060 nm VCSEL optical emission was probed using a fiber from the top with an angle optimized to reduce back-reflections. Fig. 22(b) illustrates the power consumption breakdown across the major building blocks of a single Tx channel, including VCSEL. The complete experimental setup is illustrated in Fig. 22(c). During characterizations, a 92 GSa/s AWG from Keysight generated a PRBS15 test pattern, which was delivered through 2.5 inch multicoax TR70 connectors to the driver's differential inputs. The driver operated from a single supply of 1 V, while a single VCSEL was biased at 6 mA via an on-chip current source, with –2.7 V applied at the CC terminal. The 1060 nm VCSEL's optical emission was first coupled into a lensed fiber (SM at 1060 nm [49]) and then propagated over 5 km standard SMF. Although standard SMF (G.652) at 1060 nm may weakly support higher-order modes [50], their excitation depends on the launch conditions (lateral offset, angular tilt, axial spacing, etc.).The truly SM lensed fiber was used to provide controlled input field to minimize coupling into higher-order modes. An optical receiver from Thorlabs (RX42AF), featuring a responsivity of 0.425 A/W with a 39 GHz BW and noise-

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TABLE I
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART VCSEL DRIVERS.

	OFC'24[51]	ECOC'23[52]	OFC'24[53]	OFC'23[9]	JSSCC'25[14]	This work
VCSEL Wavelength	1060 nm	1060 nm	1060 nm	850 nm	850 nm	**1060 nm**
Integrated Driver Technology	no driver	no driver	with driver	22 nm FDSOI	22nm FinFet	**28nm CMOS**
VCSEL Bandwidth, Current Bias	35 GHz, 10 mA	27 GHz, 8 mA	30 GHz, 8 mA	28 GHz, 6 mA	26 GHz, 9 mA	**31 GHz, 6 mA**
Baud-rate, Modulation Format	60 GBd, NRZ	45 GBd, NRZ	53.125 GBd, PAM4	56 GBd, NRZ	64 GBd, NRZ	**60 GBd, NRZ**
Fiber Length	2 km	10 km	2 km	100m	BTB	**5 km**
On-scope Equalization	5-tap FFE	5-tap FFE	20-tap FFE	No FFE	No FFE	**10-tap FFE**
Optical Transmitter† Energy Efficiency	-	-	5 pJ/b (*full link)	-	1.3 pJ/b	**0.94 pJ/b**
Optical Driver Energy Efficiency	-	-	-	0.4 pJ/b	0.66 pJ/b	**0.62 pJ/b**
Bitrate-Distance Product (*FEC-corrected)	113.4 Gb/s.km	425.2 Gb/s.km	200.8 Gb/s.km	-	-	**283.47 Gb/s.km**

† Total power consumption of VCSEL and Driver considered.

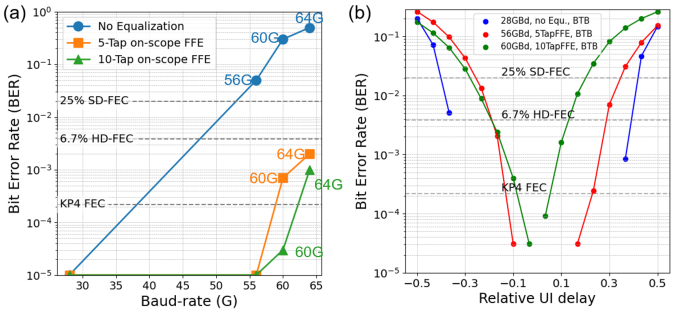


Fig. 24. (a)BER vs. baud-rate for 5 km SMF with different FFE configurations and (b) horizontal bathtub curves for 28, 56, and 60 GBd BTB links.

equivalent power of 23 $pW/\sqrt{Hz}$ was used to receive the optical signals. The receiver, providing a gain of 2125 V/W at 1060 nm, converted the optical signals to electrical signal waveforms for capture and visualization using the DCA-X oscilloscope from Keysight. The BER was measured during post-processing by counting erroneous bits from transmitted 2^{15} bit sequences targeting a KP4-FEC BER threshold of 2.2e-4 with 95% confidence level. During the measurements, the driver, operating with a supply of 1 V, with a 31 GHz 1060 nm VCSEL biased with 6 mA current (cathode at -2.7 V), achieves a Tx energy efficiency of 0.94 pJ/b. The 1060 nm VCSEL-based optical Tx achieved error-free NRZ transmission with BER $<$ 1e-12 up to 60 Gbaud over 5 km SMF after FEC. The eye diagrams in Figs. 23(a) and (c) show back-to-back (BTB) NRZ transmission at 56 Gbaud and 60 Gbaud, using on-scope FFEs with 5 and 10 taps, respectively. For BTB experiment, the Tx achieved optical modulation amplitudes (OMAs) of 148 μW and 101 μW, respectively. After transmission over 5 km SMF, as shown in Figs. 23(b) and (d), fiber loss and dispersion reduced the OMA to 53 μW at 56 Gbaud and 51 μW at 60 Gbaud. The measured TDEC (NRZ) for 56 GBd and 60 GBd transmission over 5 km SMF were 1.93 dB and 3.58 dB, respectively. Fig. 24(a) indicates that 60 GBd NRZ transmission could meet the KP4-FEC threshold with a 10-tap FFE, while 56 GBd requires only a 5-tap FFE. The horizontal bathtub curves for BTB NRZ transmission at 28, 56, and 60 GBd are illustrated in Fig. 24(b).

D. Comparison With State-of-the-Art

The performance of the proposed optical Tx is compared against driver-less 1060 nm VCSEL demonstrations [51], [52] and also with state-of-the-art VCSEL drivers [53], [9], [14] in Tab. I. The driverless 1060 nm VCSEL reported in [52] achieved a FEC-corrected bitrate-distance product of 425.2 Gb/s.km, but the demonstration lacked a driver, PCB, RF connectors, and used shorter PRBS9 bit patterns. In contrast, the VCSEL-based optical Tx presented in this work, incorporates an integrated CMOS-based driver, employs a longer PRBS15 bit patterns and demonstrates the record high FEC-corrected [17] bitrate-distance product of 283.47 Gb/s.km among 1060 nm VCSELs with integrated drivers. Furthermore, compared to the 1060 nm VCSEL driver implemented in the work [53] using 20-tap FFE, our optical Tx attains a higher bitrate-distance product with only 10-tap FFE, demonstrating improved BW and energy efficiency with reduced equalization complexity.

VI. CONCLUSION

This article presents five primary contributions. First, it details the development of an energy-efficient direct-drive optical Tx utilizing a CC-type SM 1060 nm VCSEL specifically co-designed for medium-reach transmission (up to 5 km) for LPO-based inter-cluster DCI. Second, it discusses several CMOS-inverter-based BW enhancement techniques used in the 28 nm CMOS driver. These include a transformed-coupled input buffer, an additive CTLE with active inductors, and a T-coil-coupled resistive feedback CTLE. Third, it has introduced the proposed GDC circuit to equalize the low-bias underdamped VCSEL response. Fourth, a compact SPICE-compatible VerilogA-based circuit-level VCSEL device model featuring self-heating is proposed to co-design and (co-)optimize the optical Tx interface. Fifth, the optical Tx using a SM 1060 nm VCSEL, featuring 31 GHz BW, demonstrated 60 Gbaud NRZ transmission over 5 km of SMF enabled by on-chip pre-emphasis and a 10-tap on-scope FFE with an estimated BER $<$ 1e-12 after FEC. Furthermore,

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the optical Tx achieved a record-high FEC-corrected bitrate-distance product of 283.47 Gb/s.km and a Tx energy efficiency of 0.94 pJ/b among integrated drivers using 1060 nm VCSEL-based optical communication links.

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