Atomic Hydrogen Exposure to Enable High-Quality Low-Temperature SiO_2 with Excellent pMOS NBTI Reliability Compatible with 3D Sequential Tier Stacking

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***Abstract*—Fabrication of stacked CMOS tiers in a 3D sequential integration requires development of low thermal budget process modules. High-quality SiO_2 interfacial layer (IL), obtained up to now only by high-temperature (≥850°C) oxidation or exposure, is crucial for pMOS NBTI reliability. In unannealed IL's grown at reduced temperatures, we show that unrelaxed interface strain induces high defect densities, with physics-based NBTI modeling suggesting excessive hydroxyl-*E'* defect formation due to Si-O bond stretch. Based on *ab-initio* theoretical insights, we demonstrate an atomic hydrogen treatment to passivate SiO_2 defects at low temperatures (100-300°C), which is shown to be vastly more effective than high pressure molecular hydrogen exposure, and to yield an SiO_2 quality and reliability surpassing a 900°C oxide.**

Introduction

Stacking of transistor tiers in a 3D sequential integration flow was recently demonstrated (e.g., [1]) as a promising approach to continue increasing CMOS functionality per die area. New development of process modules at reduced thermal budget is crucial to maintain the functionality of the lower tiers. Gate stack reliability is extremely sensitive to fabrication temperature: we have recently shown that omitting the standard high-temperature 'reliability anneal' (~900°C) results in very poor NBTI (**Fig. 1**) and PBTI reliability of a RMG HKMG stack. In [2] we demonstrated sufficient nMOS reliability at low thermal budget by inserting dipole-forming layers at the SiO_2-HfO_2 interface to induce a more favorable line-up between the HfO_2 and Si band edges resulting in less charge trapping. Such approach is useful also for pMOS NBTI only if the SiO_2 IL is aggressively scaled (<0.7nm). In contrast, for a 1~1.2 nm IL–still of relevance for state-of-the-art technology–excessive hole trapping in the low temperature SiO_2 represents the limiting factor for NBTI reliability [2]. In [3] we have shown that post-metal anneals at reduced temperature (<600°C) can reduce the charging trap density in HfO_2; however, the same approach is ineffective for SiO_2 hole traps (**Fig. 2**).

In this work we demonstrate a solution for low thermal budget NBTI reliability with a standard thermal SiO_2 IL (Fig. 1). By comparing the experimental properties of the hole traps with *ab-initio* calculations, we confirm the most probable microscopic defect structures to be hydroxyl-*E'* centers and possibly hydrogen bridges [4,5]. We find that defect formation is strongly dependent on the (*last*) Si oxidation temperature [6] and ascribe this dependence to residual interface strain at low temperatures [7,8]. Based on theoretical insights [9,10], we demonstrate a low temperature (100-300°C) atomic hydrogen treatment which efficiently passivates emerging oxide defects and makes the SiO_2 quality comparable or superior to a 900°C (grown or exposed) oxide, in terms of minimized positive charge and excellent reliability. We also demonstrate that a more conventional exposure of the IL to molecular hydrogen, even at high pressure and temperature (20 atm, 450°C), yields only marginal improvements, highlighting the importance of developing specific treatments to enable low thermal budget gate stacks.

Experimental

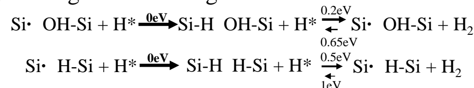
MOS capacitors were fabricated on a 300mm test vehicle in an RMG flow. Three different thermal SiO_2 IL's (~1.2nm) grown at 600/700/900°C by ISSG or RTO processes were considered. Treatments were performed on the IL right after formation. The gate stack was completed in all cases by depositing ~1.8nm HfO_2 and 5nm TiN by ALD. Unless noted otherwise, a final sintering (400°C-20' in molecular H_2) was performed to passivate the Si/SiO_2 interface. For reference, one stack comprised a chemical oxide IL (~0.7nm) and another stack (w/ a 700°C IL) was exposed to a 'reliability anneal' (850°C-1.5" in He, after deposition of a sacrificial TiN/*a*-Si gate). In selected cases, after formation the IL was exposed to atomic hydrogen generated in a remote plasma, or to H_2 (20 atm) and/or to O_2 (1 or 20 atm), as discussed in the next section. EOT and effective work function (eWF) were estimated from *C-V* curves measured on capacitor test structures with the CVC Hauser tool [11]. NBTI was studied by stress/recovery sequences [12] (minimum sense delay ~10ms; stress times up to 1ks) at increasing stress $E_{ox}\approx(V_g-V_{fb0})/(\text{EOT}+0.4\text{nm})$ at 25°C (to sense mainly the hole trapping component) and at 125°C (to sense also the D_{it} generation component). Degradation was benchmarked as the induced effective charge sheet density $\Delta N_{eff}\equiv\Delta V_{fb}*C_{ox}/q$. An additional set of NBTI stresses up to 20ks was performed at 125°C, periodically interrupted to measure the *C-f-V* response [13] to directly monitor D_{it} generation from *C-V* stretch out correction or from the parallel conductance peak in depletion.

Results and Discussion

The so-called 'reliability anneal' (~900°C) is a crucial step in RMG HKMG gate stack fabrication, but it is not compatible with stacked top tier fabrication. Omitting this post-metal anneal results in poor (PBTI [2] and) NBTI reliability with induced V_{th} shifts ~10× larger compared to a Foundry 28 nm ref. process (**Fig. 1**). We used the imec/T.U. Wien BTI modeling framework Comphy [14] to estimate the hole trap energy levels within the SiO_2 bandgap, and to compare with *ab-initio* calculations of the charge transition levels of known SiO_2 defect structures [4] (**Fig. 2**). The often-invoked oxygen vacancies show too deep charge transition levels to be of relevance for the NBTI reliability of low voltage Logic technologies. In contrast, the hydroxyl-*E'* and hydrogen bridge structures (Fig. 2b-c) are expected to have charge transition levels in the vicinity of Si E_v and are therefore compatible with our experimental NBTI signature. In particular, the hydroxyl-*E'* tends to form in the presence of stretched Si-O bonds [10]. To investigate the role of oxidation temperature on the hole trap formation, we compare the NBTI reliability of stacks with various IL's (**Fig. 3**): a strong dependence is observed, with the IL grown at the highest temperature (900°C) showing the best reliability. Note that performing an 850°C post-metal 'reliability anneal' yields a trap density as low as the one measured on a 900°C IL, suggesting a key role of the *last* oxidation temperature [6]. The dependence of the hole trap density on the oxidation temperature matches well the stretched Si-O FTIR signal reported in [7] (**Fig. 4**). These initial observations suggest the qualitative model depicted in **Fig. 5**: a reduced oxidation temperature does not allow for a complete relaxation of strain at the Si/SiO_2 interface, resulting in a larger presence of stretched Si-O bonds, which are precursors for hydroxyl-*E'* formation. As a consequence, the hole trap and fixed positive charge densities depend on the oxidation temperature (Fig. 5b), where the hole trap band tail reaching above Si E_v is perceived as additional fixed charge, as it would be positively charged already at flat-band [6]. While *formation of these defects is an unavoidable consequence of thermodynamics,* we demonstrate that *this specific type of hole traps can be passivated after IL formation at low temperature by proper hydrogen treatments*.

The hydroxyl-*E'* was suggested as an NBTI-inducing defect already in 1995 [5], and has been recently extensively studied in the context

of RTN/NBTI kinetics models: as depicted in **Fig. 6**, it manifests itself in the stable and meta-stable neutral and positive configurations necessary to explain hole trapping kinetics. Interestingly, it has been suggested in [15] that the so-called 'anomalous RTN' phenomenon (i.e., an active trap which suddenly stops producing an RTN signal) might be explained by '*defect volatility*', due to coincidental interaction between the defect and hydrogen species present in the gate stack. Based on this insight, we envisioned the possibility of preferentially inducing defect volatility during the fabrication process, by directly exposing the IL to hydrogen. Density-functional theory calculations [10] suggest that exposure to atomic hydrogen can yield spontaneous passivation of the Si-dangling bond at the hydroxyl-*E'* and hydrogen bridges sites through the reactions:



Alternatively, removal of the sticking hydrogen (over a thermal barrier) by dimerization and H_2 molecule release, could also de-activate the defects: the hydroxyl-*E'* would tend to reform a correct Si-O-Si bond (see Fig. 6 left), while the hydrogen bridge (**Fig. 7**) would transform into an oxygen vacancy not contributing to NBTI (cf. Fig. 2b). Note that: i) hydrogen species might also activate defects at precursor sites, and therefore properly controlling the exposure conditions to favorably skew the reaction balance is crucial, ii) similar passivating reactions could be induced also by exposure to molecular hydrogen, though over sizeable energy barriers. Consistently, we could only achieve marginal 2-3× NBTI improvement when exposing a 600°C IL to molecular hydrogen for up to 2h at 450°C, despite resorting to 20atm pressure to maximize H_2 availability (**Fig. 8**).

We therefore designed a remote hydrogen plasma process (**Fig. 9**) to expose the IL to hydrogen radicals (H*). As suggested by theory, this results in a very effective passivation of the hole traps (**Fig. 10**): a dramatic NBTI improvement is observed (~2-20× for 10"-10' exposures at 100°C , and ~7-100× at 300°C) due to the suppression of the hole trap density down to or below the level of a 900°C ref. IL. By comparing the trap density reduction factors observed for the different exposures, an effective thermal barrier of 0.21±0.06eV is estimated for the beneficial reaction(s) taking place at the defect sites (**Fig. 11**). We note that the short H* exposures do not result in any EOT increase, while a marginal increase of 1-1.5Å is observed for the 10' exposures at 100-300°C; in contrast, a gradual increase of the eWF is consistently observed for all the H* exposures (**Fig. 12**), suggesting concurrent suppression of both hole traps and positive oxide charge (cf. Fig. 5b). Moreover, the H* exposures results in reduced gate leakage (**Fig. 13**) and improved breakdown robustness (**Fig. 14**).

Performing an additional anneal in oxygen (450°C-0.5h 1atm O_2) after exposing the 600°C IL to H* results again in very poor NBTI reliability (**Fig. 15**). This suggests that additional oxidation of the Si surface (now at 450°C, instead of the original 600°C oxidation) increases again the near-interface defect density. To prove the reversibility of the defect formation/passivation with H* processes, we first expose the 600°C IL to a high-pressure oxygen anneal (450°C-0.5h 20atm O_2) which induces ~2Å oxide regrowth: this procedure yields the worst NBTI reliability, which is nevertheless improved again by subsequent H* exposure (**Fig. 16**). Conversely, even a high-quality 900°C IL is further improved by H* (**Fig. 17**), suggesting this treatment can be beneficial (although not strictly necessary) also in a standard high thermal budget fabrication flow.

Across all the IL growth/treatment combinations studied, a remarkable correlation between the NBTI reliability and the eWF is consistently observed (**Fig. 18**), as postulated by our initial qualitative model (cf. Fig. 5): the IL's grown at the lowest T (450°C) show the lowest maximum-allowed V_{ov} for sufficient NBTI reliability (~0.2V) and also the lowest eWF (~4.73eV despite the use of a high WF TiN gate); increasing the oxidation temperature or exposing the stack to a 'reliability anneal' enhances both the max V_{ov} and the eWF; similarly, both the H_2 and H* treatments (the latter most effectively) enhance the max V_{ov} up to 1.8V and eWF up to 5.04eV along the same trend.

A possible detrimental effect of H* exposure is the de-passivation of Si-H bonds at the interface [16]. However, this is readily solved by performing a standard sintering anneal (400°C-20' H_2) at the end of the RMG flow. Omitting the latter after H* exposure of the IL (**Fig. 19**) results indeed in poor interface passivation (D_{it0}~2×10^{11} /cm^2/eV), and in a less improved NBTI reliability. To investigate interface stability, additional NBTI stresses were performed at elevated temperature (125°C), and D_{it} generation was monitored by the parallel conductance in depletion. **Fig. 20** reports the D_{it} generation kinetics measured at accelerated stress conditions (E_{ox}=5.7MV/cm) in selected stacks. In all cases, similar time-dependences are observed: HP H_2 or H* exposure of the 600°C IL results in improved interface stability, comparable to a 700°C IL, although not as good as 900°C or 850°C-exposed IL's. The field-acceleration of the D_{it} generation for various gate stack configurations is reported in **Fig. 21**: a beneficially stronger field-acceleration is observed with H* exposure, resulting in smaller degradation at operating E_{ox}. Moreover, the energy profile of the NBTI-generated D_{it} appears similar in all stacks (**Fig. 22**), ruling out the formation of different types of interface states as a potential consequence of H* exposure.

To understand the NBTI reliability improvement demonstrated with H* exposure further, we calibrated Comphy models [14] for all the studied gate stacks. D_{it} generation was first calibrated based on the conductance peak increase with stress; a hole trap defect band was then included and calibrated to accurately reproduce the measured NBTI stress/recovery traces (**Fig. 23**). The models are used here to visualize the reduction in hole trap density induced by increasing the oxidation temperature, or by treating the IL with hydrogen (**Fig. 24**): H* exposure is observed to yield the lowest density of hole traps in the vicinity of Si E_v, and as a consequence to yield the *best overall NBTI reliability, even when compared with conventional high-temperature IL's at elevated stress temperature* (**Fig. 25**).

CONCLUSIONS

Excessive hole trapping limits the NBTI reliability of low temperature SiO_2 IL's. We have correlated the NBTI dependence on the (*last*) IL oxidation temperature to unrelaxed interface strain, which induces excessive formation of hydrogen-related hole traps (hydroxyl-*E'*). By combining experimental observations with theoretical insights, we developed a low temperature (100-300°C) atomic hydrogen treatment which dramatically reduces the density of hole traps, yielding an oxide quality superior to a 900°C ref. IL. We have established a correlation between NBTI reliability and positive oxide charges, ascribing the latter also to the tail of the SiO_2 hole trap defect band reaching above Si E_v. These insights extend the validity of the 'Deal triangle' of oxidation [6] also to NBTI reliability (**Fig. 26**), and enable the fabrication of high quality SiO_2 at low temperatures by controlling the hydrogen dynamics, which represents a breakthrough for stacked CMOS tier fabrication.

ACKNOWLEDGEMENTS: Research funded by imec's Core Partner Program.

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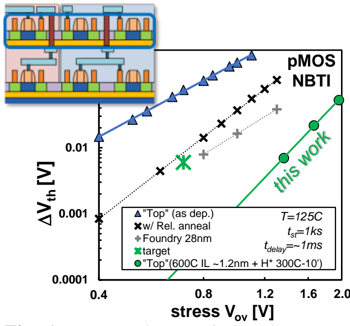


Fig. 1: Measured NBTI-induced ΔV_{th} for increasing stress V_{ov} (T=125°C, t_{stress}=1ks) in Si RMG HKMG. Omitting the so-called 'reliability anneal' for compatibility with stacked transistor top tier (inset sketch) results in a reliability penalty w.r.t. a Foundry 28nm ref. [2], overcome in this work by low temperature atomic H* exposure.

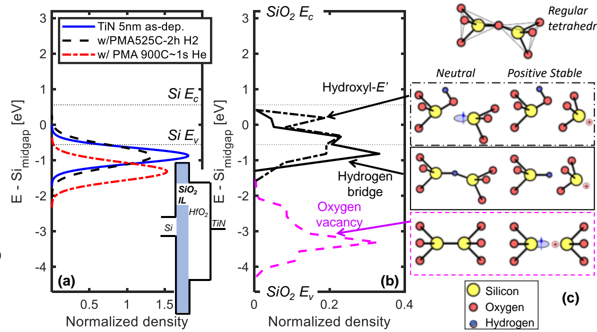


Fig. 2: **(a)** The probability density functions of the hole trap levels in the SiO_2 IL, as estimated with Comphy [3,14] for the as-dep. gate stack, or after a 525°C-2h post-metal anneal, or after a typical 'reliability anneal' (~900°C), compare well with **(b)** ab-initio statistical calculations of charge transition levels [4] of **(c)** the hydroxyl-*E'* and hydrogen bridge microscopic defect structures, but not with the deep levels calculated for the oxygen vacancies.

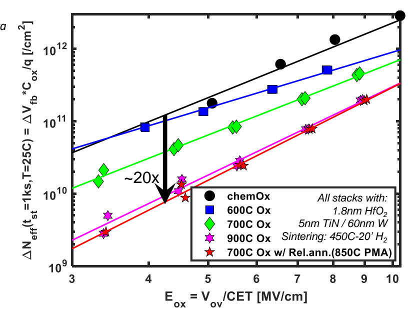


Fig. 3: Effective NBTI-induced trapped charge sheet density ΔN_{eff} measured for increasing stress E_{ox} (t_{stress}=1ks, T=25°C to expose mainly the trapping component) on RMG HKMG stacks with different IL's: a chemical oxide (~0.7nm), or three thermal oxides (~1.2nm) grown at 600/700/900°C. The stack with the 700°C IL was also exposed to a post-metal 850°C 'reliability anneal'.

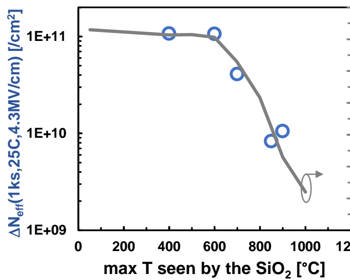


Fig. 4: Trapped charge density (ΔN_{eff} at E_{ox}=4.3 MV/cm, cf. Fig. 3) plotted as a function of the highest temperature seen by the IL during fabrication. The notable drop above 600°C compares well with the drop in Si-O bond stretching reported in [7] (line).

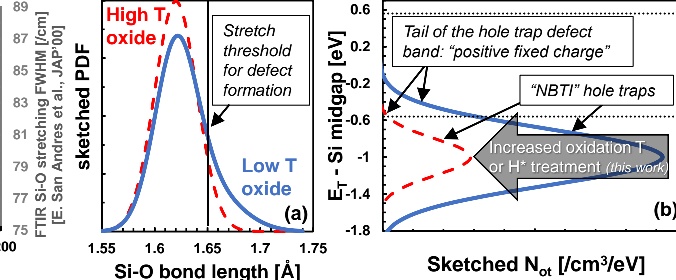


Fig. 5: Sketch of the proposed model: **(a)** Si-O bonds stretched beyond ~1.65Å can form hydroxyl-*E'* defects (after [9,10]). The fraction of stretched Si-O bonds (i.e., precursors) is larger in a low temperature oxide due to unrelaxed interface strain. **(b)** This results in a larger hole trap (and also positive oxide charge) density, which can be suppressed at low temperatures by carefully designed hydrogen treatments, as demonstrated here.

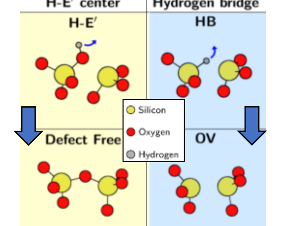


Fig. 7: By removing the sticking hydrogen atom, the hydroxyl-*E'* would tend to reform a correct Si-O-Si configuration (Fig. 6), while the hydrogen bridge would transform into an oxygen vacancy, with transition level too deep for charging at operating voltages, cf. Fig. 2 [4].

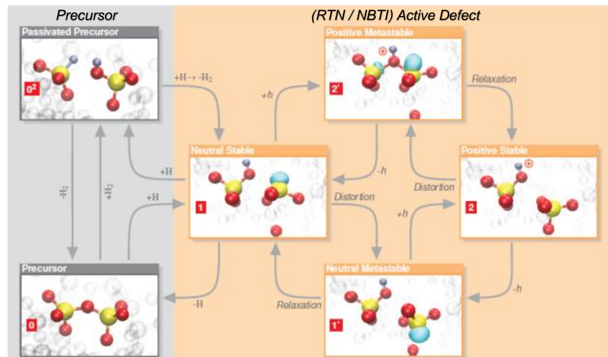


Fig. 6: 4-state configurations of the hydroxyl *E*', proposed in [15] to model NBTI kinetics: the Si dangling bond (1 and 1' configurations) loses its electron upon hole capture, yielding the positive meta-stable (2') and stable (2) configurations. By various interactions with hydrogen the defect can transform into a precursor state (left): this can explain defect 'volatility' observed in RTN studies [15].

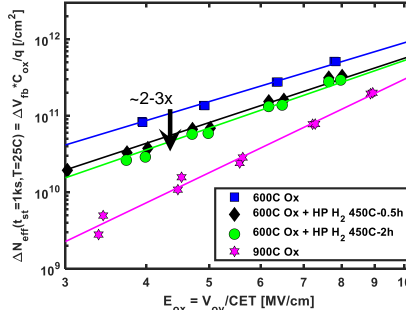


Fig. 8: Exposing the 600°C IL to high-pressure (20 atm) 450°C anneal in molecular H_2 for 0.5 or 2h before HKMG results only in a 2-3× reduction of the NBTI-induced ΔN_{eff}, i.e., not enough to match the reliability of a ref. stack based on a 900°C IL.

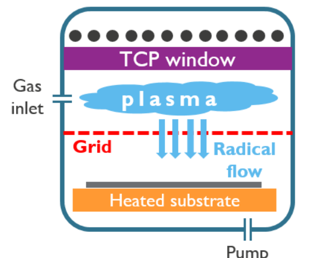


Fig. 9: Schematic of the remote plasma setup developed on a 300mm commercial etch tool to expose the IL to hydrogen radicals at the desired (low) temperature.

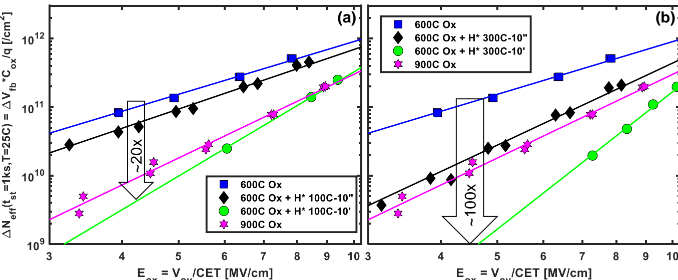
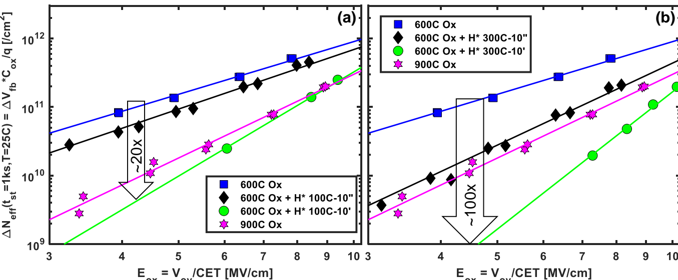



Fig. 10: Exposing the 600°C IL before HKMG to atomic H* for 10" or 10' at **(a)** 100°C, or **(b)** 300°C, results in a dramatic reduction (up to ~100×) of the NBTI-induced ΔN_{eff}(T=25°C). The 900°C ref. IL can be matched or surpassed (100 or 300°C) with a 10' exposure.

Fig. 11: ΔN_{eff} reduction factors for different H* exposures modelled as a first-order reaction with (low) activation energy ~0.21eV.

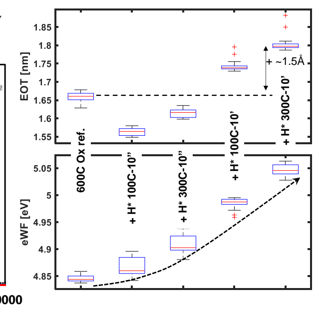


Fig. 12: **(a)** EOT and **(b)** eWF of the final stack for different H* exposures on the IL. A marginal EOT increase (1-1.5Å) is observed only for the 10' exposure, while a gradual increase of the eWF is consistently observed.

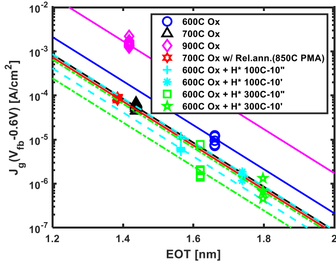


Fig. 13: Gate leakage density (sensed at V_{fb}-0.6V) of the stacks w/ the ref. IL's and w/ the 600°C IL exposed to H*, plotted vs. the EOT of the final stack. Dashed lines depict a typical J_g-EOT scaling trend (10× increase for 0.2nm scaling). H* always results in reduced J_g compared to the 600°C ref.

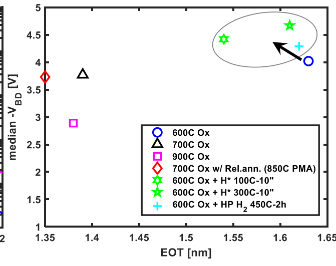


Fig. 14: Median V_g-to-breakdown measured in a set of 100μm² capacitors with various gate stacks, plotted vs. EOT. Exposing the 600°C IL to H_2 or H* results in improved breakdown robustness.

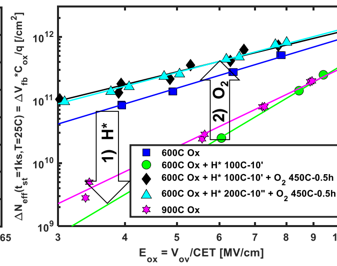


Fig. 15: NBTI-induced ΔN_{eff} vs. stress E_{ox}. The 600°C IL, after H* treatment (200°C-10" or 100°C-10'), was exposed to O_2 450°C-0.5h to induce re-oxidation of the Si surface at low temperature. The latter negates the NBTI improvement.

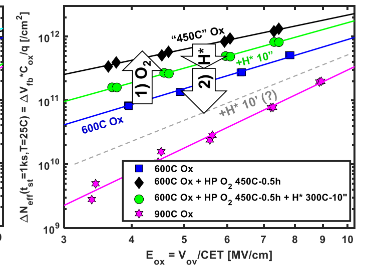


Fig. 16: NBTI-induced ΔN_{eff} vs. stress E_{ox}. The 600°C IL was exposed to 20atm O_2 450°C-0.5h to induce an EOT regrowth of ~2Å, resulting in further degraded NBTI; a subsequent exposure to H* (300°C-10") improves the reliability, which might be completely restored by longer exposures.

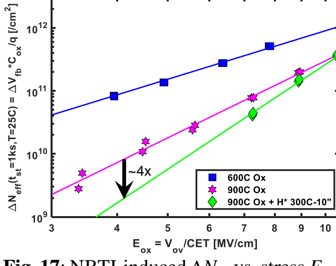


Fig. 17: NBTI-induced ΔN_{eff} vs. stress E_{ox}. Exposing a 900°C IL to H* (300°C-10") results in further reliability improvement.

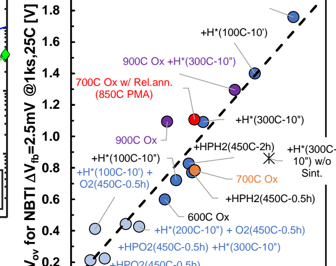


Fig. 18: Correlation plot of NBTI reliability (shown as the V_{ov} necessary to reach a 2.5mV shift after 1ks stress at 25°C) vs. the eWF. Stacks with improved reliability – i.e., with IL grown at higher temperature, or exposed to H_2 or H* – always show an increased eWF (i.e., reduced positive charge, cf. Fig. 5b). Note that the V_{ov} improvement range (0.2→1.8V) is much larger than the eWF increase (4.73→5.04eV), which proves that the NBTI improvement is not solely due to fixed charge reduction (lower E_{ox} at same V_{ov}).

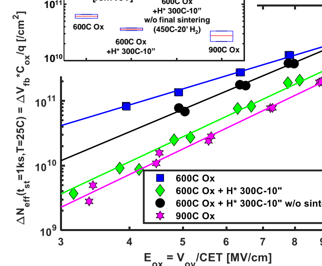


Fig. 19: NBTI-induced ΔN_{eff} vs. stress E_{ox}. Omitting the final post-metal sintering (400°C-20',1atm H_2) partially negates the improvement induced by IL exposure to H* (300°C-10"), and results in larger time-zero D_{it} (inset, 2×10^{11} vs. 4×10^{10} /cm²/eV).

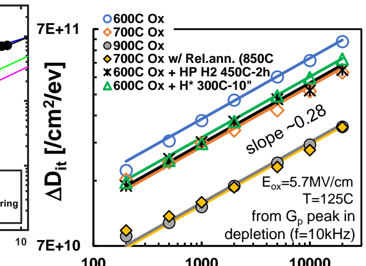
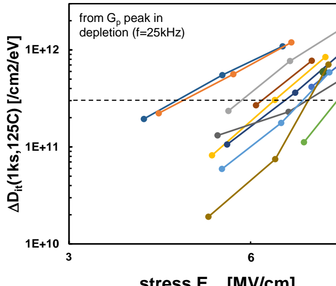


Fig. 20: NBTI-induced D_{it} generation kinetics monitored by the parallel conductance peak in depletion (f=10kHz) during 125°C stress at E_{ox}= 5.7MV/cm. Same kinetics is observed irrespective of the IL treatment; exposure to H_2 or H* reduces the ΔD_{it} on the 600°C IL stack, matching a 700°C ref. IL, while a more stable interface is observed in the 850-900°C IL's.



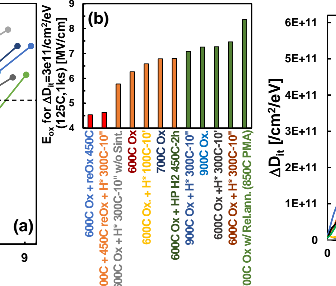


Fig. 21: **(a)** NBTI-induced D_{it} generation monitored on various gate stacks by the parallel conductance peak in depletion (f=25kHz) during stress at 125°C and increasing E_{ox}. **(b)** Estimated E_{ox} to induce $\Delta D_{it}=3\times10^{11}$ cm^{-2}eV^{-1} after 1ks stress [cutline of (a)] plotted vs. the stack configuration, from worst to best. Re-oxidation at 450°C results in poorest interface stability, which is instead substantially improved by increasing the oxidation T or exposing the (600°C) IL to HP H_2 or H*.

Fig. 22: **(a)** $\Delta D_{it}(E)$ profile induced by 20ks NBTI stress at E_{ox}=5.7MV/cm, 125°C, as extracted from C-V stretch-out correction [13]. **(b)** $\Delta D_{it}(E)$ profile as in (a), normalized to the peak amplitudes.

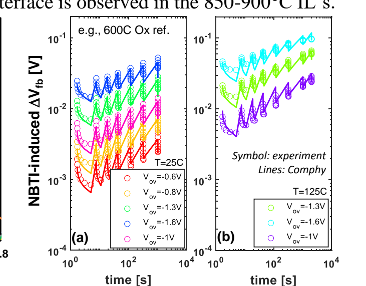
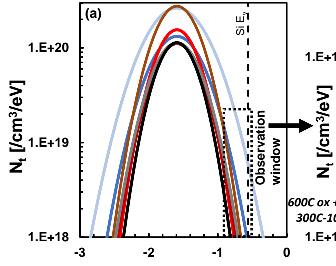


Fig. 23: Comphy models are calibrated to reproduce the NBTI stress/recovery sequences measured on each stack at increasing stress V_{ov}, at **(a)** 25°C and **(b)** 125°C (600°C ref. shown here as example).



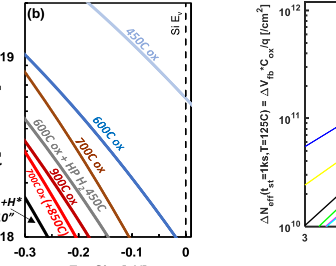


Fig. 24: **(a)** Hole trap defect band calibrated in Comphy (cf. Fig. 23): only N_t and σ_{Et} were adjusted to reproduce the NBTI kinetics of each stack. **(b)** Zoom-in on the energy levels right below Si E_v: exposure of a 600°C oxide to H* (300°C-10") results in the least detrimental defect band (even compared to the 900°C IL).

Fig. 25: NBTI-induced ΔN_{eff} vs. stress E_{ox} after 1ks stress, here at elevated stress temperature (125°C). Exposing a 600°C IL to H* (10', 100/300°C) supresses hole trapping (Figs. 10,24), and moderately reduces also the D_{it} generation (Figs. 20-22), yielding best overall NBTI reliability, even with respect to a 900°C IL or to a stack exposed to a 850°C 'reliability anneal'.

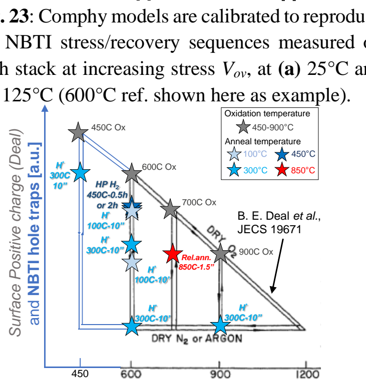


Fig. 26: This work extends the validity of the "Deal-triangle" [6] from surface positive charge to NBTI reliability. Hole trapping in SiO_2 is controlled by oxidation temperature, with the last oxidation determining the charging trap density. After oxidation, hole traps can be passivated by H* at low temperature (100-300°C) or –less effectively and at higher temperatures (450°C)– by HP H_2.