Journal of Applied Physics

RESEARCH ARTICLE | FEBRUARY 19 2025

Cu interconnect lifetime estimation in the presence of thermal gradients

Y. Ding ; O. Varela Pedreira ; M. Lofrano ; H. Zahedmanesh ; I. Ciofi ; T. Chavez ; H. Farr ; I. De Wolf ; K. Croes

J. Appl. Phys. 137, 075106 (2025)
https://doi.org/10.1063/5.0245489

Articles You May Be Interested In

Void-dynamics in nano-wires and the role of microstructure investigated via a multi-scale physics-based model

J. Appl. Phys. (March 2021)

A framework for combined simulations of electromigration induced stress evolution, void nucleation, and its dynamics: Application to nano-interconnect reliability

J. Appl. Phys. (October 2023)

Investigating the electromigration limits of Cu nano-interconnects using a novel hybrid physics-based model

J. Appl. Phys. (August 2019)

11 February 2026 10:29:35

Journal of Applied Physics | ARTICLE | pubs.aip.org/aip/jap

Cu interconnect lifetime estimation in the presence of thermal gradients

Cite as: J. Appl. Phys. **137**, 075106 (2025); doi: 10.1063/5.0245489
Submitted: 27 October 2024 · Accepted: 28 January 2025 ·
Published Online: 19 February 2025

View Online

Export Citation

CrossMark

Y. Ding,[1,2,a)] O. Varela Pedreira,[2,b)] M. Lofrano,[2,c)] H. Zahedmanesh,[2,d)] I. Ciofi,[2,e)] T. Chavez,[3,f)] H. Farr,[3,g)] I. De Wolf,[1,2,h)] and K. Croes[2,i)]

AFFILIATIONS

[1]Department of Materials Engineering, Faculty of Engineering Sciences, KU Leuven, Leuven B-3001, Belgium
[2]imec, Kapeldreef 75, Leuven B-3001, Belgium
[3]QualiTau Inc., 5303 Betsy Ross Dr., Santa Clara, California 95054, USA

[a)]**Author to whom correspondence should be addressed:** youqi.ding@imec.be
[b)]**Electronic mail:** olalla.varelapedreira@imec.be
[c)]**Electronic mail:** melina.lofrano@imec.be
[d)]**Electronic mail:** houman.zahedmanesh@imec.be
[e)]**Electronic mail:** ivan.ciofi@imec.be
[f)]**Electronic mail:** tonyc@qualitau.com
[g)]**Electronic mail:** hosainf@qualitau.com
[h)]**Electronic mail:** ingrid.dewolf@imec.be
[i)]**Electronic mail:** kristof.croes@imec.be

11 February 2026 10:29:35

ABSTRACT

Through physical and electrical analysis, the impact of thermal gradients on mass transport in Cu interconnects is studied using a dedicated test structure. The key physical parameter for thermomigration (TM), the heat of transport (Q^*), is evaluated experimentally to be 0.21 eV. Furthermore, an analytical model based on existing 1D physics-based models [M. A. Korhonen *et al.*, J. Appl. Phys. **73**, 3790–3799 (1993); H. Zahedmanesh *et al.*, Microelectron. Reliab. **111**, 113769 (2020)] is proposed to predict the time to void nucleation, the void growth rate (v_{growth}), and the time to failure (TTF) due to TM. Also, their dependence on temperature (T), temperature gradient $\left(\frac{dT}{dx}\right)$, and second derivative of the temperature $\left(\frac{d^2T}{dx^2}\right)$ is derived. This analytical model calibrated using experimental data predicts a TTF of 38 years for a 1 μm wide Cu interconnect under specific stress conditions: an operating temperature of 100 °C, a local temperature increase of 67 °C, and a $\frac{d^2T}{dx^2} = -2.9\,°\mathrm{C}/\mu\mathrm{m}^2$ induced by an external heat source.

© 2025 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution-NonCommercial 4.0 International (CC BY-NC) license (https://creativecommons.org/licenses/by-nc/4.0/). https://doi.org/10.1063/5.0245489

I. INTRODUCTION

In electronic circuits, the back-end-of-line (BEOL) metal interconnects handle power delivery and signal distribution from the front-end-of-line (FEOL) transistors to the package in which the circuits are embedded. Due to requirements for increased computational speed and higher memory capacity, smaller and smaller densely packed transistors and memory cells are being developed. Consequently, the dimensions of BEOL interconnects need to shrink as well making RC delay in the BEOL, a critical factor affecting overall circuit performance.[1–3] Options to enhance the performance and to reduce the RC delay of these scaled interconnects have been extensively explored, such as optimizing the Cu metallization process,[4–8] introducing new dielectric materials,[9,10] and ultimately relocating the power delivery network to the backside of the chip.[11,12] Although these developments are beneficial for the overall chip performance, they affect the interconnect reliability, and, thus, trade-offs between performance and reliability need to be made.

© Author(s) 2025

Despite major advances in research to replace Cu with alternative metals,[13,14] Cu remains the primary interconnect material in today's market due to its suitability for mass production and its widespread adoption in industry. Hence, continued fundamental research about the degradation mechanisms of Cu interconnects is required.

Historically, two main metal reliability issues were being addressed in Cu interconnects: electromigration (EM) and stress-induced voiding (SIV). EM involves atom migration through a momentum exchange between electrons and Cu atoms, which results in a tensile stress built up at the cathode side of an interconnect, eventually leading to void nucleation.[15–17] Continued current stress leads to void growth and, finally, to interconnect failure. SIV,[18–21] on the other hand, is driven by mechanical stress gradients in Cu. Stresses and stress gradients in interconnect metals are the consequence of the coefficient of thermal expansion mismatches between different materials used in the BEOL. During cooling down from deposition temperature to room temperature, some materials shrink more than others, leading to mechanical stresses. These process-induced stress gradients lead to void nucleation and growth, potentially resulting in opens.

Next to currents and mechanical stress gradients, often neglected driving forces for metal degradation in Cu interconnects are thermal gradients. The presence of thermal gradients induces another failure mechanism called thermomigration (TM). In older BEOL technologies, thermal gradients were negligible. With scaling, however, concerns regarding thermal gradients arise due to an increased self-heating induced by higher current densities and an increased metal electrical resistance.[22–25] Additional concerns come from the increased heating generated by the high amount of densely stacked transistors and the related required external cooling.[26] These different factors are expected to create higher thermal gradients in advanced BEOL interconnects, potentially causing metal degradation due to TM. Note that this concern is not limited to classical BEOL interconnects for power and signal distribution. The impact of thermomigration is not only relevant for logic and memory systems, but also for silicon photonic devices, where W-heaters are used to control the temperature of the waveguide.[27] W-heaters can generate significant heat, leading to high-temperature gradients, which can accelerate EM failures in their Cu injectors.[28,29]

The impact of TM has been extensively explored in solder joints,[30–32] where TM was observed to reduce lifetimes by a factor of 6 during classical EM testing.[33] Recent publications focused on the impact of temperature gradients on the degradation of metal interconnects. Tan *et al.*[34] developed an atomistic model allowing to compute atomic fluxes due to electron winds, temperature gradients, and mechanical stress gradients. The authors concluded that driving forces from TM are comparable in magnitude to EM. Zahedmanesh *et al.*[35] adapted the Korhonen 1D physics-based model to estimate the void nucleation time due to thermal gradients for Cu interconnects. This study estimated that a temperature difference of more than 25 °C can cause void nucleation in 10 nm wide Cu interconnects. Somaiah *et al.*[36] experimentally observed that mass transport driven by an electric current can be amplified at the cathode and reduced at the anode due to an interaction between TM and EM. Cui *et al.*[37] proposed a 1D solution to evaluate the acceleration factor for degradation due to a given current density. This acceleration factor was found to be 4.2 for current densities in the range of 2–5 MA/cm^2 when TM accompanies EM in Al interconnects.

In addition to understanding the interaction between TM and EM, it is crucial to conduct comprehensive studies regarding the TM phenomenon itself in interconnects. This includes examining the physical parameters of TM, the void dynamics, and the TM-related lifetime. The first two questions were addressed in previous publications.[38,39] This paper reports on the impact of thermal gradients on the lifetime of metal interconnects. By using a dedicated test structure and advanced modeling, Cu interconnect lifetime estimations in the presence of thermal gradients are proposed. The first section of this paper reviews common EM, SIV, and TM theories. The second section describes the developed test structure and the experimental setup for its reliability characterization. In the Experimental section, the long-term TM measurements are described and the results are discussed. Afterward, in the Modeling section, an electro-thermal finite element model (FEM) is used to estimate the relevant temperatures and temperature gradients, and a 1D numerical physics-based model is used to assess the time to void nucleation (TTV). Next, after calibration with experimental data, analytical solutions for TTV, void growth rates (v_{growth}), and time to failure (TTF) are proposed. Finally, this analytical lifetime prediction model is used to quantify the influence of temperature (T), temperature gradient $\left(\frac{dT}{dx}\right)$, and second derivative of the temperature $\left(\frac{d^2T}{dx^2}\right)$ on interconnect lifetimes.

11 February 2026 10:29:35

II. MODELS FOR ESTIMATING THE LIFETIME OF EM, SIV, AND TM

To assess the impact of EM and SIV on interconnect lifetimes, extensive studies on mass transport-induced failures driven by electron winds and stress gradients have been performed. During diffusion-dominated mass transport processes, void nucleation occurs first, followed by void growth.

The time to void nucleation can be modeled with the 1D physics-based model by Korhonen.[40] This model proposes a relationship between atomic mass transport and stress evolution over time in an interconnect. Assuming that vacancy concentrations in a confined metal line reach an equilibrium, the partial differential equation for stress evolution can be written as

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left(\frac{DB\Omega}{k_B T}\left(\frac{\partial \sigma}{\partial x} - \frac{Z^* e\rho j}{\Omega}\right)\right), \quad (1)$$

$$D = D_0 \exp\left(\frac{-E_a}{k_B T}\right), \quad (2)$$

where B is the effective elastic bulk modulus, σ is the hydrostatic stress, D is the effective atomic diffusivity with temperature dependence, D_0 is the diffusivity pre-exponential factor, k_B is the Boltzmann constant, Ω is the atomic volume, Z^* is the effective charge number, e is the electronic charge, j is the current density, and E_a is the effective activation energy. By defining a critical stress

© Author(s) 2025

level and evaluating the stress evolution over time, the time to void nucleation can be predicted.

Because Korhonen's model does not allow to address impacts from geometry, microstructure, barriers and passivation layers, etc., more precise and complex models have been developed. In Ref. 41, the impact of a via taper angle and line extension on EM was studied using two-dimensional simulations. Also, assessing the impact of microstructure[42] and more general stress evaluation studies have been done using three-dimensional simulations.[43,44] Important to note is that these advanced models still demonstrate good agreement with the 1D Korhonen model, but their complexity requires more calculations, making them challenging to account for the impact of thermal gradients.

After a void is nucleated, the tensile stresses at the void position are relaxed abruptly.[41,45] Under the applied stress conditions (temperature and current density), the void grows, leading to a resistance increase of the interconnect. The interconnect is considered as failed when the increase of the resistance reaches predefined failure criteria. The time at which this happens is called the time to failure (TTF).

The temperature and current density dependence of the Cu interconnect EM lifetime can be modeled by using the empirical equation formulated by Jim Black,[46,47]

$$MTTF = A\left(\frac{1}{j}\right)^{n} \exp\left(\frac{E_a}{k_B T}\right), \tag{3}$$

where $MTTF$ is the median time to failure, A is a constant that contains a factor involving the cross-sectional area of the interconnect, and n is the current exponent. The first attempts to include the impact of Joule heating-induced temperature gradients on lifetime were done by studying current crowding during void nucleation.[48] In that study, through a statistical model of thin film conductors, the authors studied the effect of local heating induced by local cross-sectional area changes and observed an increase in the current exponent with current density.

In Black's equation, the impact of a temperature gradient is not included. The atomic mass transport arising from TM can be written as follows:[30]

$$J_{TM} = -\frac{DCQ^{*}}{k_B T^2}\frac{\partial T}{\partial x}, \tag{4}$$

where Q^* is the heat of transport, C is the atomic concentration, T is the temperature, and $\frac{\partial T}{\partial x}$ is the temperature gradient. This equation describes the atom migration from high-temperature to low-temperature regions. In[38,39] we experimentally observed TM-induced voids and estimated the physical parameters Q^* and D_0 by using the 1D physics-based model.[35,40] However, accurately estimating the lifetime in the presence of thermal gradients remained unresolved and will be addressed here.

III. TM TEST STRUCTURE

The used test structure consists of a classical EM structure where an on-chip heater is placed underneath the EM line (Fig. 1). The on-chip heater is used to induce thermal gradients in the EM line above it. The EM structure consists of a 120 μm long, 1 μm wide Cu metal 2 (M2) line, 10 μm wide Cu metal 1 (M1) injectors, and 0.6–0.6 μm Cu vias. This injector is fabricated in M1 with a single damascene process and is electrically connected to bondpads. The V1/M2 level is fabricated with a dual-damascene process. A metal local sense (MLS) is added to the M2 line, positioned 10 μm from the edge of the M1 injector. The purpose of the MLS is to detect small changes in resistance during stress.[49] Cu metallization consists of a physical vapor deposited (PVD) TaN/Ta barrier/linear followed by a PVD Cu seed, Cu plating, and a chemical mechanical polishing (CMP) step.[29,39] The heater element is a meander with 300 nm wide tungsten (W) lines fabricated below the M1 level (W-heater) and is situated between the MLS and the M1 injector so it heats the region between the M1–via–M2 and the MLS (*M2_s*). The W-heater is directly connected electrically to bondpads, enabling heat generation by applying currents.

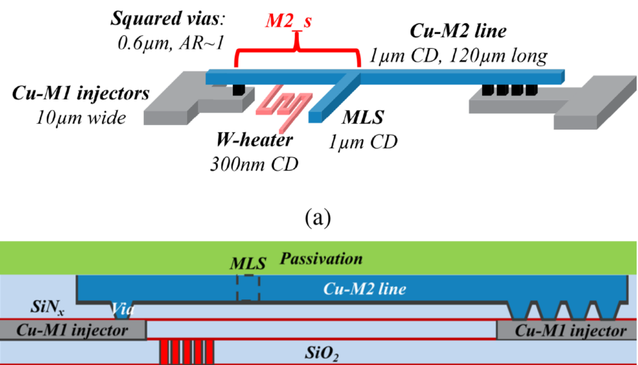


FIG. 1. The TM test structure consists of a classic EM test structure with a local sense (MLS) positioned at a distance of 10 μm away from the M1 injector. A W-heater is placed 2 μm away from the M1 injector below M1. The dielectric between the W-heater and the Cu-M2 line is 1 μm of SiO_2. The 3D schematic is shown in (a) and the cross-sectional cartoon is shown in (b). (a) Adapted with permission from Y. Ding *et al.*, Thermomigration-induced void formation in Cu-interconnects-Assessment of main physical parameters, 2023 IEEE IRPS. Copyright 2023 IEEE. (b) Adapted with permission from Ding *et al.*, Microelectron. Reliab. **138**, 114632 (2022). Copyright 2022 Elsevier.

IV. EXPERIMENT

Long-term package level tests are carried out in a package level EM test system. The sample is located in an oven. Current is sent to the W-heater to induce self-heating, which subsequently conducts heat to the metal line above, generating in addition to the oven temperature, temperature increases and temperature gradients at the M2 level. Using the specially designed MLS, any minor increases in resistance at *M2_s* can be monitored *in situ* through electrical measurements (Fig. 2).

11 February 2026 10:29:35

© Author(s) 2025

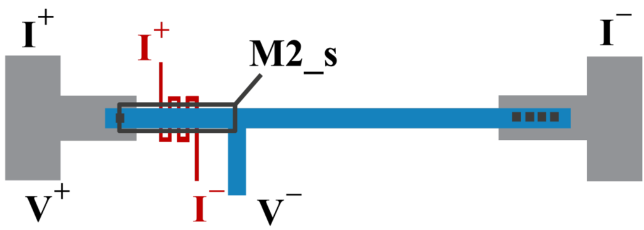


FIG. 2. Electrical connections for the TM test: Current is applied to the W-heater to induce Joule heating. The *M2_s* resistance ($< 1\,\Omega$) is measured using the four-point measurement technique by applying a low sense current (< 0.2 mA).

A. Experimental data

During stress, the resistance evolution of the structures is monitored for over 1750 h using oven temperatures varying between 75 and 200 °C. Simultaneously, different currents are applied to the W-heater (power from 12 to 25 mW) to induce varying self-heating, in the range from 41 to 84 °C at *M2_s*. The resistance change of *M2_s* in each sample for the different oven temperatures (T_{oven}) and under various average temperature increases in the *M2_s* region (ΔT_{M2_s}) induced by the W-heater are shown in Fig. 3. ΔT_{M2_s} is calculated using a calibrated FE model.[38] It can be seen that measurements with higher T_{oven} have more increase in resistance after the same duration of stress, despite the same local heating. This can be attributed to the increased ambient temperature, which

FIG. 3. TM measurements are carried out at varying oven temperatures. By varying the applied power to the W-heater from 12 to 25 mW, a temperature increase at *M2_s* from 41 to 84 °C is induced. Each sample is stressed at a certain oven temperature and heater power. ΔT_{M2_s} is the average temperature increase in the *M2_s* region. Throughout the test, resistance changes over time at *M2_s* are monitored for oven temperatures at (a) 75, (b) 100, (c) 150, and (d) 200 °C.

11 February 2026 10:29:35

© Author(s) 2025

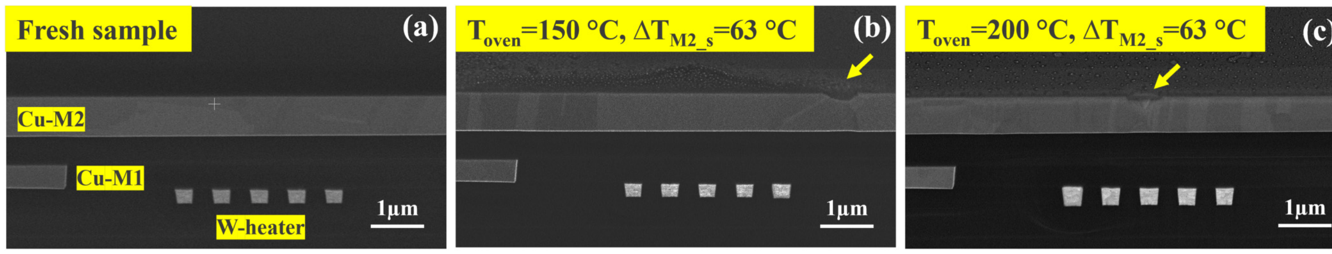


FIG. 4. (a) FIB result for the fresh sample shows no pre-existing void; (b) FIB result for sample stress at $T_{oven} = 150\,°C$, $\Delta T_{M2_s} = 63\,°C$ shows the void at Cu/SiCN interfaces right above the W-heater; (b) FIB result for sample stress at $T_{oven} = 200\,°C$, $\Delta T_{M2_s} = 63\,°C$ shows the void at Cu/SiCN interfaces directly above the center of the heater.

accelerates the atom diffusion process, similar to EM. Unfortunately, for some of the tests at higher T_{oven}, an unexpected degradation (large resistance increase) in the W-heater is observed before the planned 1750 h of testing time. Therefore, for these samples [Figs. 3(a) and 3(d)], only data from the initial phase are shown as during this time, the W-heater worked as expected.

B. Failure analysis

Failure analysis using a focused ion beam (FIB) was performed on failed samples, with three examples presented in Fig. 4. Figure 4(a) is the benchmark showing a fresh sample without any testing. No pre-existing voids are observed, indicating the samples were well processed. Figure 4(b) is a sample stressed at $T_{oven} = 150\,°C$, $\Delta T_{M2_s} = 63\,°C$ ($P_{heater} = 18.8\,mW$). A void is observed slightly to the right of the heater region. This can be attributed to the microstructure, suggesting that the triple point for flux divergence is located on the right side. Figure 4(c) is a sample stressed at $T_{oven} = 200\,°C$, $\Delta T_{M2_s} = 63\,°C$ ($P_{heater} = 18.8\,mW$). In this case, the void is observed directly above the center of W-heater. These results show voids nucleated at the Cu/SiCN interface, confirming that this interface is the dominant diffusion path. Furthermore, all voids are located above the W-heater region, aligning with our previous findings that predicted void formation at the location of the highest hydrostatic stress.[38,39]

C. Void nucleation model

Throughout the TM experimental results shown in Fig. 3, the $M2_s$ exhibits a progressive resistance increase over time. The local sense test structure enables monitoring minor resistance changes, associated with void dynamics. In our previous publication,[39] a three-stage void nucleation model was observed:

(I) Pre-void nucleation: The resistance remains constant until the critical stress is reached, initiating void nucleation.

(II) First void growth: The resistance shows a nearly linear increase with time.

(III) Second void growth: The resistance continues to increase nearly linearly over time, with a steeper slope. The change of the slope indicates the second void nucleation and growth together with the first void.

Most of the tested samples in this study display only the first and second stages of void growth, as shown in Fig. 5 and visible in some of the graphs from Fig. 3. The reason for that is high heater power is not applied at high oven temperature to ensure the heater reliability.

The power supplied to the W-heater, denoted as P_{heater}, directly influences the temperature increase under various stress conditions. The void temperature increase is linked to the heater power (P_{heater}) and the peak temperature at the metal line normalized by power ($\Delta T_{peak@1mW}$) is shown in Eq. (5). The temperature at the void location, T_{void}, is calculated using Eq. (6). By distinguishing these two stages, the TTV and slope of the resistance change shown in Fig. 3 are obtained and plotted in Fig. 6. In Sec. V B and Sec. VI A, the TTV will be compared with the results calculated by models. The linear slope of the resistance change in stage II will be used to estimate the v_{growth},

11 February 2026 10:29:35

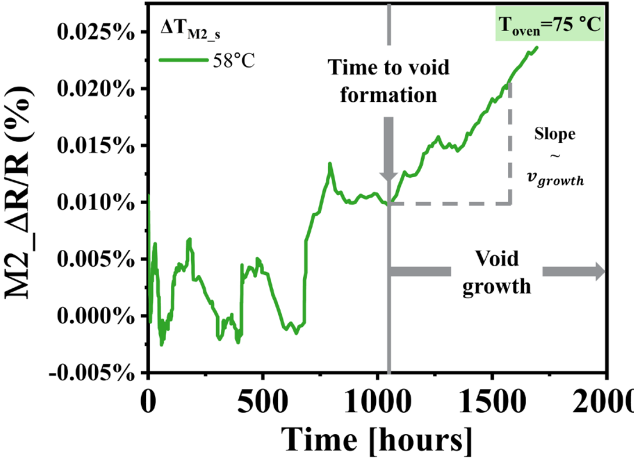
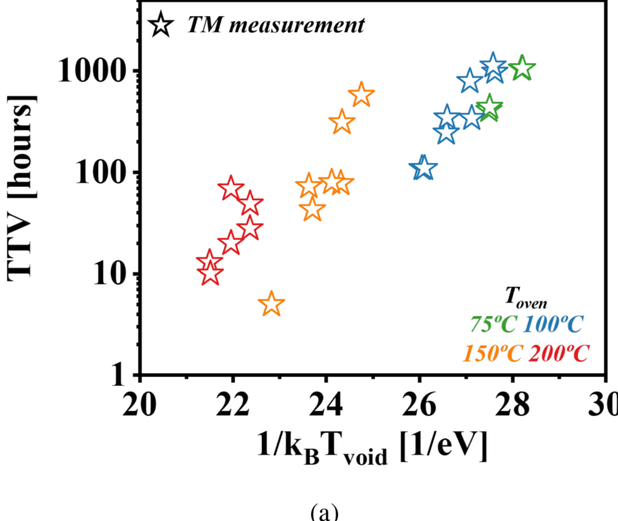
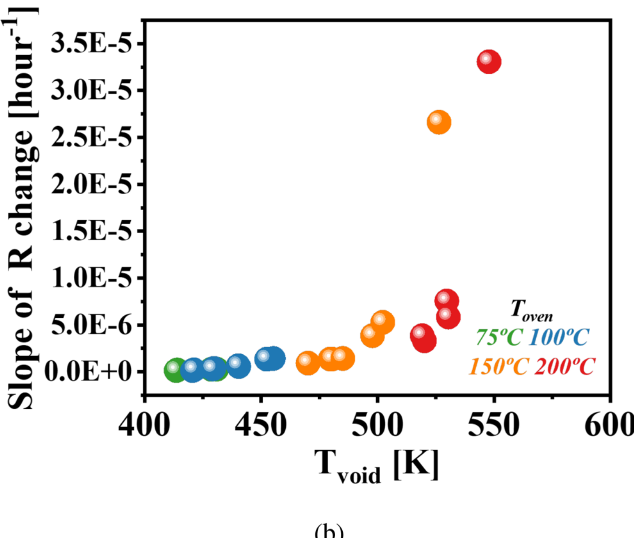


FIG. 5. Example of resistance increase in $M2_s$ over time for $T_{oven} = 75\,°C$ and $\Delta T_{M2_s} = 58\,°C$. Pre-void nucleation (stage I) is observed during the first 1060 h, during which the resistance remains constant. Subsequently, in stage II, the first void growth shows a linear increase of the resistance as a function of time.

© Author(s) 2025



(a)



(b)

FIG. 6. TTV (a) and the slope of resistance increase (b) are extrapolated from Fig. 3 under varying stress conditions.

$$\Delta T_{void} = \Delta T_{peak@1mW} \times P_{heater}, \tag{5}$$

$$T_{void} = T_{oven} + \Delta T_{void}. \tag{6}$$

V. NUMERICAL MODEL: COMBINED MODELING APPROACH FOR TIME TO VOID NUCLEATION

To model the impact of TM, we use an approach that combines FEM and 1D physics-based numerical model, where the results from FEM are used as input for the 1D physics-based model to obtain the TTV.

A. Calibrated electro-thermal finite element model

To characterize the temperature and temperature gradient within the test structure, a 3D FEM mimicking this structure[38] is built. Employing an electro-thermal coupling analysis, a current is applied to the W-heater to model the temperature increase resulting from Joule heating. The average Joule heating of the W-heater is also determined experimentally by measuring the resistance through Eq. (7), where R_0 is R at $T = 0\,^{\circ}$C and TCR denotes the temperature coefficient of resistance,

$$T = \frac{R(T) - R_0}{R_0 \times TCR}. \tag{7}$$

To validate the FEM, the temperature increase obtained through the Joule heating measurement is compared with the modeling results.[38] This calibrated model enables a comprehensive examination of the temperature and temperature gradient distributions across the entire structure. For a power input of 1 mW at the W-heater, the temperature, temperature gradient, and the second derivative of temperature distributions in M2 of the test structure are depicted in Fig. 7. The $M2_s$ metal line reaches an average temperature increase above $3.35\,^{\circ}$C due to the heat generated in the W-heater. The position directly above the center of the W-heater exhibits the highest temperature ($3.76\,^{\circ}$C) and the highest second derivative of the temperature ($-0.16\,^{\circ}\mathrm{C}/\mu\mathrm{m}^2$).

B. 1D physics-based model

Under temperature gradients, atoms tend to migrate from hot regions to cold regions. However, the non-uniform temperature distribution induces a stress gradient as well, which further promotes atom migration in the same direction as TM. As atoms migrate toward more tensile regions due to both stress migration (SM) and TM, the stress gradient changes. Eventually, SM begins to compete with TM. This competition continues until the stress reaches the criteria for void nucleation or saturation (SM compensates TM).

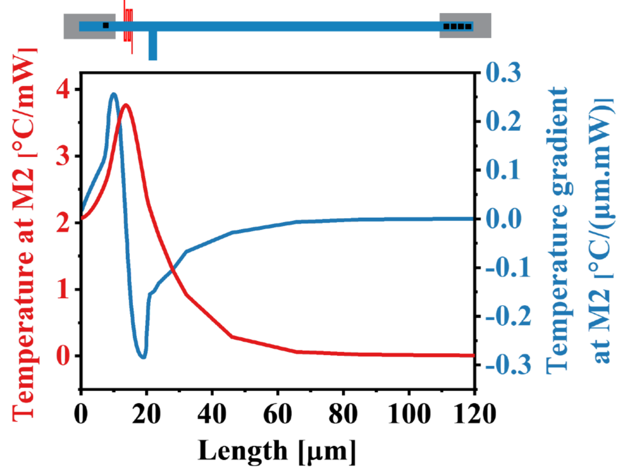
We employ a modified 1D physics-based model, as detailed in Ref. 35, to exclusively account for both TM and SM in void nucleation. This is represented by the following equation:

$$\frac{\partial \sigma}{\partial t} = \frac{\partial}{\partial x}\left(\frac{DB\Omega}{k_B T}\left(\frac{\partial \sigma}{\partial x} - \frac{Q^*}{\Omega T}\frac{\partial T}{\partial x}\right)\right). \tag{8}$$

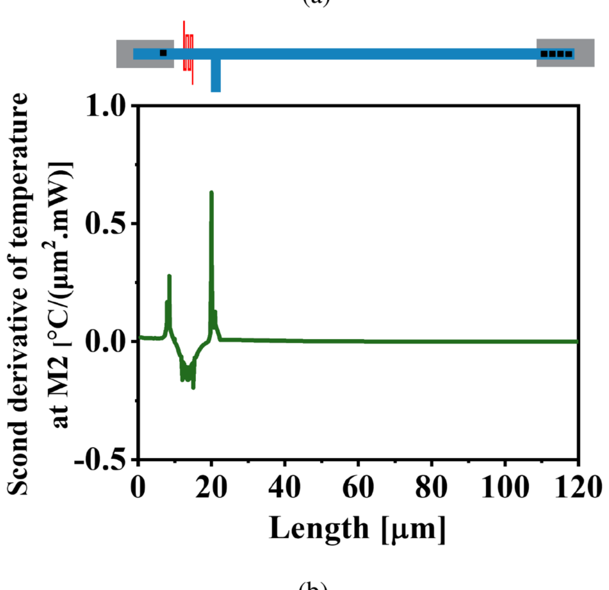
Using the temperature and temperature gradient computed from the FEM, and the parameters summarized in Table I, Eq. (8) allows us to predict the evolution of hydrostatic stress in the Cu line. Figure 8 presents a comparison of the TTV between the experimental results [from Fig. 6(a)] and the numerical modeling results [from Eq. (8)]. The model fits the data very well. The observed voids are located in the M2 layer,[39] directly above the center of the W-heater, where the temperature is at its peak value.

Our earlier estimates of $Q^* = 0.21(\pm 0.01)$ eV and $D_0 = 2.5 \times 10^{-9}(\pm 0.25 \times 10^{-9})\,\mathrm{m}^2/\mathrm{s}$ using TTV from experimental data and the 1D physics-based model[39] are confirmed again with the new data acquired at different test conditions.

11 February 2026 10:29:35



(a)



(b)

FIG. 7. Using the electro-thermal model, the temperature increase, the temperature gradient, and the second derivative of the temperature along the metal line above the W-heater are analyzed. A power of 1 mW applied to the W-heater results in a 3.76 °C temperature rise at *M2_s* directly above the W-heater, this generates a second derivative of the temperature of $-0.16\,°C/\mu m^2$.

VI. ANALYTICAL MODEL FOR THERMOMIGRATION

Although the numerical model can accurately predict the time to void nucleation, it is computationally intensive and requires detailed input for temperature and gradient distribution, which is challenging. Therefore, developing an analytical model to estimate the time to void formation more easily and quickly is necessary.

TABLE I. Physical parameters used as input in the model.

Parameter	Value	Description
D	$(2.5\times10^{-9})\times e^{\frac{-E_a}{k_BT}}$	Effective atomic diffusivity
E_a	0.84 eV	Effective activation energy
Q^*	0.21 eV	Heat of transport
$\Delta\sigma_{crit}$	$2(\sigma_{crit}-\sigma_0)=194$ MPa	Critical stress change
B	24.5 GPa	Effective elastic bulk modulus

There are two factors contributing to the mass transport of thermomigration: stress gradient and thermal gradient. Void nucleation primarily occurs due to the flux divergence of atom migration. In our studies, we can assume that the thermal gradient remains constant over time, as the heat conduction from the heater is unlikely to change significantly during the test. However, the stress gradient term is more intricate due to the time-dependent behavior of the stress evolution.

The flux of atom migration due to a thermal gradient has been shown before in Eq. (4). D is a function of temperature shown in Eq. (2). The divergence of this flux drives the accumulation or depletion of material, leading to void formation and growth. The flux divergence resulting from TM can be expressed as follows:

$$\nabla\cdot\mathbf{J_{TM}}=\frac{dJ_{TM}}{dx}=-d\left(D_0\exp\left(\frac{E_a}{k_BT}\right)\frac{CQ^*}{k_BT^2}\frac{\partial T}{\partial x}\right)\Big/dx. \tag{9}$$

The above equation can be further calculated as

$$\frac{dJ_{TM}}{dx}=-\frac{D_0CQ^*}{k_B}\exp\left(-\frac{E_a}{k_BT}\right)\times\left(\frac{E_aQ^*}{k_BT^4}\left(\frac{\partial T}{\partial x}\right)^2-\frac{2Q^*}{T^3}\left(\frac{\partial T}{\partial x}\right)^2+\frac{Q^*}{T^2}\frac{\partial^2T}{\partial x^2}\right) \tag{10}$$

11 February 2026 10:29:35

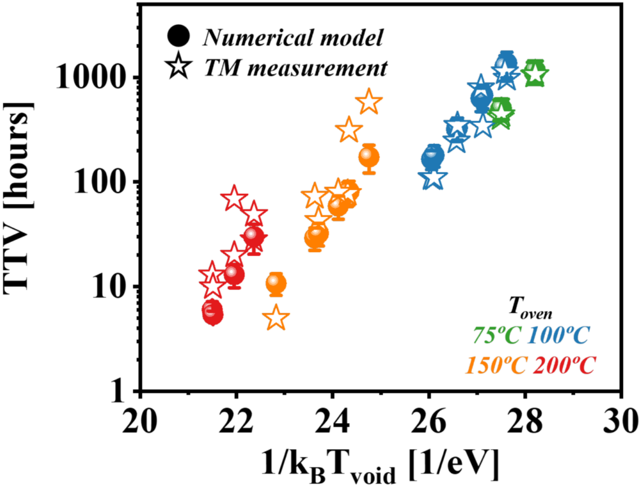


FIG. 8. Comparison of time to void (TTV) nucleation as a function of $1/k_BT_{void}$ between experiment data [Fig. 6(a)] and numerical results [Eq. (8)].

© Author(s) 2025

and after simplifying becomes

$$\frac{dJ_{TM}}{dx} = -\frac{D_0 C Q^*}{k_B T^2} \exp\left(-\frac{E_a}{k_B T}\right)\left(\frac{E_a}{k_B T^2}\left(\frac{\partial T}{\partial x}\right)^2 - \frac{2}{T}\left(\frac{\partial T}{\partial x}\right)^2 + \frac{\partial^2 T}{\partial x^2}\right). \quad (11)$$

The individual terms in brackets are defined as follows:

$$a = \frac{E_a}{k_B T^2}\left(\frac{\partial T}{\partial x}\right)^2, \quad (12)$$

$$b = -\frac{2}{T}\left(\frac{\partial T}{\partial x}\right)^2, \quad (13)$$

$$c = \frac{\partial^2 T}{\partial x^2}, \quad (14)$$

$$d = a + b + c = \frac{E_a}{k_B T^2}\left(\frac{\partial T}{\partial x}\right)^2 - \frac{2}{T}\left(\frac{\partial T}{\partial x}\right)^2 + \frac{\partial^2 T}{\partial x^2}. \quad (15)$$

Using the temperature and temperature gradient at different stress conditions obtained from the FE model, the values of the aforementioned terms were plotted in Fig. 9. The figure shows an example of the result when the $T_{oven} = 100\,°\text{C}$ and $\Delta T_{M2_s} = 58\,°\text{C}$ ($P_{heater} = 17.3$ mW). In the region above the heater, which is the region where the TM-induced voids are nucleated, the contribution from TM is predominantly influenced by factor c [Eq. (14)], which is mainly related to the change in the temperature gradient. The ratio between the term c in Eq. (14) and the term d in Eq. (15) as a function of void temperature for all tested conditions shown in Fig. 3 is plotted in Fig. 10. Since all ratios are between 1.0000 and 1.0005, we can conclude that in the region above the

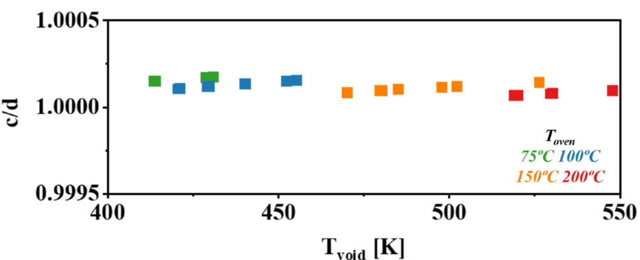
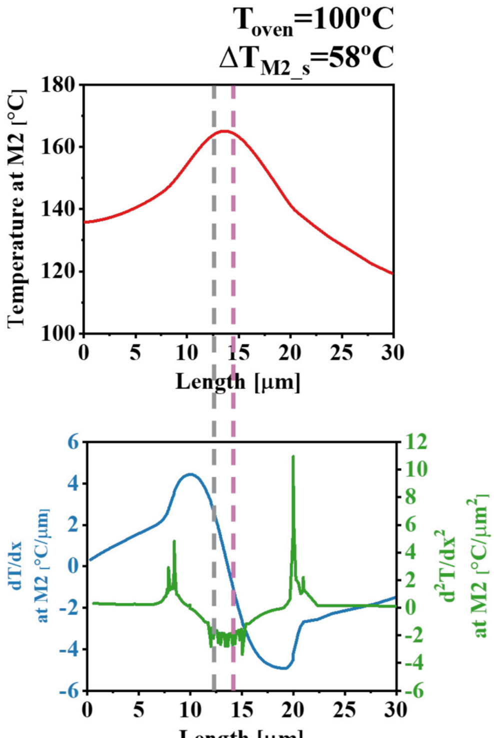


FIG. 10. The ratio between the term c in Eq. (14) and the term d in Eq. (15) as a function of void temperature for all tested conditions is shown in Fig. 3. The results are close to 1, indicating that d is the predominantly impact by c.



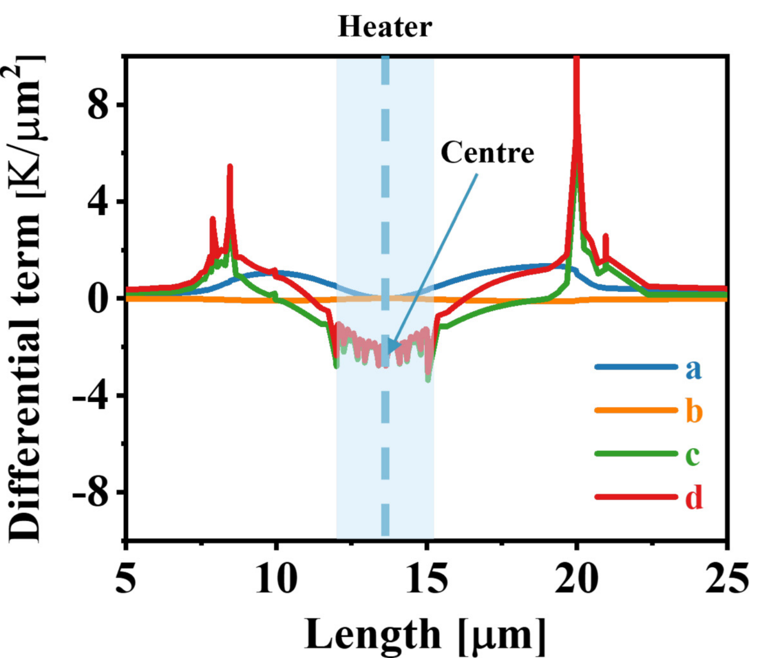


FIG. 9. A comprehensive comparison of each term [Eqs. (12)–(15)] associated with TM-induced flux divergence by using the T, $\frac{dT}{dx}$, $\frac{d^2T}{dx^2}$ values from FEM.

11 February 2026 10:29:35

heater, $d \approx c$,

$$d \approx c = \frac{\partial^2 T}{\partial x^2}. \tag{16}$$

This provides the simplified formula for flux divergence due to thermomigration as presented in Eq. (9). This equation is instrumental in analytically evaluating the impact of thermal gradient on void dynamics in interconnects,

$$\nabla \cdot \mathbf{J_{TM}} = -\frac{D_0 C}{k_B} exp\left(-\frac{E_a}{k_B T}\right)\frac{Q^*}{T^2}\frac{\partial^2 T}{\partial x^2}. \tag{17}$$

A. Void nucleation

In terms of void nucleation, contributions from both stress gradients and thermal gradients must be considered. The flux of atom migration due to a stress gradient can be expressed as follows:

$$J_{SM} = \frac{D}{k_B T}\frac{\partial \sigma}{\partial x}. \tag{18}$$

Therefore, the stress evolution over time under thermomigration can be expressed as

$$\frac{\partial \sigma}{\partial t} = \frac{B}{C}\frac{\partial (J_{SM} + J_{TM})}{\partial x}. \tag{19}$$

Figure 11 plots the change of atomic flux as a function of time at the peak temperature location when $T_{oven} = 100\,°\text{C}$ and $\Delta T_{M2_s} = 58\,°\text{C}$ ($P_{heater} = 17.3\,\text{mW}$). The mass transport driven by the thermal gradient remains constant over time, as indicated by the red line. A positive value of the flux divergence for TM suggests a loss of atoms at the peak temperature position during the experiment. The blue curve represents the contribution from SM. When a current is applied to the W-heater, a stress gradient is induced in the metal line due to the temperature distribution. This stress gradient contributes to mass transport during the initial hours, accounting for up to a maximum of 14% of the total mass transport.[39] As atom migration alters the stress gradient, SM begins to rival TM until it reaches saturation or void nucleation. The combined effects of TM and SM are illustrated by the green line. The decreasing trend over time represents the rising influence of the stress gradient which acts in the opposite direction of atomic flow. The red-hatched area under the red line represents the integration of the TM flux divergence over time, while the green-hatched area represents the integration of the combined TM and SM flux divergence over time. At the specific location of the metal line, the hydrostatic stress change over time can be calculated by considering TM and SM as follows:

$$\Delta \sigma = \frac{C}{B}\int_0^t \frac{\partial (J_{SM} + J_{TM})}{\partial x}\, dt. \tag{20}$$

Assuming that the temperature and temperature gradient remain constant throughout the measurement, the change in flux driven by the thermal gradient is also constant. Consequently, the expression for the time to void nucleation can be easily derived by considering only TM, as indicated by the red area in Fig. 11,

$$TTV_{TM} = \frac{C}{B}\frac{\Delta \sigma_{crit}}{\nabla \cdot \mathbf{J_{TM}}}. \tag{21}$$

Directly using Eq. (21) may lead to an underestimation of the time to void nucleation. While it is evident that stress migration also partially impacts void nucleation, calculating the change in stress gradient over time analytically remains challenging. To address this, the results obtained from the numerical model [Eq. (8)] and the analytical expression [Eq. (21)] are fitted giving a new expression of time to void nucleation, as shown in Eq. (22) and Fig. 12, which includes the contribution from stress migration. Note that

11 February 2026 10:29:35

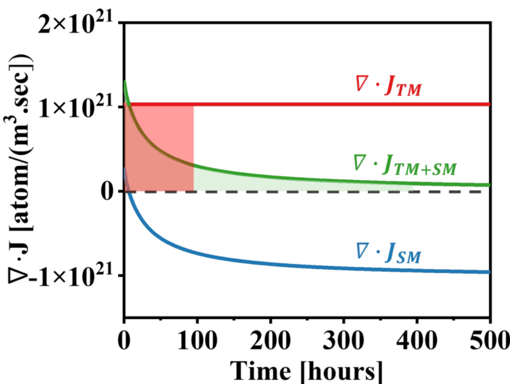


FIG. 11. The atomic flux divergences for TM, SM, and TM+SM are compared over time. The integrated area under the curve is directly correlated with the hydrostatic stress, indicating that neglecting the influence of SM leads to an underestimation of the time required for void nucleation.

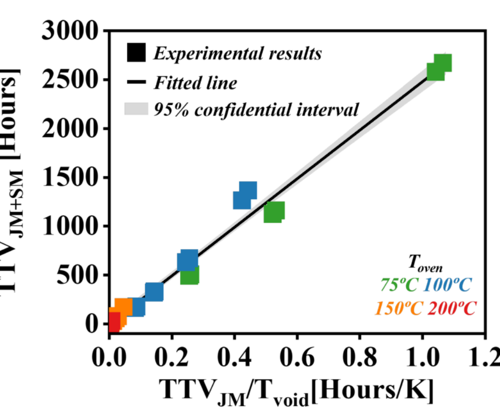


FIG. 12. The data calculated from the numerical model [Eq. (8)] for TTV_{TM+SM} are fitted with the data for TTV_{TM}/T_{void} from Eq. (21). A constant value $2484 \pm 62\,\text{K}$ is obtained from the fitting. The gray-hatched region represents the 95% confidence interval of the linear least squares fitting.

© Author(s) 2025

this constant value extrapolated by the fit may change depending on the structure dimensions and integration,

$$TTV_{TM+SM} = \frac{2484}{T_{void}} \times TTV_{TM}. \tag{22}$$

Merging Eqs. (17), (21), and (22), results in a new expression of TTV as shown in Eq. (23). α is the factor linked to the constant correction factor mentioned above and the critical stress for the void formation,

$$TTV_{TM+SM} = \alpha \times \frac{k_B}{D_0} \exp\left(\frac{E_a}{k_B T}\right) \frac{T}{Q^*} \left(\frac{\partial^2 T}{\partial x^2}\right)^{-1}, \tag{23}$$

$$\alpha = -2484 \times \frac{\Delta\sigma_{crit}}{B}. \tag{24}$$

Figure 13 shows the comparison between this new analytical equation [Eq. (23)], and the numerical model presented in Sec. V. It can be seen that the analytical model closely aligns with the numerical model, affirming its validity in predicting the time to void nucleation. Subsequently, we compared the results from the analytical model with the experimental data, as shown in Fig. 14. The agreement between the results highlights the robustness of the analytical formula to represent the interaction between TM and SM. This formula allows to calculate the TTV, making it possible to predict the reliability of metal interconnect structures under different TM stress conditions.

B. Void growth

The resistance increase shown in Fig. 6(b) can be linked to the void volume.[39] The four-point measurement setup is shown in Fig. 2, where the major contributor to the measured resistance is the $M2_s$ part. Assuming the void is cubic with length (l_{void}), width (w_{void}), and height (h_{void}), the change in measured resistance can be attributed to the resistance change in a small segment of the M2 with length (l_{void}) as shown in Fig. 15. The resistance of this small segment (R_{M2}) without the void can be expressed as a parallel connection between the barrier (Ta/TaN) and Cu,

$$R_{M2} = \frac{R_{Cu} R_{Ta/TaN}}{R_{Cu} + R_{Ta/TaN}} \approx R_{Cu}, \tag{25}$$

where R_{Cu} is the resistance of the Cu line and $R_{Ta/TaN}$ is the resistance of the Ta/TaN barrier. Since $R_{Ta/TaN}$ is approximately 340 times larger than R_{Cu} at this dimension due to its high resistivity and small cross-section area, R_{M2} is approximately equal to R_{Cu}. When a void is nucleated at this small segment of the Cu line, the

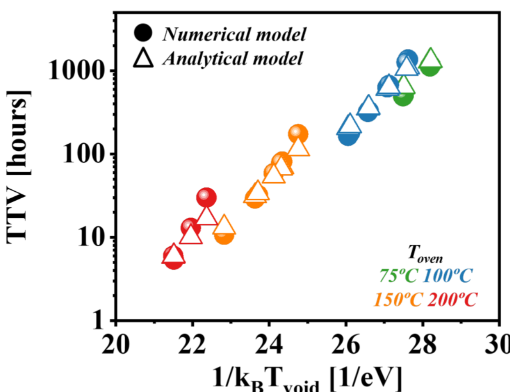


FIG. 13. Comparison of TTV as a function of $1/k_B T_{void}$ between numerical result [Eq. (8)] and analytical result [Eq. (23)].

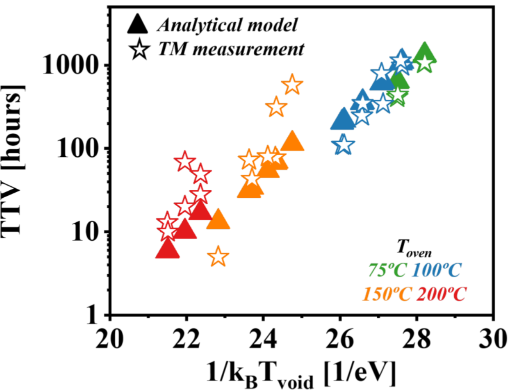


FIG. 14. Comparison of TTV as a function of $1/k_B T_{void}$ between experiment data [Fig. 6(a)] and analytical result [Eq. (23)].

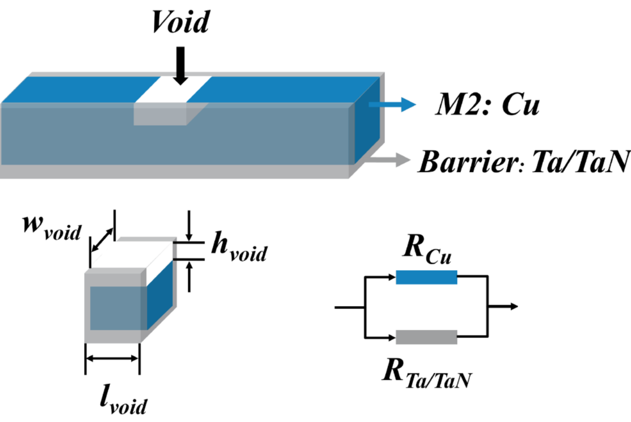


FIG. 15. Schematic of the M2 line shows Cu and the Ta/TaN barrier structure. The void shape is assumed to be cubic with dimensions: length (l_{void}), width (w_{void}), and height (h_{void}). The resistance of part of the M2 line composing the void with the length (l_{void}) is a parallel connection between Cu and the Ta/TaN barrier.

11 February 2026 10:29:35

© Author(s) 2025

resistance ($R_{M2,void}$) becomes

$$R_{M2,void} = \frac{R_{Cu,void} R_{Ta/TaN}}{R_{Cu,void} + R_{Ta/TaN}} \approx R_{Cu,void}, \tag{26}$$

where $R_{Cu,void}$ is the resistance of the Cu line with a void, which is larger than R_{Cu} due to the smaller cross-section area. The increase of resistance due to the void can be expressed as

$$\Delta R_{Cu} = R_{Cu,void} - R_{Cu} = \rho_{Cu}\left(\frac{l_{void}}{s_{Cu} - w_{void} \times h_{void}} - \frac{l_{void}}{s_{Cu}}\right), \tag{27}$$

where the s_{Cu} is the original cross-section area of the Cu line. The resistance change rate measured from the experiment can be expressed as

$$\Delta R = R_{M2,void} - R_{M2} \approx \Delta R_{Cu}, \tag{28}$$

$$\frac{\Delta R}{R} \approx \frac{\Delta R_{Cu}}{R} = \frac{\rho_{Cu} l_{void}}{R}\left(\frac{1}{s_{M2,Cu} - w_{void} \times h_{void}} - \frac{1}{s_{M2,Cu}}\right), \tag{29}$$

where R is the initial resistance of $M2_s$ measured at the beginning of the TM test and ΔR is the resistance change relative to R. In our 1D model introduced in Sec. V B, no change in the width and height direction is assumed, and thus the void growth along the line direction is related to the increase in l_{void} as

$$l_{void} \propto v_{growth} \times t, \tag{30}$$

where v_{growth} is the void growth rate and t is the time. Therefore, one can assume a direct correlation between the void growth rate and the change in resistance

$$\frac{\Delta R}{R} \propto v_{growth} \times t. \tag{31}$$

Our setup allows us to measure the $M2_s$ resistance increase continuously over time. In this scenario, the slope of the resistance increase is directly proportional to the void growth rate

$$Slope = \frac{\Delta R}{R}/t \propto v_{growth}. \tag{32}$$

It is established that following void nucleation, the stress surrounding the void rapidly relaxes to zero[41,45] and the impact from the stress gradient is relatively small at high temperatures.[50,51] At that moment, SM stops contributing to mass transport, making the thermal gradient the dominant driving force for void growth. Hence, in Fig. 16, only the slope of the resistance changes as a function of the atom flux due to TM is plotted. It can be observed that the slope of the resistance change shows a linear relationship with the TM-induced flux divergence. This observation confirms the assumption that TM is the primary driving force for void growth,

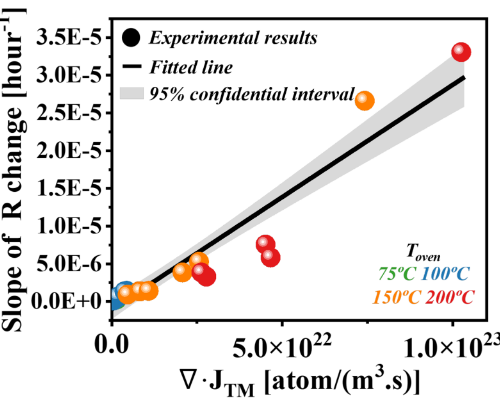


FIG. 16. The slope of resistance change observed in the TM experiment [Fig. 6(b)] is compared with the flux change for TM [Eq. (17)]. The linear relationship between these two suggests that TM dominates the void growth. The gray-hatched region represents the 95% confidence interval of the linear least squares fitting.

$$\frac{\Delta R}{R}/t \propto \nabla \cdot \mathbf{J_{TM}}. \tag{33}$$

Considering that the void growth rate is directly related to the change in flux caused by TM,

$$v_{growth} \propto \nabla \cdot \mathbf{J_{TM}}. \tag{34}$$

The equation for void growth can be expressed as

$$v_{growth} = \beta \times \frac{D_0}{k_B} \times \exp\left(-\frac{E_a}{k_B T}\right)\frac{Q^*}{T^2}\frac{\partial^2 T}{\partial x^2}, \tag{35}$$

where β is the factor that links the change in vacancy flux to void volume, as well as the relationship between resistance change and void volume. This factor can be extrapolated through a set of measurements on dedicated test structures.

C. Lifetime estimation

In conventional EM studies, the lifetime is defined by setting a failure criterion based on a certain increase in resistance, typically 20%. The time to failure consists of two components: the TTV and the time to reach a specified resistance increase, as shown in Eq. (36). Given that the TTV is typically much shorter compared to the time to reach a certain resistance increase, we can simplify the equation to consider only the second term. Hence, the equation for the TM-lifetime dependence on void temperature and the second derivative of temperature at this location can be expressed by Eq. (37),

$$TTF = TTV + \frac{\Delta R}{R \times v_{growth}}, \tag{36}$$

11 February 2026 10:29:35

© Author(s) 2025

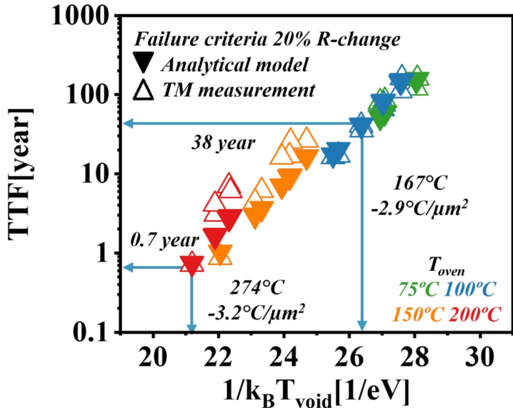


FIG. 17. Comparison of time to failure (TTF) formation as a function of $1/k_BT_{void}$ between experiment data (extrapolated from Fig. 3) and analytical result [from Eq. (37)].

$$TTF = \gamma \times \frac{k_B}{D_0} \times \exp\left(\frac{E_a}{k_BT}\right)\frac{T^2}{Q^*}\left(\frac{\partial^2 T}{\partial x^2}\right)^{-1}, \tag{37}$$

where γ links to β in v_{growth} and the failure criteria. Similar to β, this factor can be extrapolated through a series of measurements on dedicated test structures. Using Eq. (37), the TTF is calculated for all measured samples and plotted in Fig. 17 using open triangle markers. In order to compare these results to experiments, the 20% resistance increase criterion should be used. However, due to the unexpected heater degradation, a 20% increase in resistance could not be experimentally measured. Therefore, the linearly increasing part of the resistance (i.e. after TTV) of all samples was extrapolated using a linear relationship (Fig. 3), allowing to calculate the TTF based on a failure criterion of a 20% increase in resistance. These extrapolated results, represented by solid triangle markers, are compared with the analytical results in Fig. 17. A very good agreement is demonstrated between the model and the experimental data. The obtained TTF, shown in Fig. 17, can be compared with the TTV plotted in Fig. 14. The TTV is in the order of hours, while the TTF is in the order of years. The minimum time difference between TTF and TTV is a factor of 1000, confirming that the void nucleation phase is relatively short compared to the overall time to failure. Moreover, it can be deduced from the figure that at $T_{oven} = 200\,°C$, $\Delta T_{void} = 74\,°C$, and $\frac{d^2T}{dx^2} = -3.2\,°C/\mu m^2$, the sample fails after 0.7 yr. Under operating conditions where $T_{oven} = 100\,°C$, $\Delta T_{void} = 67\,°C$ and $\frac{d^2T}{dx^2} = -2.9\,°C/\mu m^2$, the estimated lifetime is 38 yr. This analysis demonstrates the feasibility of using this analytical equation to estimate the TM-induced failure time at various stress conditions.

It is worth noting that this analytical model enables the assessment of the impact of varying temperatures or the second derivative of temperature without knowing γ for a specific test structure. Similar to Black's equation, by maintaining a constant second derivative of temperature, the effective activation energy can be extrapolated from the TTF at different temperatures. In this scenario, where temperature is the only variable, the logarithm of Eq. (37) can be expressed as

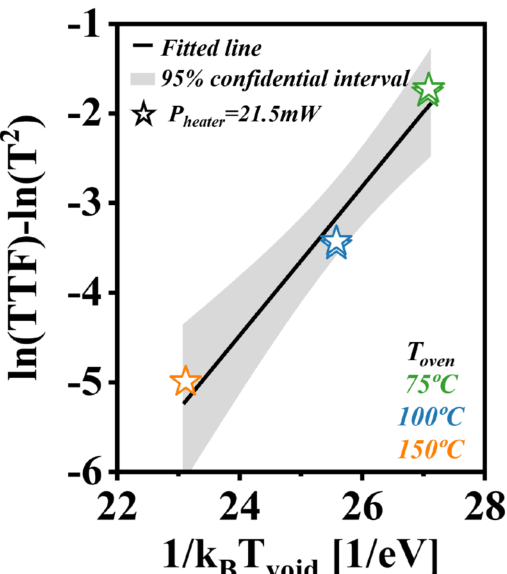


FIG. 18. Equation (38) is fitted for W-heater power ($P_{heater} \approx 21.5$ mW) under three different oven temperatures to determine the slope, which represents the effective activation energy. The TTF is experimental data at a 20% resistance increase, and the temperature is the sum of the void temperature increase ($\Delta T_{void} = 80.9\,°C$) and oven temperature. The gray-hatched region represents the 95% confidence interval of this non-linear least squares fitting.

11 February 2026 10:29:35

$$\ln(TTF) - ln(T^2) = \frac{E_a}{k_BT} + C, \tag{38}$$

where C is a constant including all the temperature-independent terms. To validate whether Eq. (38) can be used to extrapolate the effective activation energy, an example is plotted in Fig. 18. Non-linear least squares fitting is used to get the slope of the curve for three different oven temperatures (75, 100, and 150 °C) with W-heater power ($P_{heater} \approx 21.5$ mW, $\Delta T_{void} = 80.9\,°C$, $\frac{d^2T}{dx^2} = -3.4\,°C/\mu m^2$). The fitted E_a (0.83 ± 0.09 eV) is close to the 0.84 eV obtained from the classical EM test demonstrating the applicability of this analytical model for activation energy assessment.

VII. CONCLUSION

Thermomigration tests were performed on a dedicated test structure where a thermal gradient can be induced by the power dissipated in an on-chip W-heater. The resistance increase of the copper interconnect exhibits a typical void dynamics model with two stages: (i) pre-void nucleation and (ii) void growth. Using the TTV, we validated the physical parameters extrapolated from the 1D physics-based model previously reported in Ref. 39. Subsequently, an analytical model was derived to estimate the TTV, v_{growth}, and TTF based on the 1D physics-based model and electro-thermal model.

© Author(s) 2025

The results obtained from the analytical model were experimentally validated. These new developed and validated analytical models offer a straightforward way to calculate the impact of a thermal gradient on metal interconnect reliability.

ACKNOWLEDGMENTS

The authors would like to thank the participants of reliability and thermal meetings as well as the members of the Nano-interconnect program for the fruitful discussions. Also, imec's industrial affiliation R&D program on Optical I/O is acknowledged for support on the thermal gradient test structure. Myriam Van de Peer and Veerle Simons are acknowledged for their help with operational work. Chris Drijbooms and Fiona Crystal Mascarenhas are acknowledged for FIB inspections. Special thanks go to Xinyue Chang and Ahmed Saleh for their valuable discussions.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Y. Ding: Conceptualization (equal); Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (equal); Software (equal); Validation (equal); Visualization (equal); Writing – original draft (lead); Writing – review & editing (equal). **O. Varela Pedreira:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Project administration (equal); Resources (lead); Supervision (lead); Validation (equal); Visualization (equal); Writing – review & editing (equal). **M. Lofrano:** Conceptualization (supporting); Formal analysis (supporting); Methodology (supporting); Software (equal); Supervision (equal); Validation (supporting); Writing – review & editing (supporting). **H. Zahedmanesh:** Formal analysis (supporting); Software (equal); Validation (supporting); Writing – review & editing (supporting). **I. Ciofi:** Project administration (supporting); Resources (supporting); Writing – review & editing (supporting). **T. Chavez:** Investigation (supporting); Resources (supporting). **H. Farr:** Methodology (supporting); Resources (supporting). **I. De Wolf:** Conceptualization (equal); Data curation (supporting); Formal analysis (supporting); Funding acquisition (lead); Investigation (equal); Methodology (supporting); Project administration (equal); Resources (supporting); Supervision (equal); Validation (supporting); Visualization (supporting); Writing – review & editing (equal). **K. Croes:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (supporting); Project administration (lead); Resources (equal); Supervision (lead); Validation (supporting); Visualization (supporting); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1] M. R. Baklanov, C. Adelmann, L. Zhao, and S. D. Gendt, "Advanced interconnects: Materials, processing, and reliability," ECS J. Solid State Sci. Technol. **4**, Y1 (2014).
[2] R. Brain, "Interconnect scaling: Challenges and opportunities," in *2016 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2016), pp. 9.3.1–9.3.4.
[3] G. Bonilla, N. Lanzillo, C.-K. Hu, C. Penny, and A. Kumar, "Interconnect scaling challenges, and opportunities to enable system-level performance beyond 30 nm pitch," in *2020 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2020), pp. 20.4.1–20.4.4.
[4] A. S. Oates, "Strategies to ensure electromigration reliability of Cu/low-k interconnects at 10 nm," ECS J. Solid State Sci. Technol. **4**, N3168 (2015).
[5] D. Priyadarshini, S. Nguyen, H. Shobha, S. Cohen, T. Shaw, E. Liniger, C. Hu, C. Parks, E. Adams, J. Burnham, A. Simon, G. Bonilla, A. Grill, D. Canaperi, D. Edelstein, D. Collins, M. Balseanu, M. Stolfi, J. Ren, and K. Shah, "Advanced metal and dielectric barrier cap films for Cu low k interconnects," in *IEEE International Interconnect Technology Conference* (IEEE, 2014), pp. 185–188.
[6] N. Jourdan, M. van der Veen, V. Vega Gonzalez, K. Croes, A. Lesniewska, O. Varela Pedreira, S. Van Elshocht, J. Bömmels, and Z. Tőkei, "CVD-Mn/CVD-Ru-based barrier/liner solution for advanced BEOL Cu/low-k interconnects," in *2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC)* (IEEE, 2016), pp. 37–39.
[7] M. H. van der Veen, N. Jourdan, V. V. Gonzalez, C. J. Wilson, N. Heylen, O. V. Pedreira, H. Struyf, K. Croes, J. Bömmels, and Z. Tőkei, "Barrier/liner stacks for scaling the Cu interconnect metallization," in *2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC)* (IEEE, 2016), pp. 28–30.
[8] R. R. Patlolla, K. Motoyama, B. Peethala, T. Standaert, D. Canaperi, and N. Saulnier, "CMP development for Ru liner structures beyond 14 nm," ECS J. Solid State Sci. Technol. **7**, P397 (2018).
[9] Z. Tőkei, K. Croes, and G. P. Beyer, "Reliability of copper low-*k* interconnects," Microelectron. Eng. Mater. Adv. Metall. 2009 **87**, 348–354 (2010).
[10] Y. Barbarin, K. Croes, P. Roussel, Y. Li, P. Verdonck, M. Baklanov, Z. Tőkei, and L. Zhao, "Reliability characteristics of thin porous low-K silica-based interconnect dielectrics," in *2013 IEEE International Reliability Physics Symposium (IRPS)* (IEEE, 2013), pp. 2F.3.1–2F.3.5.
[11] B. Cline, D. Prasad, E. Beyne, and O. Zografos, "Power from below: Buried interconnects will help save Moore's law," IEEE Spectrum **58**, 46–51 (2021).
[12] E. Beyne, A. Jourdain, and G. Beyer, "Nano-through silicon vias (nTSV) for backside power delivery networks (BSPDN)," in *2023 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits)* (IEEE, 2023), pp. 1–2.
[13] M. H. van der Veen, O. V. Pedreira, N. Jourdan, S. Park, H. Struyf, Z. Tőkei, C. L. Cerantes, F. Chen, X. Xie, Z. Wu, A. Jansen, J. Machillot, and A. Cockburn, "Low resistance Cu vias for 24 nm pitch and beyond," in *2022 IEEE International Interconnect Technology Conference (IITC)* (IEEE, 2022), pp. 129–131.
[14] O. V. Pedreira, V. Simons, M. van der Veen, I. Ciofi, S. Park, Z. Tőkei, K. Croes, S. Pethe, W. Lei, S. Hwang, Z. Wu, F. Chen, A. Jansen, J. Machillot, and A. Cockburn, "Reliability benchmark of various via prefill metals," in *2022 IEEE International Interconnect Technology Conference (IITC)* (IEEE, 2022), pp. 31–33.
[15] E. Ogawa, K.-D. Lee, V. Blaschke, and P. Ho, "Electromigration reliability issues in dual-damascene Cu interconnections," IEEE Trans. Reliab. **51**, 403–419 (2002).
[16] C.-K. Hu, L. Gignac, B. Baker, E. Liniger, R. Yu, and P. Flaitz, "Impact of Cu microstructure on electromigration reliability," in *2007 IEEE International Interconnect Technology Conference* (IEEE, 2007), pp. 93–95.
[17] H. Zahedmanesh, O. Varela Pedreira, C. Wilson, Z. Tőkei, and K. Croes, "Copper electromigration; prediction of scaling limits," in *Proceedings of IEEE 2019 International Interconnect Technology Conference (IITC)* (IEEE, 2019), pp. 3–5.
[18] E. Ogawa, J. McPherson, J. Rosal, K. Dickerson, T.-C. Chiu, L. Tsung, M. Jain, T. Bonifield, J. Ondrusek, and W. McKee, "Stress-induced voiding under vias

11 February 2026 10:29:35

© Author(s) 2025

connected to wide Cu metal leads," in *Proceedings of 40th Annual 2002 IEEE International Reliability Physics Symposium (Cat. No.02CH37320)* (IEEE, 2002), pp. 312–321.
[19]M. Kawano, T. Fukase, Y. Yamamoto, T. Ito, S. Yokogawa, H. Tsuda, Y. Kunimune, T. Saitoh, K. Ueno, and M. Sekine, "Stress relaxation in dual-damascene Cu interconnects to suppress stress-induced voiding," in *Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No.03TH8695)* (IEEE, 2003), pp. 210–212.
[20]T. Oshima, K. Hinode, H. Yamaguchi, H. Aoki, K. Torii, T. Saito, K. Ishikawa, J. Noguchi, M. Fukui, T. Nakamura, S. Uno, K. Tsugane, J. Murata, K. Kikushima, H. Sekisaka, E. Murakami, K. Okuyama, and T. Iwasaki, "Suppression of stress-induced voiding in copper interconnects," in *International Electron Devices Meeting: Technical Digest* (IEEE, 2002), pp. 757–760.
[21]S. Yokogawa and H. Tsuchiya, "Lifetime distribution analysis of stress-induced voiding based on void nucleation and growth in Cu/low- interconnects," IEEE Trans. Device Mater. Reliab. **13**, 272–276 (2013).
[22]S. Yokogawa, Y. Kakuhara, and H. Tsuchiya, "Joule heating effects on electromigration in Cu/low-interconnects," in *2009 IEEE International Reliability Physics Symposium* (IEEE, 2009), pp. 837–843.
[23]W. Ahn, Y.-P. Chen, and M. A. Alam, "An analytical transient joule heating model for an interconnect in a modern IC: Material selection (Cu, Co, Ru) and cooling strategies," in *2019 IEEE International Reliability Physics Symposium (IRPS)* (IEEE, 2019), pp. 1–6.
[24]M. Lofrano, O. V. Pedreira, I. Ciofi, H. Oprins, S. Park, and Z. Tokei, "Joule heating investigation for advanced interconnect schemes with airgaps," in *2021 IEEE International Interconnect Technology Conference (IITC)* (IEEE, 2021), pp. 1–3.
[25]X. Chang, H. Oprins, M. Lofrano, V. Cherman, B. Vermeersch, J. D. Fortuny, S. Park, Z. Tokei, and I. De Wolf, "Calibrated fast thermal calculation and experimental characterization of advanced BEOL stacks," in *2023 IEEE International Interconnect Technology Conference (IITC) and IEEE Materials for Advanced Metallization Conference (MAM)(IITC/MAM)* (IEEE, 2023), pp. 1–3.
[26]M. Lofrano, B. Vermeersch, H. Oprins, S. Park, and Z. Tokei, "Impact of FEOL cross-heating on the thermal performance of advanced BEOL," in *2022 21st IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (iTherm)* (IEEE, 2022), pp. 1–9.
[27]D. Coenen, K. Croes, A. Tsiara, H. Oprins, V. Simons, O. V. Pedreira, Y. Ban, J. Van Campenhout, and I. De Wolf, "Electromigration performance improvement of metal heaters for Si photonic ring modulators," IEEE Trans. Device Mater. Reliab. **22**, 417–423 (2022).
[28]D. Coenen, H. Oprins, M. Berciano, G. Muliuk, P. D. Heyn, J. V. Campenhout, and I. De Wolf, "Electro-absorption modulator thermo-optical self-heating analysis," J. Lightwave Technol. **41**, 6000–6006 (2023).
[29]O. V. Pedreira, Y. Ding, D. Coenen, P. Roussel, A. Saleh, V. Simons, H. Zahedmanesh, I. Ciofi, and K. Croes, "De-coupling thermo-migration from electromigration using a dedicated test structure," in *2024 IEEE International Reliability Physics Symposium (IRPS)* (IEEE, 2024), pp. 1–5.
[30]R. A. Oriani, "Thermomigration in solid metals," J. Phys. Chem. Solids **30**, 339–351 (1969).
[31]H. Ye, C. Basaran, and D. Hopkins, "Thermomigration in Pb-Sn solder joints under joule heating during electric current stressing," Appl. Phys. Lett. **82**(7), 1045–1047 (2003).
[32]C. Chen, H.-Y. Hsiao, Y.-W. Chang, F. Ouyang, and K. N. Tu, "Thermomigration in solder joints," Mater. Sci. Eng.: R: Rep. **73**, 85–100 (2012).
[33]S. Patra, D. Chen, and R. Geiger, "Reliability degradation with electrical, thermal and thermal gradient stress in interconnects," in *2013 IEEE International Symposium on Circuits and Systems (ISCAS)* (IEEE, 2013), pp. 1063–1066.
[34]C. M. Tan and A. Roy, "Investigation of the effect of temperature and stress gradients on accelerated EM test for Cu narrow interconnects," Thin Solid Films **504**, 288–293 (2006).
[35]H. Zahedmanesh and K. Croes, "Modelling stress evolution and voiding in advanced copper nano-interconnects under thermal gradients," Microelectron. Reliab. **111**, 113769 (2020).
[36]N. Somaiah and P. Kumar, "Inverse Blech length phenomenon in thin-film stripes," Phys. Rev. Appl. **10**, 054052 (2018).
[37]Z. Cui, X. Fan, Y. Zhang, S. Vollebregt, J. Fan, and G. Zhang, "Coupling model of electromigration and experimental verification—Part II: Impact of thermomigration," J. Mech. Phys. Solids **174**, 105256 (2023).
[38]Y. Ding, M. Lofrano, O. V. Pedreira, H. Zahedmanesh, K. Croes, and I. D. Wolf, "A combined modelling approach to design test structures to study thermomigration in Cu interconnects," Microelectron. Reliab. **138**, 114632 (2022).
[39]Y. Ding, O. V. Pedreira, M. Lofrano, H. Zahedmanesh, T. Chavez, H. Farr, I. De Wolf, and K. Croes, "Thermomigration-induced void formation in Cu-interconnects – assessment of main physical parameters," in *2023 IEEE International Reliability Physics Symposium (IRPS)* (IEEE, 2023), pp. 1–7.
[40]M. A. Korhonen, P. Bo/rgesen, K. N. Tu, and C.-Y. Li, "Stress evolution due to electromigration in confined metal lines," J. Appl. Phys. **73**, 3790–3799 (1993).
[41]A. S. Saleh, K. Croes, H. Ceric, I. De Wolf, and H. Zahedmanesh, "A framework for combined simulations of electromigration induced stress evolution, void nucleation, and its dynamics: Application to nano-interconnect reliability," J. Appl. Phys. **134**, 135102 (2023).
[42]H. Ceric, R. L. de Orio, J. Cervenka, and S. Selberherr, "Copper microstructure impact on evolution of electromigration induced voids," in *2009 International Conference on Simulation of Semiconductor Processes and Devices* (IEEE, 2009), pp. 1–4.
[43]M. E. Sarychev, Y. V. Zhitnikov, L. Borucki, C.-L. Liu, and T. M. Makhviladze, "General model for mechanical stress evolution during electromigration," J. Appl. Phys. **86**, 3068–3075 (1999).
[44]H. Ye, C. Basaran, and D. Hopkins, "Numerical simulation of stress evolution during electromigration in IC interconnect lines," IEEE Transactions on Components and Packaging Technologies **26**, 673–681 (2003).
[45]F. Yost, D. Amos, and A. Romig, "Stress-driven diffusive voiding of aluminum conductor lines," in *27th Annual Proceedings, International Reliability Physics Symposium* (IEEE, 1989), pp. 193–201.
[46]J. Black, "Electromigration failure modes in aluminum metallization for semiconductor devices," Proc. IEEE **57**, 1587–1594 (1969).
[47]J. Black, "Electromigration—a brief survey and some recent results," IEEE Trans. Electron Devices **16**, 338–347 (1969).
[48]J. D. Venables and R. G. Lye, "A statistical model for electromigration induced failure in thin film conductors," in *10th Reliability Physics Symposium* (IEEE, 1972), pp. 159–164.
[49]K. Croes, M. Lofrano, C. Wilson, L. Carbonell, Y. Siew, G. Beyer, and Z. Tőkei, "Study of void formation kinetics in Cu interconnects using local sense structures," in *2011 International Reliability Physics Symposium* (IEEE, 2011), pp. 3E.5.1–3E.5.7.
[50]R. Rosenberg and M. Ohring, "Void formation and growth during electromigration in thin films," J. Appl. Phys. **42**, 5671–5679 (1971).
[51]H. Wang, Z. Li, and J. Sun, "Effects of stress and temperature gradients on the evolution of void in metal interconnects driven by electric current and mechanical stress," Modell. Simul. Mater. Sci. Eng. **14**, 607 (2006).

11 February 2026 10:29:35

© Author(s) 2025