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ABSTRACT

Time-dependent conduction in epitaxial superlattice (SL) strain relief layers of GaN high electron mobility transistors on 200 mm engineered substrates with a poly-AlN core was observed and analyzed. This phenomenon occurs when the devices were operated with substrate bias of ~ -300 V for 10^1–10^3 s. The formation of the conduction path is related to trap-assisted leakage through the SLs on the engineered substrates; de-trapped carriers spread out vertically and laterally within a portion of the SLs, leading to a higher electrical field across the rest of the layers. This conduction mechanism may be hidden during the devices' normal operation (target 650–1200 V). It could lead to undesired effects during the operation of the devices, such as a time-dependent dynamic R_{on}. More resistive SLs will potentially reduce the impact of this phenomenon.

Gallium nitride (GaN) based high electron mobility transistors (HEMTs) are promising candidates for next-generation high-efficiency power converters,[1] with high breakdown voltage, low on-resistance, and fast switching speed facilitated by the two dimensional electron gas (2DEG) at the AlGaN/GaN heterojunction providing performance advantages over conventional silicon-based devices.[2,3] GaN-based epitaxial structures used for the production of commercial power electronic devices are typically grown on silicon substrates due to their low cost and good manufacturability.[4] Recently, GaN-based epitaxial structures for power devices have been grown on 200 mm engineered substrates with a polycrystalline aluminum nitride core from Qromis Substrate Technology (QST®).[5] QST® substrates possess a coefficient of thermal expansion close to that of the GaN epitaxial structure, enabling easier management of thermomechanical strain induced during the epitaxial growth processes, together with a Si crystalline starting layer to enable high quality GaN growth nucleation. Additionally, QST® substrates feature higher thermal conductivity than Si substrates,[6] which is beneficial for thermal management during high power operation. Nevertheless, heteroepitaxial GaN growth on either Si or QST® substrates requires the inclusion of epitaxial strain relief layers between the substrate and the active device layers for managing the effects of lattice mismatch and differences in thermal expansion coefficients.[7,8] A reversed stepped superlattice (RSSL) strain relief layer scheme has been demonstrated in GaN growth on QST® substrates, enabling growth of thick (7.5 μm) high quality GaN layers.[9] The RSSL strain relief structure design induces an alternating compressive and tensile stress, resulting in a very low wafer bow after epitaxy.[10] However, the electrical reliability and stability of the thick RSSL structure has not yet been fully assessed, which is important for enabling a manufacturable power device product. Here, we report a time-dependent conduction mechanism within the RSSL when devices are stressed with around -300 V (from -250 to -400 V) substrate bias. This conduction inside the superlattice layers will be hidden under normal operation of the devices (target voltage range for the buffer stacks is 650–1200 V). This time-dependent phenomenon could lead to undesired effects during the transient and off-state operation of the devices.

The device under test consists of a thick buffer (7.5 μm) on a 200 mm QST® substrate grown using metal organic chemical vapor

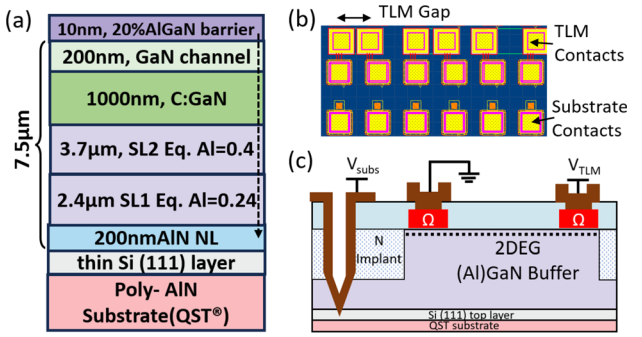

FIG. 1. (a) Schematic of the wafer stack. (b) Devices layout—squares on the top row are the TLMs. (c) The cross section of the fabricated devices.

deposition (MOCVD), shown in Fig. 1(a). The RSSL includes two SL layers with different equivalent Al compositions,[10] which are 24% for the lower SL1 (2.4 μm) and 44% for the upper SL2 (3.7 μm), respectively, and a 1000 nm C-doped GaN buffer. A 200 nm UID-GaN channel is deposited followed by a 10 nm $Al_{0.2}Ga_{0.8}N$ barrier layer for forming the 2DEG channel (more details of the RSSL are discussed in Ref. 10).

Transfer length method (TLM) structures were fabricated on the wafer, consisting of Ohmic contacts with spacings of 10, 18, and 100 μm, as shown in Fig. 1(b). Al-containing metal substrate contacts penetrating from the surface of the wafer to the conductive Si (111) layer fabricated using deep via processing were also included, as shown in Fig. 1(c). The 2DEG channels of the devices were electrically isolated using nitrogen implantation, and the Si (111) layer on the bottom of each device was electrically shorted together. These structures then enable substrate back biasing measurements, in which the conductivity between the TLM contacts is monitored as a function of bias applied to the backside of the epitaxial layer stack.

Details on the substrate back biasing technique are reported by Uren *et al.*[11–14] and have been used to gain insight into charge transport in the buffer layer in GaN-on-Si epitaxial structures. Substrate bias voltages up to -900 V were applied here for the 650 V-target GaN-on-QST HEMTs in order to analyze the carrier transportation in the strain relief layer, applied using a Keithley 2657A source meter, while a voltage of 0.1 V was applied between the TLM contacts and the corresponding channel current monitored by a Keithley 2636B source meter. Fluorinert was deposited on the surface of the wafer to prevent air breakdown destroying devices during testing. The background noise of the system was 1 fA.

Figure 2(a) demonstrates the normalized current between the two contacts of the TLM with 18 μm spacing, during bidirectional substrate ramps applied from 0 to −900 V to the back of the epitaxial structure, with various ramp rates. During fast sweep rate (9.2 V/s), a hysteresis was observed similar to that which has been reported in the GaN-on-Si HEMT.[11,12,15] The channel current is initially depleted following the ideal capacitive line (i.e., the entire epitaxy behaves as a dielectric, with current above or below this line indicative of positive or negative charge storage, respectively)[16] and then subsequently saturates due to band-to-band trap-assisted leakage in the UID-GaN.[11] This saturation occurs at lower voltages for slower ramp rates (1.4 and 0.7 V/s) as more time is provided for carriers to reach equilibrium.[11] However, there is an additional undulation feature in the normalized

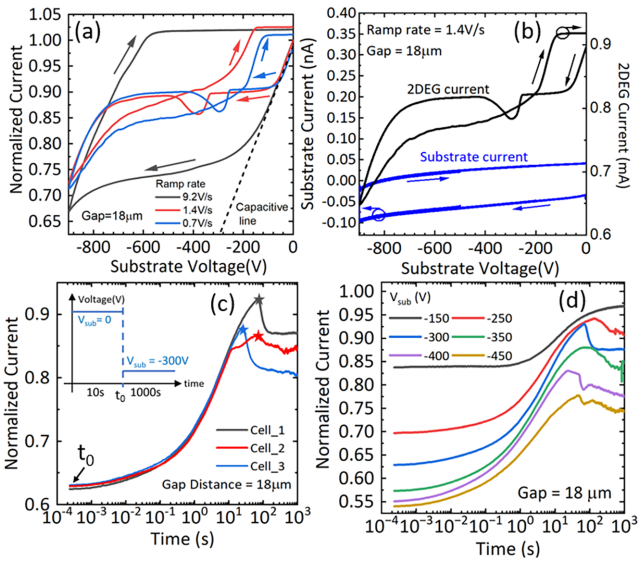

FIG. 2. (a) Normalized current between TLM contacts with 18 μm gap, as a function of substrate back bias, for different ramp rates. (b) The substrate leakage current during the substrate ramp. (c) Current transient under $V_{sub} = -300$ V for 1000 s on three identical devices with 18 μm gap on three different cells on the same wafer. (d) The current transient of devices with an 18 μm gap under different V_{sub} for 1000 s.

current profile observed at around $V_{sub} = -300$ V for slower ramp rates (1.4 and 0.7 V/s). Specifically, with V_{sub} sweeping toward more negative values, the normalized current drops significantly (by ~5%) before gradually increasing until it recovers back to the saturation level. Moreover, this current undulation occurs at lower voltages for the lower ramp rate of 0.7 V/s compared to 1.4 V/s. Figure 2(b) shows the substrate leakage current during the substrate ramp process. The very low substrate leakage current (50–100 pA) indicates that the measured channel current drop is not due to leakage through the substrate.

Figure 2(c) demonstrates the current transients at constant substrate stress $V_{sub} = -300$ V for 1000 s on three nominally identical TLM structures with 18 μm spacing at three nominally identical cells on the same wafer. The current value is normalized to the current without applied substrate stress. The increase in the current over ~1 s is attributed to the band-to-band leakage through the UID-GaN, similar to the current transient in GaN-on-Si devices.[16] Significant current reduction then occurs on a 10–100 s timescale, which corresponds to the undulation feature in Fig. 2(a). The onset time of the current reduction and its magnitude in nominally identical cells exhibit a large variation even with the same contact spacing.

Figure 2(d) shows the impact of the substrate stress voltage on the current reduction mentioned above for current transients in the same device (contact spacing = 18 μm). The normalized current starts from different current levels under different negative substrate bias as expected. The following current reduction occurs on a 10^1–10^3 s timescale when V_{sub} is more negative than about −250 V. The onset time of the current reduction did not show any obvious dependence on the applied substrate bias, for $V_{sub} = -250$ to −450 V.

The relationship between the current reduction mentioned earlier and the gap distances is shown in Fig. 3. The onset time of the current

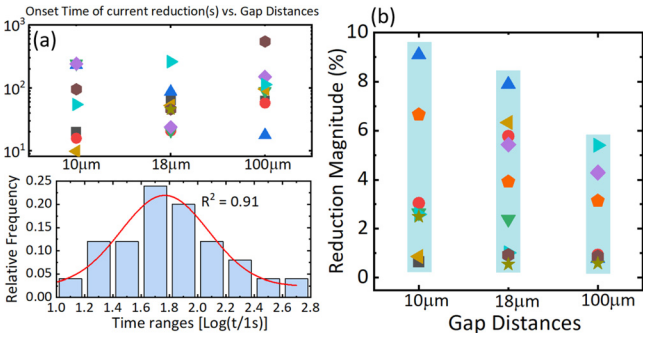

FIG. 3. (a) The onset time values of the current reduction in the current transient under $V_{sub} = -300$ V for 1000 s [the stars at Fig. 2(c)] from ten groups of devices located at the different parts of the wafer with all gap spacings. The figure shows the histogram of these values. (b) The current reduction magnitude (%) of these devices during this undulation.

reduction under $V_{sub} = -300$ V stress [stars in Fig. 2(c)] for multiple devices in different gap spacings is collected and shown in Fig. 3(a). The onset time of the current reduction of these devices is distributed within 10^1–10^3 s randomly, which indicates they are not strongly dependent on the contact spacings. The relative frequency (counts/total numbers) of these time values is demonstrated as histogram in Fig. 3(a), which follows a lognormal distribution around a central value of ∼100 s. Figure 3(b) demonstrates the magnitude of the 2DEG current reduction of these devices. The range of current reduction magnitude decreases as the contact gap distance increases, from 0.5%–10% for 10 μm to 0.8%–5% for 100 μm.

We make three observations on the undulation: (i) it occurs at a lower voltage under a lower sweep rate [Fig. 2(a)]; (ii) it is repeatable [results shown in Figs. 2(a) and 3 are on the same devices]; (iii) the onset time of the undulation in the transients is not strongly dependent on contact spacings and follows a lognormal distribution with center around ∼100 s [Fig. 3(a)]. This time-dependent, statistical nature of the current undulation coupled with its recoverable properties indicates a trap-driven conduction mechanism, rather than a catastrophic breakdown such as via dislocations[17–19] or physical SL relaxation.

To explain the results earlier, the status of the device when the undulation feature occurs must first be understood. Charge transportation inside the GaN HEMT epitaxial stack during substrate biasing is discussed in Refs. 11–14 and 16. Figure 4 shows the band diagrams of the stack along the cutline in Fig. 1(a) at different stages during the downward sweep of the substrate ramp. Saturation of the channel current during the downward sweep of the substrate bias measurement indicates the presence of band-to-band leakage from the 2DEG through the UID-GaN (channel) layer [Fig. 4(a)]. Holes from the UID-GaN leakage accumulate at the bottom of the GaN:C layer, maintaining a constant field in the UID-GaN channel.

When the undulation occurs (Figs. 2 and 3) within the voltage range under which this current saturation (∼−300 V) is typically observed, it indicates that the previous equilibrium is broken due to an increased voltage drop across the channel layer, causing the charges to re-distribute again. From Fig. 2(a), the fact that the channel current returns to the pre-undulation saturation level after the undulation indicates the field in the UID-GaN and GaN layers is also the same; however, the field distribution within the SL layers can be different.

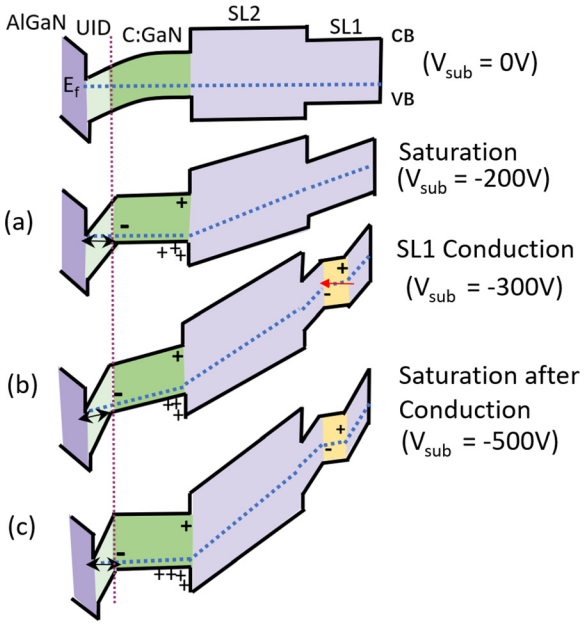

FIG. 4. Band diagram along the dashed line in Fig. 1(a) under the different bias conditions. The double arrow across UID-GaN represents the band-to-band leakage. The red arrow represents the conduction mechanism inside SLs.

Additionally, the low substrate leakage current and the absence of any current step [Fig. 2(b)] tend to exclude electron injection from the substrate.

Hence, we propose that the undulation is the result of the formation of an internal vertical conduction path, which shorts out a portion of the structure. The position where the conduction path is generated is inferred to be within the strain relief layers (SL1 and SL2). The reason for the undulation is most likely when part of a SL becomes conductive due to an internal leakage path that forms via trap-assisted tunneling between traps within a portion of a SL [evidenced by the larger onset time (∼100 s)]. As shown in Fig. 4(b), the hopping electrons cause a separation of charge inside the SLs forming a dipole and reducing the local electrical field. This leads to an increase in electrical field in the rest of the device layers, which, in turn, causes the 2DEG to be partly depleted. The device recovers when the charge flow through the UID-GaN channel accumulates a positive charge in the GaN:C that screens the increased SL field, and the current returns to its saturation value [Fig. 4(c)]. During the fastest reverse scan of the substrate ramp, the stored positive charge at the bottom of the C:GaN is neutralized by electrons flowing across the 2DEG/channel junction, which becomes forward biased. This screens the 2DEG from any rapid changes in field within the SLs.[11] Thus, no undulation related effects are visible during this reverse scan. For a slower reverse ramp rate, the two-stage saturation is due to band-to-band hole leakage across the UID-GaN layer, allowing the stored hole density to follow the ramp, followed by the lower field suppressing the hole leakage and then showing the same behavior as the fast reverse sweep.[16]

The conduction path suggested earlier reduces the electrically effective SL thickness and may lead to a time-dependent dynamic R_{on} during the switching of the devices. This conduction may occur in

either SL1 and/or SL2, where either becoming conductive will give rise to the change of electric field in the GaN channel layer. Figures 4(b) and 4(c) show an example of the case that this conduction happens inside SL1. Since the phenomenon appears to be repeatable and reversible, it seems that the local breakdown does not lead to any damage, so presumably the dipole discharges when the bias is removed. It is possible that the breakdown is related to the negative-differential-resistance associated with filamentary conduction previously observed in heavily carbon doped GaN.[20] However, the mechanism here is likely distinct since there is no significant vertical conduction associated with the breakdown in this case.

In the proposed model, the magnitude of the current reduction is related to the vertical thickness of that part of the SL, which becomes conductive, and the lateral extent of that conducting region. Figure 5(a) illustrates a mechanism by which the dipole sheet could occur. A localized vertical leakage path would open within one of the SLs, perhaps following a dislocation. After this, lateral charge transport could occur at the top (negative charge) or bottom (positive charge) of an SL barrier. It is already well known that the heterojunction barriers within the buffer are susceptible to lateral 2DEG and 2DHG conduction despite being heavily compensation doped with carbon,[10,15,21,22] and hence, it is quite reasonable that a localized injection of positive or negative charge should spread laterally driven by the lateral component of the high vertical field at the edge of the dipole region. The fact that the undulation takes several seconds to form [Figs. 2(a) and 2(c)] would then be consistent with a rapid vertical leakage followed by a slow lateral transport across the area of the TLM structure.

If we assume that the dipole region extends across the entire area of the TLM structure (i.e., up to $\sim 100 \times 100\ \mu$m for the studied structures), and that there is full screening of the applied vertical field within the dipole, then the magnitude of the change in current associated with the undulation can be used to estimate the minimum thickness of the dipole layer.

As shown in Fig. 5(b), if there were no screening in the C:GaN layer, the normalized 2DEG current under substrate ramp should follow the blue ideal capacitive line.[11,16] When the undulation begins, the capacitive line will jump to the red one due to the change of the effective stack thickness, specifically the conductive thickness inside the SL. The difference between the two capacitive lines under $V_{sub} = -300$ V (A–B) indicates the magnitude of the 2DEG current drop caused by

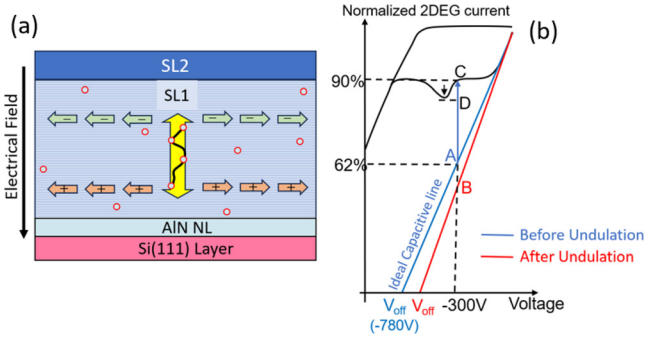

FIG. 5. (a) The diagram of the route of the conduction path inside SLs. The red circles represent the defect/traps inside SLs. (b) The diagram of the ideal capacitive lines before and after the undulation. The pitch-off voltage of the stack before undulation is −780 V calculated by $V_{TB} = -qn_{2deg}/C_{tot}$.[11]

the change of the SL thickness if we regard the stack as an ideal capacitor. Arrow AC indicates the charge relaxation process corresponding to the current transient in Fig. 2(c). We can exclude this relaxation process within the C:GaN when calculating the conductive thickness inside SL because this long timescale process will not impact the effect of sudden increased electric field. Thus, the magnitude of the undulation (C–D) is actually equal to the magnitude of line segment AB. Through a pure capacitance model, the conductive thickness can be calculated by

$$\Delta d = \varepsilon \cdot \left(\frac{1}{C_{\text{before}}} - \frac{1}{C_{\text{After}}}\right) = \frac{\varepsilon \cdot V}{Q_0} \cdot \left(\frac{1}{1-\eta_A} - \frac{1}{1-\eta_B}\right), \quad (1)$$

where C_{before} and C_{after} are the total capacitance of the stack before and after undulation, respectively, $Q_0 = qn_{2\text{deg}}$ is the unbiased 2DEG charge, and η_A and η_B are the percentage of the 2DEG density at points A and B shown in Fig. 5(b), respectively. By filling in the experimental values into the equation, we find that a ∼3.5% magnitude of current corresponds to ∼600 nm thickness conductive leakage path inside the SL. This analytic model was validated by TCAD simulation of the effect on the substrate ramp characteristic of electrically shorting a portion of the SL. This was done by adding a high density of shallow acceptors across the entire width of the device. This showed a reduction of current in the saturated part of the characteristic that was consistent with the result from Eq. (1).

This model has assumed that the induced dipole fully screens the field within the layer and extends across the entire TLM. However, equally likely is that the screening is not complete or extends only partially across the TLM. The latter has experimental support in Fig. 3(b), where the magnitude of the undulation appears to be somewhat smaller for larger TLM structures. Thus, a more plausible scenario for the vertical leakage path is that leakage is limited by the change in structure of the RSSL, with the leakage path occurring through a larger thickness or even the entire thickness of either SL1 or SL2. The dipole charges may then not be sufficient to fully screen the field within the affected SL, explaining why the magnitude is less than would be predicted from Eq. (1) using the full SL thickness.

We reported a conduction mechanism within the reversed stepped superlattice layers on 200 mm engineered substrates. A trap-assisted leakage inside the SLs formed when the device was operating around ∼300 V, leading to a reduction of electrical effective SL thickness. The conduction path is inside the SL layer, occurs locally, and then allows charge to spread out laterally at an SL barrier interface. The effect of this conduction path will potentially cause a change of the device capacitance, giving rise to undesired effects during the transient operation of the devices, such as a time-dependent dynamic R_{on} at specific voltage and overstressing of the buffer. This conduction mechanism will be hidden during the normal devices' operation. More optimization of resistance of thicker SLs grown using RSSL scheme may benefit GaN HEMTs on the engineered substrates.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Zequan Chen: Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – original draft (equal). **Michael J. Uren:** Formal analysis (equal); Investigation (equal); Methodology (equal); Supervision (equal); Writing – review & editing (equal). **Peng Huang:** Formal analysis (equal); Investigation (equal). **Indraneel Sanyal:** Formal analysis (equal); Investigation (equal). **Matthew D. Smith:** Formal analysis (equal); Investigation (equal); Writing – review & editing (equal). **Anurag Vohra:** Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Sujit Kumar:** Investigation (equal); Methodology (equal). **Stefaan Decoutere:** Funding acquisition (equal); Resources (equal); Supervision (equal). **Benoit Bakeroot:** Formal analysis (equal); Investigation (equal); Project administration (lead); Writing – review & editing (equal). **Martin Kuball:** Formal analysis (equal); Funding acquisition (equal); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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