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Comparison of GaN Enhancement Mode Transistor Performance With Integrated and External Driver

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ABSTRACT

GaN components allow to reduce power losses as the lower specific on-resistance and higher switching speeds reduce both the conduction and switching loss. However, parasitics in the gate loop cause ringing which endangers the component. To counteract these problems the switching speed is lowered renouncing part of the components superior performance. A possible way to avoid gate loop parasitics and make circuit design less challenging is integrating the driver in the same package with the GaN transistor. In this paper the performance of an integrated driver with enhancement mode GaN half-bridge that is monolithically integrated using IMEC GaN-on-SOI will be tested in a synchronous boost converter setup. Converter efficiency and switching waveforms will be reported together with a comparison to a GaN half-bridge with external drivers. The converter is tested at input voltages up to 50 V and powers up to 100 W. Package temperature measurements are included to estimate the influence of the temperature dependent on-resistance on the results. At the end of the paper, a sensitivity analysis is conducted to quantify the behaviour of the losses in function of different input parameters including a measurement at switching frequencies up to 1MHz.

1. Introduction

In power electronics, there is an ongoing trend of reducing the size of power converters as this opens a lot of new application possibilities. A way to increase the power density, is augmenting the switching frequency, as this allows to reduce the size of passive components. Unfortunately, this inevitably leads to higher power dissipation, as part of the losses in the transistor are proportional to the switching frequency. To still enable higher frequencies while maintaining acceptable amounts of power dissipation, components with lower losses are developed. The familiar silicon devices have a rich past of great improvements but are reaching the theoretical limits of the materials involved. GaN based devices are an alternative as their theoretical losses are a lot smaller (Lee et al., 2019). Although the characteristics are promising, these components do not come without new challenges. The enhancement mode GaN transistor is a normally-off device but the threshold voltage is relatively low and the maximum gate voltage is close to the recommended gate drive voltage. This means that even for low amounts of ringing, false turn-on can occur and that the component is easily damaged by overshoots. These problems originate from oscillations in the gate signal that are caused by a resonance between the gate loop inductance and the gate capacitance. To protect the GaN component, damping is added in the form of extra resistance to limit these oscillations and overshoots. However, this slows down the switching speed of the component, increasing the losses, renouncing part of the components superior performance. The smaller this resistance can be made, the larger the expected performance of the GaN component. The driver plays an important role, its design should minimize overshoots and supply a stable gate voltage at high speeds. Also the PCB design is crucial as the placement of driver with respect to the transistor and the routing determines the extra parasitics that are added to the gate loop. A possible way to limit the parasitics in the gate loop and reduce the pressure on PCB design, is to integrate the driver and transistor in the same package (Dalla Vecchia et al., 2017; Lorenz et al., 2018; Trescases et al., 2020; Vecchia et al., 2019).

The concept of driver integration is already extensively shared in literature. For example, a GaN half-bridge with integrated driver is realised in Ujita et al. (2016) using GaN-on-Si. Its functionality is demon-

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strated using a synchronous buck converter from 12 V to 1.5 V. In Cui et al. (2019) another buck converter is realized, using the same technology with a maximum input voltage of 25 V. The paper notes discrepancies between the calculated and measured results at these higher input voltages. This is a consequence of the GaN-on-Si technology which does not allow to use high voltages as it is not possible to isolate the substrate of each transistor. Capacitive coupling through this common substrate significantly increases gate-charge at high operation voltages in half-bridges and increases the threshold voltage when the bias voltage becomes larger, a phenomena described in Moench et al. (2017). To address this issue it is possible to package the power GaN transistors separately. A single transistor with integrated driver is presented in Zaman et al. (2020) with voltage capabilities up to 650 V. To ease manufacturing, the driver is often implemented on a separate die which is packaged together with the power transistor. The connections are made using bond wires which already improves performance as shown in Chen et al. (2019); Seidel and Wicht (2018). In Li et al. (2017) the GaN-on-Si-on-Insulator (GaN-on-SOI) technology is demonstrated as a solution for the common substrate coupling. Here the two power transistors substrates in a half-bridge are isolated from each other using trench etching through the GaN and Si towards the SiO_2 insulation layer, isolating the two switches. A device with voltage capabilities up to 200 V is achieved. This research was based on the developments in material science concerning GaN-on-SOI which is still ongoing (Jiang et al., 2013; Lee et al., 2016; Steckl et al., 1997; Tripathy et al., 2006). A follow up in Yamashita et al. (2018) shows a GaN enhancement mode transistor with integrated driver and (Li et al., 2019b) presents the possibilities of GaN-on-SOI as a platform for integrated all-GaN ICs. Tang et al. (2018) also shows an integrated driver with transistor capabilities up to 300 V and (Noike et al., 2021) a GaN transistor with integrated driver in an asynchronous buck converter. Jiang et al. (2021) shows an integrated 200 V half bridge with integrated drivers using dv/dt control. A comparison between the performance of GaN-on-Si and GaN-on-SOI is done in Moench et al. (2021). Qromis Substrate Technology (QST®) has developed a commercially 200 mm engineered substrate, this technology is given the commercial name GaN-on-QST®. In Li et al. (2019a) a 200 V half-bridge with integrated drivers is presented using this technology. This driver is a voltage source driver, a current source version of this driver is already presented in Nagao et al. (2019). Recently (Li et al., 2020b) achieved power devices that are able to block 650 V using GaN-on-QST®.

To the authors knowledge no test results of GaN half-bridges with on chip drivers using GaN-on-SOI or GaN-on-QST® on practical converter circuits for realistic power levels (more than a few watts) were available. Because of this it was not possible to make a definitive statement on the state of the art and usability of the technology. To meet this research gap, the performance of an improved version of the GaN half-bridge with integrated driver (GaNint) presented in Yamashita et al. (2018) was evaluated. The first insights gained from this were already shared in Deckers et al. (2020). Here GaNint was compared to the performance of a similar GaN half-bridge (GaNbridge) with external commercial drivers. In both cases, half-bridge switches are made with the same IMEC GaN-on-SOI technology. The recorded efficiency of the 25 V synchronous boost converter using GaNint was less than the ones with GaNbridge, 95.3 % against 97.2 % and 96.5 % respectively. Further analysis showed that the switching behaviour of GaNint did perform better as it achieved switching speeds up to 16 ns faster than the commercial drivers. The main cause of this discrepancy between the converter efficiency results and the switching performance was placed by the temperature dependent on-resistance. This paper will report on the case temperature and gate to source voltage waveforms to further establish this hypothesis while also looking deeper into the disadvantages of integration. Together with the knowledge of the used technology and the structure of the chip, this will lead to a more nuanced conclusion. In addition to this, a sensitivity analysis to the converter input parameters will be conducted to make the results more general and the efficiency for switching frequencies up to 1 MHz will be shown.

The central research question of this paper can be formulated as: How does the performance of a GaN half-bridge with fully integrated drivers compares to the same practical setup with external commercial drivers in different operation areas?

The paper is organized as follows. First, the hypothesis on the relative performance of an integrated driver compared to external drivers will be constructed in section 2. All the experiments in this paper are conducted with the aim to quantify these statements. For the actual comparison a synchronous boost converter topology is chosen. To distinguish the normal converter behaviour from the influence of driver integration, the functioning of a synchronous boost converter will be discussed focussing on the switching instants in section 3. Then, the experimental setup will be discussed in section 4 after which the experimental results are shown in section 5. This includes the efficiency with temperature and a sensitivity analysis showing the influence of the converter input parameters. Section 6 concludes this paper.

2. Hypotheses

Integrating the driver onto the same die as the power transistor is seen as the next step in the technology development. However, this step is not necessarily beneficial as integration might also cause additional effects deteriorating the performance. This section aims to cover the most important phenomena playing. The experiments in this paper will try to quantify these statements, showing the readiness of this technology.

2.1. Positive effect of integration

The main hypothesis poses that the integration of both power switches and drivers will lead to less parasitic inductance in between the two. This would allow for higher switching speeds and less damping in the from of gate resistance as the problematic ringing is caused by the inductance that is now eliminated. This positively influences the switching losses as these are dependent on the voltage and current transition time which are limited by the gate resistance. This allows to raise the switching frequency without leading to unacceptable switching losses.

2.2. Negative side effects of integration

The main goal of the GaN-on-SOI technology used for integrating the driver is to avoid the backgating effect which normally occurs with integrated switches operating at different voltage levels. In this case the common substrate is connected to the source of Q1 causing a positive voltage between the bulk and source of Q2, leading to significant $R_{DS\ on}$ degradation. To avoid this, the SOI substrate consists of a Si handling wafer, a SiO_2 buried layer and a Si top layer on which the classical GaN structure can be build. To isolate the local substrate, an oxide filled trench is etched until the SiO_2 buried oxide layer. After this, the now isolated substrate is connected with a deep Si contact to the source of its respective switch using back-end power metal aluminium (Li et al., 2017). The carrier Si substrate is left floating. This completely isolates the switches and their respective substrates avoiding the backgating effect. However, some of the integration and substrate related effects will remain present. The extra oxide layer in between the handling wafer and the GaN structure creates capacitive effects. This parasitic substrate capacitance (sometimes called oxide capacitance) can cause extra capacitance losses (Moench et al., 2021). This will be the main negative effect of integration. The experiments in the next section will need to determine the severity and magnitude of these effects.

The inclusion of the driver onto the same die and into the same package means that also the power dissipation of the driver will contribute to the temperature increase in the power transistors. This is a disadvantage as GaN has a temperature dependent on-resistance, causing higher temperatures to lead to higher losses (Magnani et al., 2021).

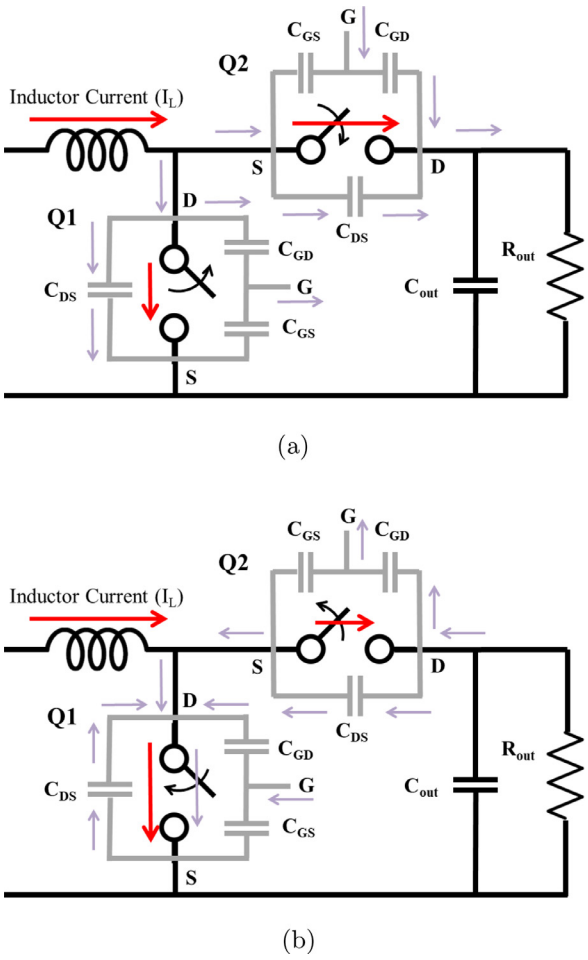


Fig. 1. Graphical representation of the self and forced commutation in a synchronous boost converter.

3. Synchronous boost converter circuit behaviour

The main aim of this paper is to compare the performance of a novel GaN device with integrated drivers to the more classical GaN devices with external drivers. For this comparison a synchronous boost converter topology is used. This is a basic power electronic circuit of which the fundamentals are well understood. However, here emphasis is placed upon the two commutations when using GaN components. This will make it possible to distinguish between phenomena caused by the circuit and by integration effects during the experiments. A detailed analytical loss calculation method for buck converters can be found in ROHM Co (2016).

3.1. Commutations

The transistor on the low side of the synchronous boost converter is called the *control switch or switching transistor* (Q1), the high side transistor is called the *synchronous rectifier transistor* (Q2). Q1 and Q2 are modelled as ideal switches with parasitic capacitances as shown on Fig. 1. The important capacitance here is the output capacitance C_{OSS} responsible for the output capacitance loss which is the sum of C_{DS} and C_{GD}. In Fig. 1a Q1 opens and Q2 closes. The inductor current (I_L) stops flowing through Q1 and starts conducting through Q2, while it is still turned off ($V_{GS} = 0$). This happens during the dead time in between the Q1 turn-off and Q2 turn-on, via the reverse conduction phenomenon. The current I_L charges C_{OSS} of Q1 and discharges C_{OSS} of Q2, bringing the switching node in between Q1 and Q2 naturally to the output voltage as I_L (thick arrows) flows in the same direction as the capacitance currents (thin arrows). This way the capacitance currents do not flow through the switches meaning they do not cause conduction losses. When Q2 turns on, there is still a small negative voltage present over the transistor due to the reverse conduction. For this reason, the transition is not completely a natural commutation (transition without switching losses) as the voltage over the transistor is not completely zero, it will be called self commutation to avoid confusion. In Fig. 1b Q1 turns on while Q2 turns off. I_L (thick arrows) flows in the opposite direction as the C_{OSS} currents (thin arrows). This means that the capacitance currents of both switches will flow through Q1 and cause conduction losses. These losses will be called output capacitance losses to distinguish them from the conduction losses caused by the load current. This transition is called a forced commutation. An overview of the different commutations in GaN components is given in Table 1 Lidow et al. (2014).

Table 1
Overview of the different commutations Lidow et al. (2014).

	Control switch (Q1)		Synchronous rectifier (Q2)	
	Turn off	Turn on	Turn on	Turn off
Commutation	Self	Forced	Reverse conduction	Reverse conduction
Output capacitance loss	No	Yes	No	In control switch (Q1)
Reverse conduction loss	No	No	Yes	Yes

3.2. Theoretical waveforms

Fig. 2 shows the expected theoretical profiles based on the transistor commutations from the previous paragraph. A current flow from drain to source is defined as positive. A complete switching cycle of the converter is divided into four regions: t_1, t_2, t_3 and t_4. In region t_1 Q1 is in the open position (blocked) and Q2 is closed (conducting). Current is flowing through Q2 towards C_{out} causing the output voltage to rise slightly. In t_2, Q2 is opened while Q1 remains open as well. The current I_L keeps flowing, forcing Q2 in reverse conduction. This reverse current flow from source to drain causes a small negative voltage drop over the transistor. This voltage transition is only minor, resulting in no Miller plateau in the gate profile and a small switching loss in Q2. As the total voltage over the two transistors is always equal to the output voltage, this small voltage drop causes a rise in the voltage over Q1. This slight change in voltage creates a small charge current due to the parasitic capacitances as can be seen in the current profile which is often neglected. In region t_3, Q1 is closed, stopping the reverse conduction through Q2 and forcing the node between the two transistors to zero. This causes a large charge current due to C_{OSS} as can be seen in the drain to source current profile together with a Miller plateau in the gate profile and larger switching losses. In region t_4, Q2 remains open and Q1 is opened again as well. I_L naturally charges the switching node to the output voltage with a speed dependent on the magnitude of this current and C_{OSS}. For Q2 this is still a hard switching transition causing a Miller plateau and switching losses. When the output voltage is reached, the voltage drop due to reverse conduction through Q2 is visible. Closing Q2 again leads to region t_1 where the whole process is repeated. The voltage transition in Q2 is small leading to low switching losses and no Miller plateau with only a small charge current.

This theoretical observation leads to a few conclusions which will be from importance in the sensitivity analysis of section 5.

Load current

Firstly, there is the influence of the load current. During self commutation, the switching speed is reversely dependent on the load current as it discharges C_{OSS}. In contrast, the forced commutation will slow down less than linearly with the rise of this current because of the change in plateau voltage at the gate. The switching loss during self commutation

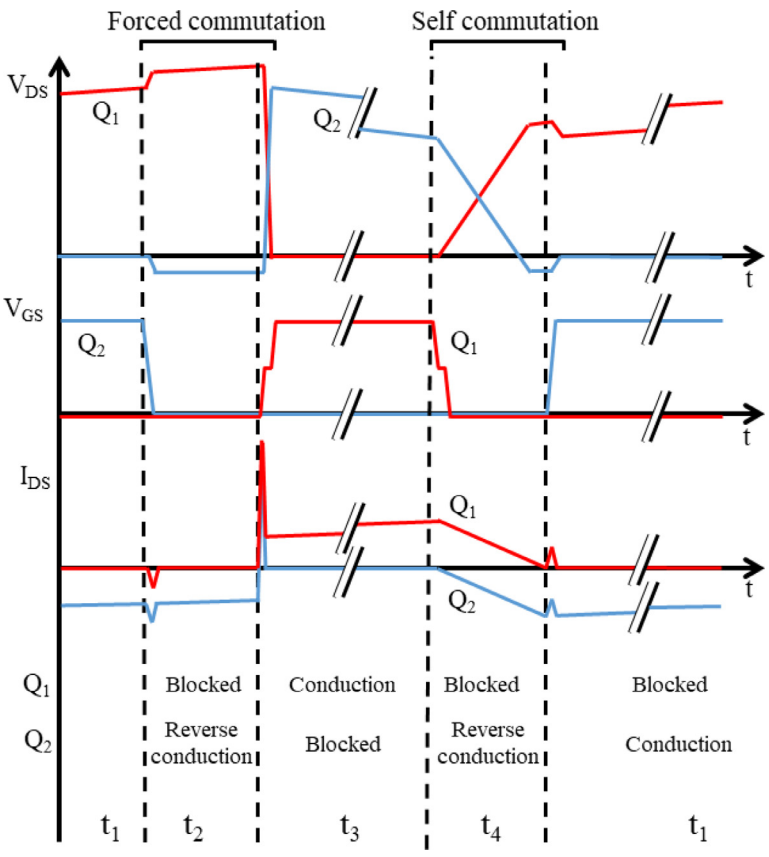


Fig. 2. Theoretical voltage and current profiles of the control switch Q1 and synchronous rectifier Q2 transistor.

(a) Board 1: Imec integrated driver (GaNint).

(b) Board 2: Texas Instruments LMG1210RVRT driver (GaNbridge and TI).

(c) Board 3: Silicon Labs Si827GB-IS1 driver (GaNbridge and SiL).

Fig. 3. Pictures of the three boards used in the experiments. All three boards are synchronous boost converters with the same components except for the driver (Deckers et al., 2020).

will remain unchanged while the switching loss during forced commutation rises in a more than linear fashion with an increasing load current.

Dead time

Secondly this also has as a consequence that the ideal dead time is dependent on the load current as it changes the switching speed during self commutation. It should be as short as possible to avoid excess reverse conduction losses but long enough to allow completion of the self commutation.

Drain to source voltage

Finally the voltage level might also influence the efficiency of the boost converter. The switching time increases in a less that linear way with the drain to source voltage V_{DS} during forced commutation as it changes the length of the Miller plateau. During self commutation, the switching time will increase linearly with V_{DS} as the charge and discharge current is constant. The switching losses are linearly dependent on the switching time and the drain to source voltage V_{DS}. The forced commutation losses will thus rise more than linear and the self commutation losses in a quadratic way with V_{DS}.

These conclusions drawn from the theoretical functioning of the circuit give an overview of how the performance changes depending on the input parameters. They will be used to analyse the results from the sensitivity analysis in chapter 5.

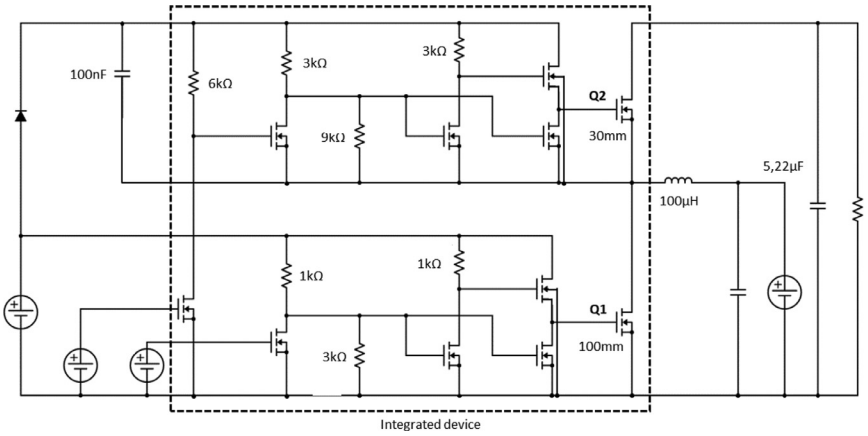


Fig. 4. Schematic of the integrated driver and half bridge.

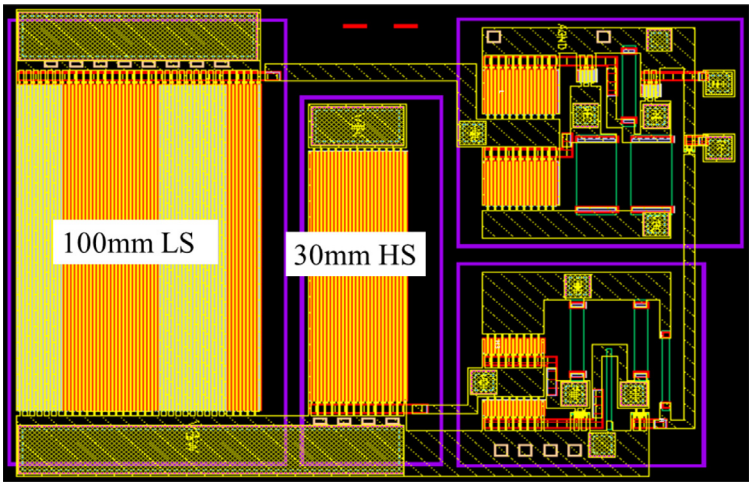


Fig. 5. Internal layout of the integrated driver (Deckers et al., 2020).

Table 2
Parameters of the boost converter.

Parameter	Symbol	Value	Unit
Output capacitance	C	5.22	μF
Main inductance	L	100	μH
Turn-on gate resistance	$R_{turn-on}$	20	Ω
Turn-off gate resistance	$R_{turn-off}$	10	Ω

4. Experimental setup

In this section the experimental setup will be presented. First the PCBs and components will be shown after which the performed experiments will be discussed.

4.1. Experimental boards

A performance comparison will be done between a GaN half-bridge with integrated and a GaN half-bridge with external drivers. To this end two GaN half-bridges are available, one GaN-on-SOI with integrated drivers (GaNint) and a very similar GaN-on-SOI without drivers (GaN-bridge). For the experiments three different synchronous boost converter boards are developed. One board will house the component of interest GaNint, the other two GaNbridge with a LMG1210RVRT (TI) driver and a Si8273GB-IS1 (SiL) driver as commercial references respectively. The parameters of the constructed boost converter are given in Table 2. The gate resistance values are only applicable to the external drivers as the internal gate resistance of GaNint is completely eliminated.

The remainder of this subsection will discuss the used components more in detail together with the resulting PCBs shown in Fig. 3. The selection of the external gate resistance is also treated separately in what follows as this is a very important value for the resulting performance of the circuits.

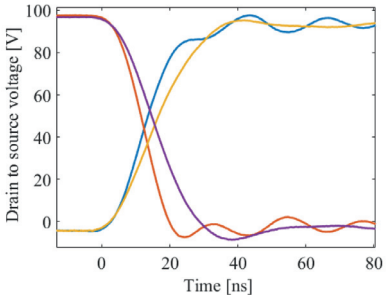
4.1.1. GaNint

In Fig. 4 the internal schematic of the GaN-on-SOI driver with GaN half-bridge is shown. The main difference with the circuit presented in Li et al. (2019a) is the presence of a level shifter allowing to provide the high side signal referenced to the same ground as the low side signal and the low side driver power. The sizing of the power transistors and resistors is a little different in order to lower the losses, the values are given in the figure.

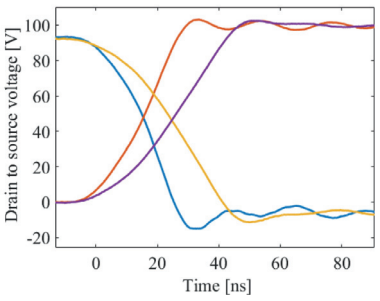
In the layout of the integrated device is shown in Fig. 5, four pockets are formed using trench etching indicated with purple boxes. This means that Q2, Q1, driver of Q2 and driver of Q1 are isolated from the carrier substrate and from each other. The substrate of each power transistor is connected to its source using vias together with the substrate of the respective drivers. The carrier Si substrate is left floating. This type of termination is typical for GaN-on-SOI (Moench et al., 2021).

The used push-pull driver inevitably has a threshold voltage drop in the pull-up transistor. Because of this, a supply voltage of 8 V will be used to reach the wanted 5 V at the gate. The high side power input will be connected to the same supply via a bootstrap diode. This will introduce a small voltage drop but this effect is only limited with the use of a Schottky diode.

The component is packaged in a Dual In Line (DIL) package with exposed bare die. The thermal characteristics of these prototype pack-



(a) Forced commutation, Q1 turns on and Q2 turns off.



(b) Self commutation, Q1 turns off and Q2 turns on.

Fig. 6. Comparison of the drain to source waveforms of the Texas Instruments driver at a turn-on turn-off pair of 10 Ω, 3 Ω and 20 Ω, 10 Ω. The measurements are done at an input voltage of 50 V and an input current of 0.7 A. The switching frequency is 200 kHz, the dead time is 200 ns and the duty cycle is 0.5.

ages are poor, leading to high temperatures even for limited amounts of power dissipation.

4.1.2. GaNbridge

To have a fair comparison, the GaN transistors used in GaNbridge are very similar as those used in GaNint. The same substrate and isolation technique is used to isolate the low and high side switch however, no integrated drivers are present allowing the use of external drivers. The main difference with GaNint is the high side switch width which is 48 mm and 30 mm respectively, causing a minor difference in $R_{DS,on}$ which is larger for GaNint. The low side switch width is with 100 mm the same for both.

GaNbridge is packaged in an UTAC package which is a custom designed package comparable to a 24L HSOP package. A thermal pad is provided at the bottom of the package to aid with heat evacuation.

4.1.3. TI

LMG1210RVRT is a half bridge driver with an isolated high side. A Low Dropout regulator (LDO) makes sure that the ideal 5 V is supplied to the gate when an input voltage higher than 6 V is used. A separate pin for the bootstrap diode is foreseen which allows to prevent overcharging to avoid excessive losses. A high Common Mode Transient Immunity (CMTI) of 300 V/ns is indicated on the datasheet and the expected rise and fall time are 3.5 ns and 2.3 ns respectively with a load capacitance of 1 nF. Next to an Under Voltage Lockout (UVLO) of 4 V the device also has an over-temperature protection. The high and low side output can be interrupted separately when a respective side crosses the temperature limit of 150 degrees Celsius.

The driver is packaged in a 19-Pin WQFN package allowing for a minimum of parasitic inductance. Two thermal pads at the bottom aid in the evacuation of heat.

During the experiments a logic supply of 5 V is used together with a gate drive supply of 8 V to allow the LDO to precisely regulate the voltage.

4.1.4. SiL

The Si8273GB-IS1 is a fully isolated high-side low-side driver with high transient immunity (200 V/ns $CMTI$). Also here the high side supply is connected with a bootstrap diode to the low side supply, a small voltage drop is thus expected. A load capacitance of 200 pF gives an expected rise time of 10.5 ns and an expected fall time of 13.3 ns. The UVLO value is 3 V which allows the use of GaN components with a recommended gate drive voltage of 5 V.

The device is packaged in a SOIC-16 NB package which has no special features for the easy transport of heat. However, the losses of the driver should be limited avoiding any problems.

A logic supply and a gate drive supply of 5 V are used during the tests as recommended.

4.1.5. Gate resistance selection

The external gate resistance is of great importance when connecting the external drivers to GaNbridge. In the tests, a rather high resistance is used because unacceptable ringing was occurring, compromising the proper functioning of the circuit. The same gate resistances are used for both external drivers because they showed similar problems and different gate resistances would make comparison more difficult. The selected turn-on resistance is 20 Ω and the turn-off resistance 10 Ω. It is possible to use a different gate resistance for turn-on and turn-off using a diode. An illustration of the influence of the gate resistance can be found in Fig. 6. Here, the switching behaviour of the TI driver is shown for two different sets of gate resistances, proving that the ringing is suppressed for higher resistances at the expense of the switching speed.

4.1.6. Resulting PCBs

The final design of the boards can be seen in Fig. 7. The aim of the layout was to make the different current loops as small as possible. The power loop can be seen in red, the low side gate loop in blue and the high side gate loop in orange. For the PCBs with external driver two versions were made with the driver both next (on the front of the PCB) and below (on the back of the PCB) the GaNbridge component in an attempt to make the gate loop even smaller. During preliminary experiments the version with everything on the front of the PCB, and thus with a slightly larger gate loop, proved to be more efficient. Probably due to the lower temperatures at these locations. These versions were selected for the final tests and are given in the figure.

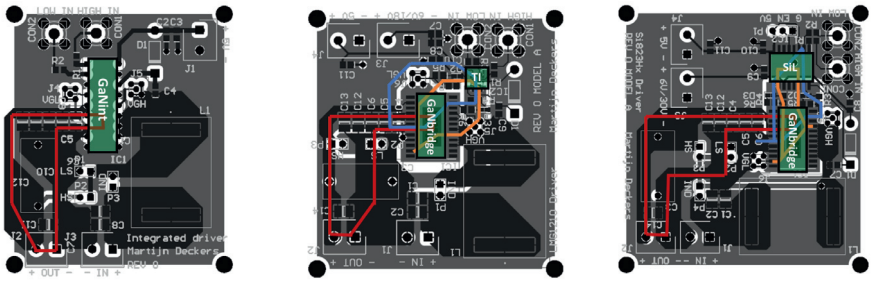
It was also tried to use the same auxiliary components around the driver and GaN transistor in all designs to ensure the fairest comparison possible. First, the board with GaNint was designed with its respective components after which the same components were used in the design of GaNbridge with TI and SiL. Because of this the components in the later might slightly deviate from the components proposed in the driver data sheets.

The PCB consist of a top and bottom copper layer of 35 μm with FR4 insulation material in between with a thickness of 1.55 mm.

4.2. Tests and equipment

The aim of this paper is to show the difference in performance between GaNint and GaNbridge with commercial drivers as a reference. This will show the state of GaN-on-SOI technology compared to the state of the art. Efficiency curves will be constructed for varying load currents at two different input voltages and switching frequencies. This will give a good overview of the relative position of each component. However, several parameters are kept constant during the experiments and also the influence of voltage and frequency is not completely clear from two set points. A sensitivity analysis is added to document all dependencies.

The different conducted tests are summarised here.



(a) Board 1: Imec integrated driver (GaNint).

(b) Board 2: Texas Instruments LMG1210RVRT driver (GaNbridge and TI).

(c) Board 3: Silicon Labs Si827GB-IS1 driver (GaNbridge and SiL).

Fig. 7. The used PCB designs with an indication of the power loop (red), low side gate loop (blue) and high side gate loop (orange).

- Test A: Constant input voltage of 25 V at 200 kHz with changing input current;
- Test B: Constant input voltage of 25 V at 500 kHz with changing input current;
- Test C: Constant input voltage of 50 V at 200 kHz with changing input current;
- Test D: Constant input voltage of 25 V and input current of 1 A at 500 kHz with changing dead time;
- Test E: Constant input voltage of 25 V / 50 V and constant input current of 0.5 A / 1 A with changing switching frequency;
- Test F: Constant input current of 1 A at 200 kHz with changing input voltage;
- Test G: Constant output voltage of 50 V at 200 kHz with changing input voltage.

Here follows a short overview of the used equipment to supply power in order to conduct these tests and measure the circuit behaviour.

- Vitrek PA900 harmonic power analyzer
- Tektronix 5 series mixed signal oscilloscope MSO56
- Tektronix IsoVu TIVH02 voltage probe
- FLIR T530 thermal camera
- Keysight 33500B series waveform generator
- Delta Elektronika SM660-AR-11 power supply and EST-150 auxiliary power supply
- Coudoint rheostat SNE500x60S2-80R

4.3. Remarks on the measurements

As described in Li et al. (2020a), the threshold voltage of the power transistor drops after stressing the component. This progressive behaviour is of minor importance in the performed experiments as the threshold value saturates when a number of cycles are completed. The threshold voltage is not very sensitive to temperature so this will only play a limited role as well. The expected threshold voltage is $3.5\ V$.

The seen performance differences will not only be caused by the effect of integration as the used driver circuits are also different. The main disadvantage of an integrated GaN based design is the absence of practically usable p-MOS devices (Ng et al., 2018). Literature is already suggesting improvements for integrated GaN drivers design like an added charge pump in Tang et al. (2018) or integrated supply voltage regulation (Kaufmann et al., 2020) based in an all n-MOS design. Current research for the CMOS based external drivers shows more complex developments such as current sensing, tunable output resistances, dead time control, reverse conduction detection, energy storage based driving and dv/dt control (Bau et al., 2020; Grezaud et al., 2016; Seidel and Wicht, 2018; Yu et al., 2018; Zhang et al., 2019). The limited complexity of the used integrated driver compared to the external drivers does not harm the scope of the paper as this reflects the actual difference between current integration technology and commercial external drivers. Because the main goal is to show the effect of driver integration on the switching performance, losses in the driver are not taken into consideration in the efficiency calculation.

5. Experimental results

In this section the experimental results from tests A, B, C, D, E, F and G will be discussed. First, the converter efficiency will be given together with the package temperature allowing to make a definitive statement about the switching speed and performance followed by a sensitivity analysis to make the found results more general.

5.1. Converter efficiency

In this subsection the efficiency of GaNint and GaNbridge with TI and SiL will be compared. This will be done for a varying loading at a few different input set points. The switching speeds and voltage waveforms will also be included. Test A is a test at low voltage and low frequency, after which test B will show the same test at a higher frequency and test C at a higher voltage. The expectation is that the advantage of driver integration becomes more profound in test B as the switching losses will be more accentuated. Also for a higher voltage the switching losses will be accentuated due to the effects described in section 3 which should be beneficial in case of driver integration. Tests B and C will also allow to specify the negative effects caused by the additional oxide capacitance as these losses are both function of the frequency and the voltage.

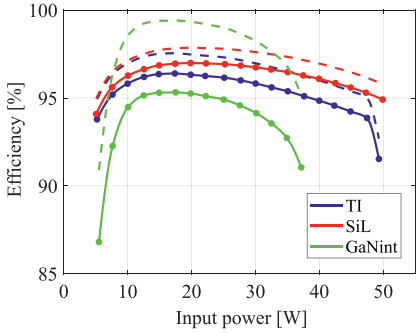
5.1.1. Test A: Performance versus loading

Efficiency

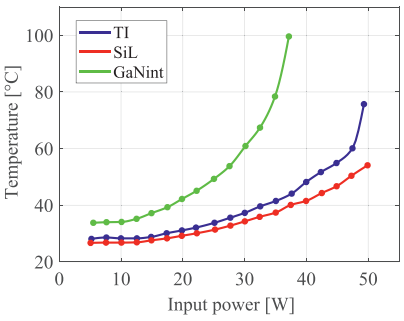
In Deckers et al. (2020) the results of test A, the boost converter efficiency in function of the input power for an input voltage of 25 V, were already reported. The recorded peak efficiency from the synchronous boost converter of 95.3 % using GaNint was less than the one with GaNbridge using commercial drivers SiL and TI achieving 97.2 % and 96.5 % respectively. For convenience the measurements are repeated in Fig. 8a. As stated previously, the driver losses are excluded from the efficiency calculation. The static power dissipation of the integrated driver (calculated) is $0.09\ W$ which is small compared to the converter loss. The reached converter efficiency results are not satisfactory as the aim was to achieve a better performance due to the elimination of excessive parasitic inductance by integration.

Influence of temperature

A possible reason for this is the high package temperature which influences the temperature dependent on-resistance. The package temperatures of GaNint and GaNbridge are given in Fig. 8b. It can be seen that

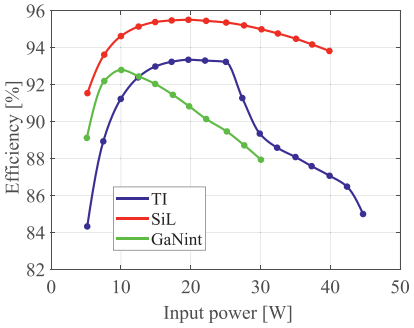


(a) Converter efficiency in function of the converter input power [1]. The dashed lines represent the estimated efficiency without conduction loss.

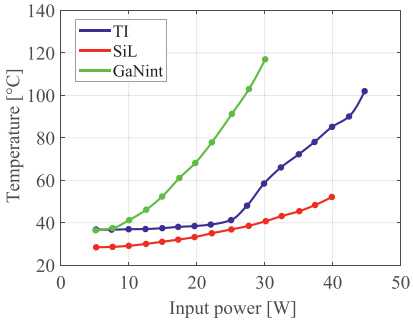


(b) UTAC and Imec integrated driver package top surface temperature in function of the converter input power.

Fig. 8. Test A: Performance comparison for different drivers. The test is done at an input voltage of 25V, a switching frequency of 200kHz, a dead time of 25ns and a duty cycle of 0.5. The dashed line indicates the estimated efficiency when the conduction losses are excluded.



(a) Converter efficiency in function of the converter input power.



(b) GaNbridge and GaNint package top surface temperature in function of the converter input power.

Fig. 9. Test B: Performance comparison for different drivers. The test is done at an input voltage of 25 V, a switching frequency of 500 kHz, a dead time of 25 ns and a duty cycle of 0.5.

the package temperature of GaNint is drastically higher than GaNbridge. The temperature mainly influences the conduction losses while the other losses like output capacitance and switching losses are a lot less temperature dependent. Excluding the conduction losses should thus largely eliminate the temperature from the evaluation. In Fig. 8b a rough estimate of the efficiency without conduction loss is included, shown with dashed lines. The conduction loss is calculated using the measured drain to source voltage drop and the current through the components. This excludes the temperature as much as possible from the problem. Now it is visible that the switching losses of GaNint are significantly lower leading to a high efficiency in comparison with GaNbridge driven by SiL and TI (except at low power). The high temperature can be caused by the packaging which is a bare die at the moment, leading to high thermal resistances. As mentioned, it should also be noted that the driver losses are dissipated in the same die than the power transistors which is also a disadvantage of extensive integration. Certainly with the used resistive push-pull driver where the losses are significant.

Influence of parasitic substrate capacitance

It can be seen that at low power, the corrected performance of GaNint is still lower than SiL and TI while the package temperatures are roughly the same. This indicates that the extra parasitic substrate capacitance C_{sub} makes a significant difference at this point. Equation 1 shows that the losses due to this capacitance P_{sub} are only dependent on the drain to source voltage V_{DS} and the switching frequency f_{sw} while the switching losses P_{SW} are also dependent on I_{DS} as given in equation 2 (together with the indirect influence on the voltage and current transition times t_v and t_c on I_{DS}). As a result, the switching losses dominate at higher currents while the increased C_{sub} becomes visible at low currents. The influence of the load current will be studied more in detail in section 5.2.

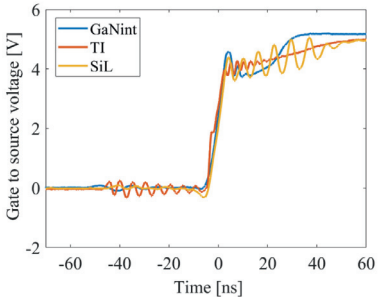
$$P_{sub} = C_{sub}\, V_{DS}^2\, f_{sw} \tag{1}$$

$$P_{SW} = \frac{1}{2}\, f_{sw}\, (t_v + t_c)\, V_{DS}\, I_{DS} \tag{2}$$

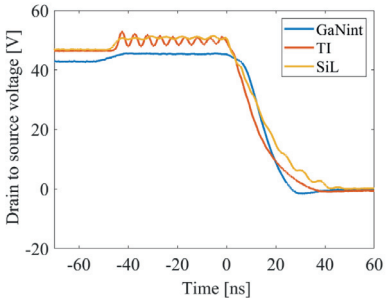
5.1.2. Test B: Performance versus loading at higher frequency

Efficiency and temperature

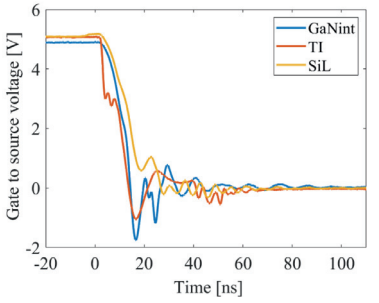
Fig. 9 gives the results of test B. The efficiency curve for the same input conditions but a higher switching frequency of 500 kHz is shown. With an input voltage of 25 V and a switching frequency of 500 kHz, SiL reaches a peak efficiency of 95.7 %, GaNint 92.9 % and TI 93.4 %. This test aims to further distinguish the switching and output capacitance losses from the constant conduction losses, given a certain temperature. These should be linearly dependent on the switching frequency, a similar spread as in test A is thus expected. However, It can be seen that the order of performance changes for low input powers as GaNint becomes more efficient than GaNbridge using the TI driver. This is unexpected as the high C_{sub} proved to be dominant at low powers in the previous experiment. This shows that the switching losses are more than linearly dependent in the switching frequency using the TI driver. This shows an advantage of integration as GaNint is less prone to ringing at these higher switching frequencies. The relation between SiL and GaNint re-



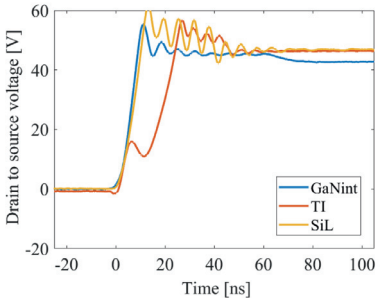
(a) Gate to source waveforms of Q1 turn-on.



(b) Drain to source waveforms of Q1 turn-on.



(c) Gate to source waveforms of Q1 turn-off.



(d) Drain to source waveforms of Q1 turn-off.

Fig. 10. Test B: Comparison of the gate to source and drain to source waveforms of Q1 for the different drivers. The measurements are done at a constant input voltage of 25 V and an input current of 1 A (25 W). The switching frequency is 500 kHz, the dead time is 50 ns and the duty cycle is 0.5.

mains similar to test A as was expected. In section 5.2 the influence of the switching frequency will be studied in more detail.

At higher powers GaNbridge with TI clearly experiences problems as the efficiency drops drastic not following the trend observed in test A. A detailed look at the gate signal showed that the upper switch (Q2) is pulled down during its conduction phase, forcing the transistor into reverse conduction, increasing the losses drastically. This leads to the sharp drop in efficiency as can be seen in the graphs. A possible explanation is that the over-temperature shutdown of the driver is triggered. The fact that this phenomenon occurred at lower power levels when the driver was mounted on the back of the GaN bridge instead of next to it resulting is less cooling, confirms this theory. It also explains why the duration of the shutdown is longer at higher power levels and why it also becomes worse in time.

Gate and drain to source waveforms of Q1

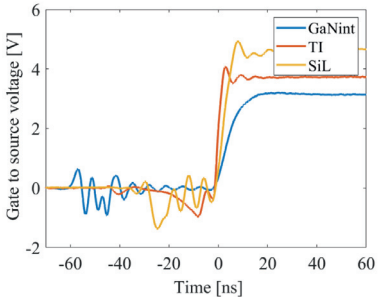
Next to the general efficiency, the gate and drain to source waveforms give a lot of information about the components performance measures like the amount of ringing present and the switching speed. First the voltage waveforms of Q1 are studied in Fig. 10. Here a major difference is visible in the ringing present in the gate signal, SiL clearly shows the most ringing followed by TI. At turn-off, GaNint shows some ringing but this is no point of concern as is does not exceed the threshold voltage of 1.7 V. TI also shows the Miller plateau which may be expected in the gate signal of Q1. The drain to source waveforms show that TI has a notably longer switching speed than the other components. GaNint overall performs the fastest switching with the switching speed of SiL reaching comparable values in this test condition.

Gate and drain to source waveforms of Q2

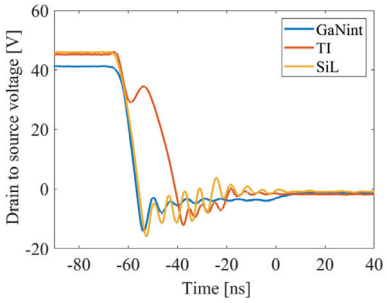
In the waveforms of Q2 shown in Fig. 11, much larger differences between the drivers can be noted. One should recall that the gate of the upper GaN switch is supplied with a bootstrap circuit. The voltage drop over the diode used can cause the gate voltage to be 0.5 V lower than the ideal supply of 5 V. This is the case for SiL where the voltage is indeed lower than the Q1 drive signal. It can also be seen that ringing is present due to the voltage transitions caused by the switching of Q2 (during the dead time before the Q2 turn-on and after the dead time when Q2 is turned off). There is also no clear slope present in the gate voltage, indicating that the bootstrap circuit (mainly the capacitor) is sufficiently sized. TI has a voltage drop which is clearly bigger than the diode voltage drop and must be caused by the internal circuit of the driver. There is also ringing present during the dead time after the turn-off of Q2 which may be a result of C_{OSS} charging currents. GaNint shows an even larger voltage drop. It is known that the used push-pull driver topology suffers from a threshold voltage drop in the pull-up transistor. A supply of 8 V was used to keep this into account but the voltage drop at the high side turns out to be more severe than anticipated and cannot be fully compensated with the use of a bootstrap circuit. This can also contribute to the increased on resistance next to the high temperature. A separate supply with a higher voltage could be used to solve this problem but care should be taken that this does not damage the low voltage transistors as some of the gates experience this voltage directly. The drain to source waveforms again show that TI has a notably longer switching speed than the other components.

5.1.3. Test C: Performance versus loading at higher voltage

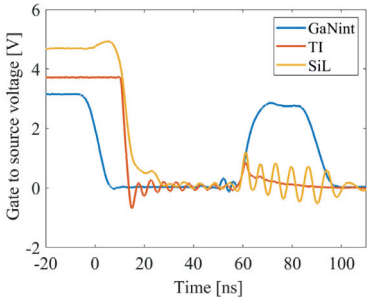
Test C again uses a switching frequency of 200 kHz but now with an input voltage of 50 V, the results are given in Fig. 12a. Slightly lower converter peak efficiencies of 94.5 % (GaNint), 97.0 % (SiL) and 96.3 % (TI) are reached. The aim of this test is to again differentiate between P_{SW} and P_{sub}. The higher voltage increases the switching losses and the output capacitance losses more than linearly. The composition of the switching losses is rigorously treated in section 3, the output capacitance losses would increase quadratically with the voltage would it not be for the capacitance decrease when the drain to source voltage rises. The P_{sub} losses increase quadratically but have a small share which causes the performance difference to remain similar to test A. At higher powers the efficiency of GaNint drops more severe but this can again be



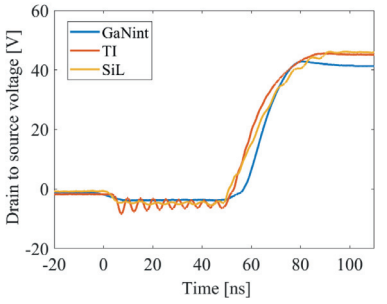
(a) Gate to source waveforms of Q2 turn-on.



(b) Drain to source waveforms of Q2 turn-on.

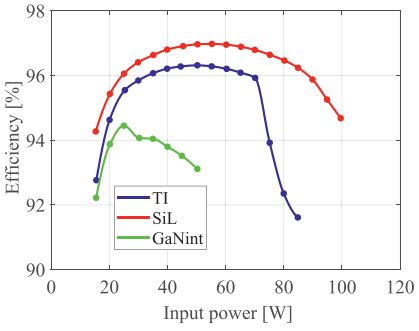


(c) Gate to source waveforms of Q2 turn-off.

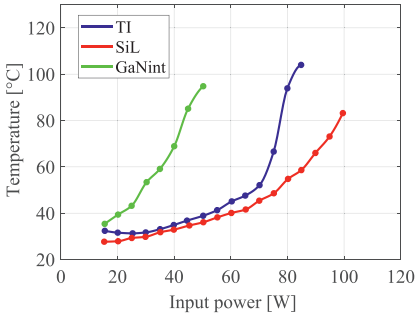


(d) Drain to source waveforms of Q2 turn-off.

Fig. 11. Test B: Comparison of the gate to source and drain to source waveforms of Q2 for the different drivers. The measurements are done at a constant input voltage of 25 V and an input current of 1 A (25 W). The switching frequency is 500 kHz, the dead time is 50 ns and the duty cycle is 0.5.



(a) Converter efficiency in function of the converter input power.



(b) GaNbridge and GaNint package top surface temperature in function of the converter input power.

Fig. 12. Test C: Performance comparison for different drivers. The test is done at an input voltage of 50 V, a switching frequency of 200 kHz, a dead time of 25 ns and a duty cycle of 0.5.

assigned to the positive feedback between temperature and conduction losses.

5.1.4. Overview

It was shown that GaNint is less performant than the commercial available drivers. A compensation for conduction losses was proposed to eliminate the different temperatures from the problem. This theoretical performance is better than the commercial driver except for low current levels where the newly created oxide capacitances dominate. A different frequency and voltage was used to see how this influences the performance. The relative performance was mostly preserved except for TI who suffered under higher frequencies where a non-linear behaviour of the switching losses was observed.

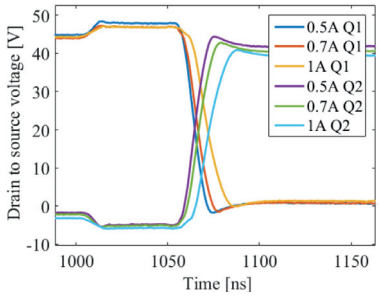
An overview of the measured peak efficiencies in this section is given in Table 3.

Table 3
Overview of the measured converter peak efficiencies.

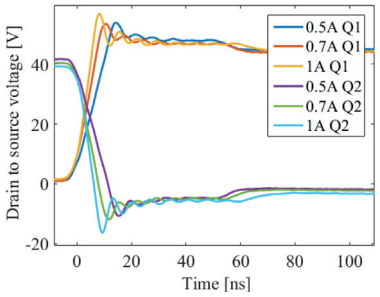
Input voltage	Frequency	GaNint	TI	SiL	Test
25 V	200 kHz	95.3 %	96.5 %	97.2 %	A
25 V	500 kHz	92.9 %	93.4 %	95.7 %	B
50 V	200 kHz	94.5 %	96.3 %	97.0 %	C

5.2. Sensitivity analysis

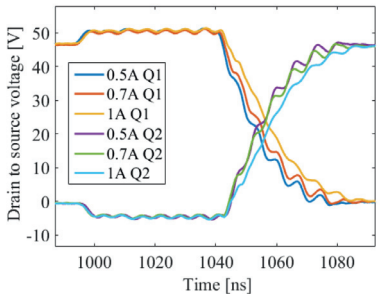
Previous subsection 5.1 showed the efficiencies in a few operating points in the boost converter. The load current, switching frequency and input voltage was changed to see the influence on performance. In this section this will be done in greater detail with a focus on switching



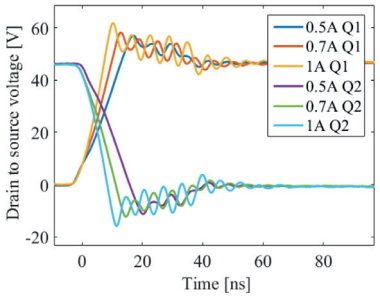
(a) Forced commutation of GaNint, Q1 turns on and Q2 turns off.



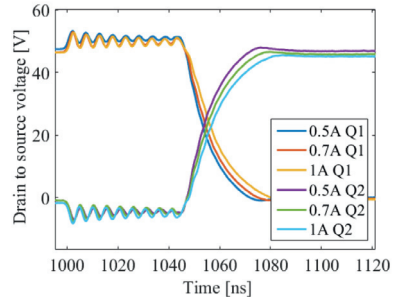
(b) Self commutation of GaNint, Q1 turns off and Q2 turns on.



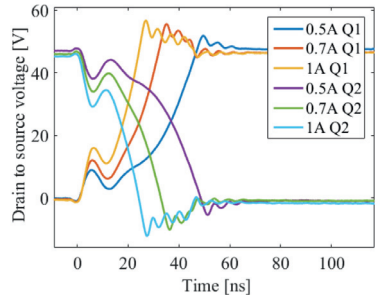
(c) Forced commutation of GaNbridge with SiL, Q1 turns on and Q2 turns off.



(d) Self commutation of GaNbridge with SiL, Q1 turns off and Q2 turns on.



(e) Forced commutation of GaNbridge with TI, Q1 turns on and Q2 turns off.



(f) Self commutation of GaNbridge with TI, Q1 turns off and Q2 turns on.

Fig. 13. Test B: Drain to source waveforms of GaNint and GaNbridge for different input currents. The measurements are done at a constant input voltage of 25V, the switching frequency is 500kHz, the dead time is 50ns and the duty cycle is 0.5.

waveforms and switching speed as this is the main parameter integration aims to improve. Parameters such as dead time and duty cycle were kept constant during the experiments, this subsection will also analyse the importance of that.

5.2.1. Test B: Load current

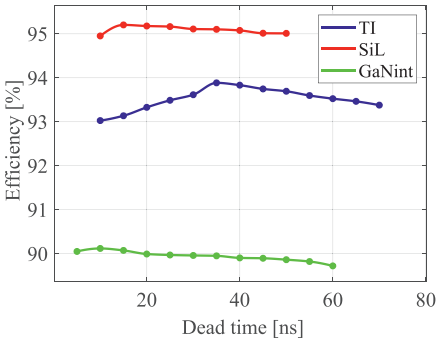
The load current is the main parameter which was varied in tests A, B and C. The drain to source voltage waveforms of test B are shown in Fig. 13 for three different current levels. According to section 3, the switching speed should increase with the load current during self commutation and decrease with the load current during forced commutation. Table 4 summarises the switching speeds. GaNint achieves the fasted switching speed meaning that the switching losses need to be lowest. However, as previously seen, this is not always able to compensate for the additional parasitic capacitance losses which are independent of the switching speed.

Table 4
Test B: Switching speed for different converter input currents during self and forced commutation. The measurements are conducted at a constant input voltage of 25V, the switching frequency is 500kHz, the dead time is 50ns and the duty cycle is 0.5 (Deckers et al., 2020).

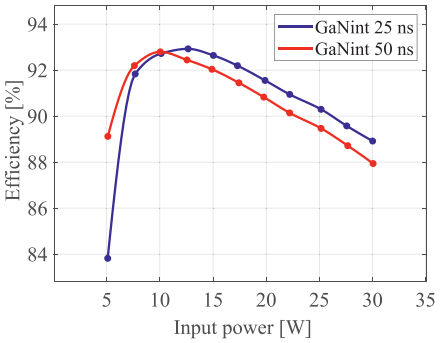
Driver	Current	0.5A	0.7A	1A
Imec integrated	Self	16ns	12ns	10ns
	Forced	18ns	22ns	30ns
Texas Instruments	Self	48ns	35ns	26ns
	Forced	33ns	35ns	37ns
Silicon Labs	Self	20ns	16ns	12ns
	Forced	36ns	38ns	40ns

5.2.2. Test D: Dead time

A parameter that was kept constant in the efficiency comparison, but also has an influence, is the used dead time. It was already mentioned

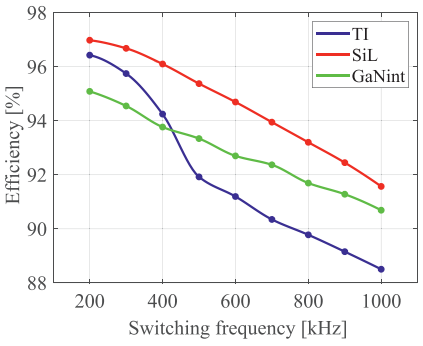


(a) Converter efficiency comparison in function of the dead time with an input current of 1 A (25 W).

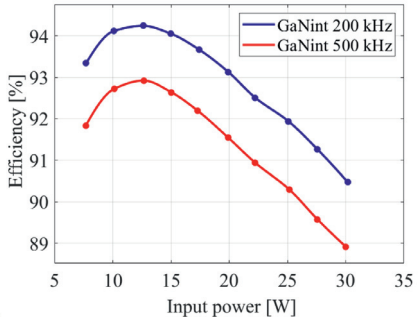


(b) Efficiency comparison for the GaNint in function of the input power for a dead time of 25 ns and 50 ns.

Fig. 14. Test D: Influence of the dead time with an input voltage of 25 V, a switching frequency of 500 kHz and the duty cycle is 0.5.



(a) Converter efficiency in function of the switching frequency at 50V 1A input for TI and SiL and 25V 0.5A input for GaNint.



(b) Converter efficiency in function of the converter input power for GaNint at a switching frequency of 200kHz and 500kHz with an input voltage of 25V and a dead time of 25ns.

Fig. 15. Test E: Converter efficiency dependence on the switching frequency with a duty cycle of 0.5 (without correction for the dead time).

in section 3 that it is possible to choose an ideal dead time. To show this, test E varies the dead time for an input of 25 V and 1 A as given in Fig. 14a. It can be seen that the ideal dead times are different for each driver. When the dead time is too long, there are a lot of reverse conduction losses. When the dead time is too short, the self commutation transfers into a forced commutation, leading to more switching losses. As a result the dead time should be taken equal to the switching time during self commutation.

This has as a consequence that the ideal dead time is dependent on the load current as it changes the switching speed during self commutation. This is illustrated in Fig. 14b where the efficiency curve of GaNint is plotted for a dead time of 25 ns and 50 ns. It can be seen that the 50 ns of dead time leads to higher efficiencies for low powers where the switching speeds are low while it leads to lower efficiencies in the high power region of the curve. This is another contribution to the shape of the efficiency curve that was not yet mentioned. It should be noted that the influence of the dead time is not very large around the optimal point. The TI driver has the largest dependency on the dead time so the dead time selection during the experiments was based on this component.

5.2.3. Test E: Switching frequency

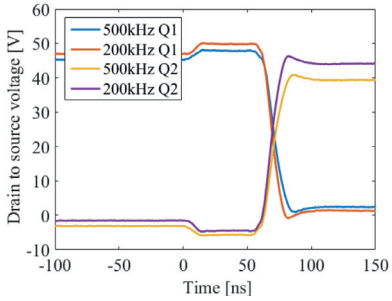
Experiment E examines the performance in function of the switching frequency. GaN components are generally used in high frequency applications because of their ability to switch fast, limiting the dissipated power in each switching action. The loss for each commutation cycle does not change, meaning that the dissipated power and efficiency should have a linear relationship with the switching frequency.

Fig. 15 shows the efficiency of the different drivers in function of the switching frequency as a result of test E. Note that the used power level for GaNint is lower because of the high case temperatures. It can be seen that GaNint and SiL are showing a quite linear behaviour as expected. The flatter slope of GaNint shows that the switching speed is faster. TI clearly shows a non linear behaviour, this means that the switching speeds are also influenced by the switching frequency. Fig. 16 shows the drain to source waveforms for two different switching frequencies clearly showing the influence on the switching speed.

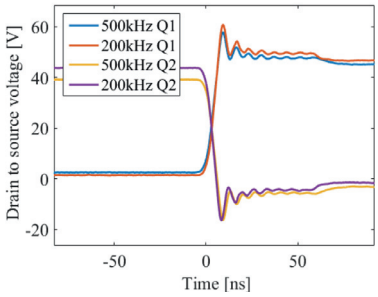
5.2.4. Test F: Input voltage

In Table 5 the results of test F are presented. Here the input current is fixed at 1 A while the input voltage is brought to 10 V, 25 V and 50 V respectively. This is a useful experiment as it allows to understand the differences seen between the efficiency measurement at 25 V and 50 V.

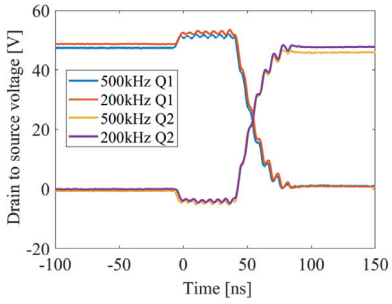
In section 3 it was already explained that the forced commutation losses will thus rise more than linear and the self commutation losses in a quadratic way with V_{DS}. The table confirms that the switching time rises with the converter input voltage, also here GaNint performs best. Fig. 17 shows the corresponding drain to source voltage waveforms.



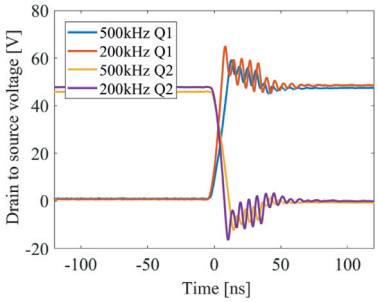
(a) Forced commutation of GaNint, Q1 turns on and Q2 turns off.



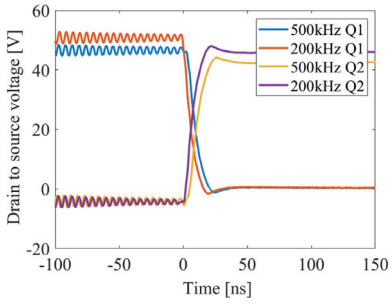
(b) Self commutation of GaNint, Q1 turns off and Q2 turns on.



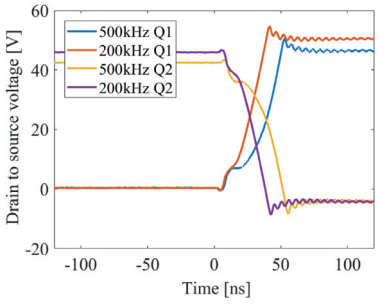
(c) Forced commutation of GaNbridge with SiL, Q1 turns on and Q2 turns off.



(d) Self commutation of GaNbridge with SiL, Q1 turns off and Q2 turns on.



(e) Forced commutation of GaNbridge with TI, Q1 turns on and Q2 turns off.



(f) Self commutation of GaNbridge with TI, Q1 turns off and Q2 turns on.

Fig. 16. Test E: Drain to source waveforms of GaNint and GaNbridge for different switching frequencies. The measurements are done at a constant input voltage of 25 V, a load current of 1 A and the duty cycle is 0.5.

Table 5
Test F: Switching speed for different converter input voltages during self and forced commutation. The measurements are done at a constant input current of 1 A, the switching frequency is 500 kHz, the dead time is 50 ns and the duty cycle is 0.5.

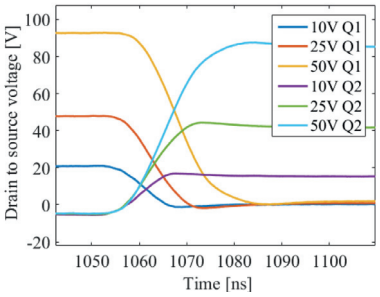
Driver	Voltage	10 V	25 V	50 V
Imec integrated	Self	11 ns	16 ns	23 ns
	Forced	13 ns	18 ns	25 ns
Texas Instruments	Self	34 ns	48 ns	53 ns
	Forced	23 ns	33 ns	41 ns
Silicon Labs	Self	12 ns	20 ns	25 ns
	Forced	25 ns	36 ns	47 ns

Fig. 18 shows this behaviour by varying the input voltage but keeping the current constant. Because the duty cycle is fixed at 0.5 the output voltage is always almost the double of the input voltage. It can be seen that for all the drivers, the losses increase in a more than linear way with the voltage, this causes the efficiency to stagnate.

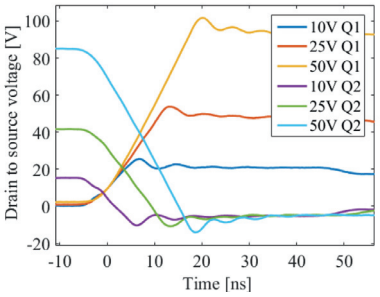
5.2.5. Test G: Closed loop duty cycle

Previously, all the tests were conducted with a duty cycle of 0.5. In real operation, mostly a fixed output voltage is wanted while the input voltage is changing. In this subsection the converter performance will be tested in this condition.

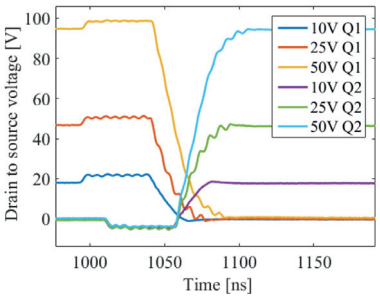
The output voltage will be kept fixed at 50V and the load current at 0.5A. The input voltage will be varied and the duty cycle will be altered accordingly. The result of test G are visible in Fig. 19. When the duty cycle is higher, the output-input voltage ratio becomes larger as well. The build up inductor current will also become greater, leading to losses proportional to the current squared. Such behaviour is indeed visible in the figure. The TI driver seems to have an odd behaviour at higher input voltages and low duty cycle. This can be explained by the



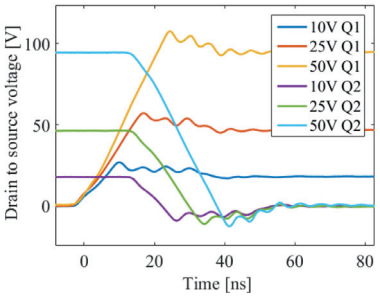
(a) Forced commutation of GaNint, Q1 turns on and Q2 turns off.



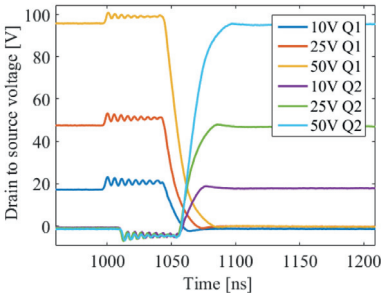
(b) Self commutation of GaNint, Q1 turns off and Q2 turns on.



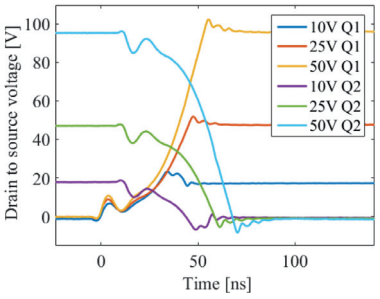
(c) Forced commutation of GaNbridge with SiL, Q1 turns on and Q2 turns off.



(d) Self commutation of GaNbridge with SiL, Q1 turns off and Q2 turns on.



(e) Forced commutation of GaNbridge with TI, Q1 turns on and Q2 turns off.



(f) Self commutation of GaNbridge with TI, Q1 turns off and Q2 turns on.

Fig. 17. Test F: Drain to source waveforms of GaNint and GaNbridge for different input voltages. The measurements are done at a constant input current of 1A, the switching frequency is 500kHz, the dead time is 50ns and the duty cycle is 0.5.

lower currents, leading to a required dead time that is longer than the foreseen 50ns to have ideal switching during the self commutation.

5.3. Summary

The previous sections explained the shape of the seen efficiency measurements and the differences between GaNint and GaNbridge. Here a short summary of the discussion is made.

The main reasons for the underperformance of GaNint:

- High temperature due to large thermal resistance in packaging;
- High temperature due to driver dissipation in the same die;
- Larger parasitic oxide capacitance due to monolithic integration creating extra electrically isolated layers;
- Very basic driver design causing a lower than ideal gate drive voltage at the high side due to bootstrap diode and driver threshold voltage drop.

The shape of the efficiency curve is caused by:

- Constant losses like output capacitance and gate charge losses become less important at higher powers;
- High temperatures increase the on-resistance and conduction loss at higher powers;
- Switching loss during forced commutation rise in a more than linear fashion with the load current;
- The oxide capacitance losses are not dependent on the load current;
- A fixed dead time leads to higher efficiencies for low powers where the switching speeds are low while it leads to lower efficiencies in the high power region of the curve (Only a very small influence).

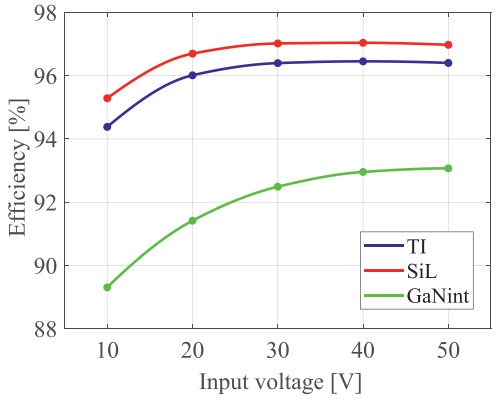


Fig. 18. Test F: Converter efficiency in function of the input voltage. The test is done at an input current of 1 A, a switching frequency of 200 kHz, a duty cycle of 0.5 (without compensation for the dead time) and a dead time of 25 ns for TI and SiL and 50 ns for the GaNint.

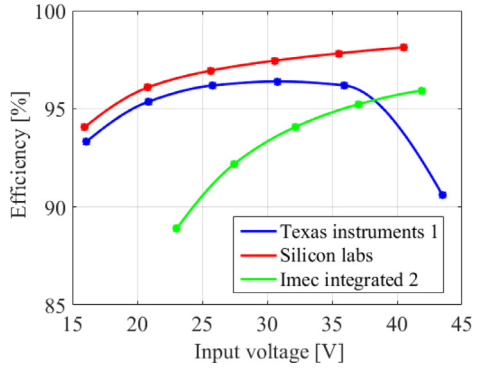


Fig. 19. Test G: Converter efficiency in function of the input voltage with a fixed output voltage of 50V and a fixed load current of 0.5A and a switching frequency of 200kHz.

6. Conclusion

In the recent years a lot of development took place in the area of GaN drivers. GaN-on-SOI technology made it possible to integrate multiple power transistors and their gate drivers onto the same die without experiencing substantial biasing effects. In this paper a GaN bridge with integrated drivers using GaN-on-SOI was tested in a boost converter setup following on the results previously reported in Deckers et al. (2020). The aim is to position the performance of the component with integrated drivers (GaNint) within the commercially available alternatives (GaNbridge with TI and SiL). A theoretical consideration also allows to estimate the influence that the input parameters have on the performance with a sensitivity analysis, these conclusions were also verified with experiments.

Several converter efficiency results were shown together with the package temperatures. The conclusion that high temperatures are causing a GaNint underperformance despite its superior switching speed remains.

However, it should be noted that the GaN-on-SOI does not allow to eliminate the full effects of integration as can be seen by the high losses at low power. This indicates that the parasitic capacitance due to the substrate is larger than in the not integrated case.

The reason for the high temperatures is the packaging, the used DIL (dual-in-line) package has very high thermal resistance. This causes the temperature to go higher compared to the other package solutions, which further increases the on-resistance and that in-turn reduces the efficiency by increasing conduction loss. Next to the packaging, the driver dissipation also leads to a temperature increase in GaNint which is not present in the switches with external driver. Certainly when the losses are substantial as is the case with the used push-pull driver.

It is visible that the performance difference between GaNint and GaNbridge becomes smaller when the switching frequency rises. This is expected as the switching losses become more important at higher frequencies accentuating the faster switching speed of GaNint.

At the end a sensitivity analysis is added, examining the influence of the most important input parameters. The dependence on the input voltage is recorded and the influence of the switching frequency is shown as an important parameter for the applicability of the components. The converter efficiency using external drivers decrease more than linear because of extra parasitic effects when using higher frequencies. GaNint has a more ideal linear dependency again showing the advantage of integration. The influence of dead time and duty cycle was also shown to examine the influence of these previously constant parameters.

In general the prototype GaNint is still outperformed by the commercially available external drivers. Better packaging will be the solution to lower the case temperature and fully exploit the better switching characteristics of GaN components with integrated driver resulting in an improved efficiency. Together, these findings formulate an answer on the research question posed in section 1.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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