PHOTONICS Research

III-V-on-Si_3N_4 widely tunable narrow-linewidth laser based on micro-transfer printing

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Leveraging its superior waveguide properties, silicon-nitride (Si_3N_4) photonics is emerging to expand the applications of photonic integrated circuits to optical systems where bulk optics and fibers today still dominate. In order to fully leverage its advantages, heterogeneous integration of III-V gain elements on Si_3N_4 is one of the most critical steps. In this paper, we demonstrate a III-V-on-Si_3N_4 widely tunable narrow-linewidth laser based on micro-transfer printing. Detailed design considerations of the tolerant III-V-to-Si_3N_4 vertical coupler, Si_3N_4-based micro-ring resonators (MRRs), and micro-heaters are discussed. By introducing the dispersion of Si_3N_4 waveguide in the design, the proposed Vernier MRRs enable an extended tuning range over multiple Vernier periods. The laser shows a wavelength tuning range of 54 nm in C and L bands with intrinsic linewidth less than 25 kHz. Within the tuning range, the side mode suppression ratio is larger than 40 dB and the output power in the Si_3N_4 waveguide reaches 6.3 mW. The integration process allows for the fabrication and quality control of both the Si_3N_4 circuits and III-V devices in its own foundry, which greatly enhances the integration yield and paves the way for large-scale integration.

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1. INTRODUCTION

Narrow-linewidth tunable lasers are desired for a wide range of applications, such as high-capacity coherent communication systems, sensors, and microwave photonics. Laser sources with a tuning range covering the C band and linewidth of hundreds of kHz have been widely used in long-haul coherent communication systems [1]. In order to further increase the transmission capacity, more wavelength bands (C and L bands), denser grids, and higher-order modulation formats (e.g., high-order QAM) are indispensable, which implies the need of even wider tuning range and narrower linewidth [2,3]. Furthermore, the laser linewidth is a key parameter determining the detection distance of coherent LiDAR [4] and distributed fiber sensors [5], as well as the quality of RF signals in photonic microwave generation [6]. Meanwhile, the wavelength tuning range is also crucial to realize large steering angles in optical phase arrays (OPAs) [7] and a high axial resolution in optical coherence tomography (OCT) [8].

Driven by these demands, integrated narrow-linewidth tunable lasers have made rapid progress in the past decades. An important step in its advancement is the move from monolithic integration on pure III-V material systems to heterogeneous integration on low-loss waveguide platforms. Early generations of tunable laser diodes were built on a III-V native substrate through integration of passive waveguides with active gain sections. On-chip compound cavities were formed to realize both wavelength tuning and linewidth reduction. By means of this approach, state-of-the-art III-V monolithic lasers have shown 60-nm wavelength tuning range and tens of kHz linewidth [9]. However, further reduction of the linewidth is difficult, mainly due to the lack of low-loss passive waveguides. By heterogeneous integration of III-V gain materials on silicon-on-insulator (SOI) wafers, the performance of narrow-linewidth tunable laser has been significantly improved [10,11]. Taking the advantages of low loss and long Bragg gratings, a heterogenous laser with 1-kHz linewidth has been demonstrated [10]. In order to further enhance the effective cavity length and reduce the footprint, micro-ring resonators (MRRs) were proposed to build the laser cavity. The effective length of an MRR near its resonance can be tens or even hundreds times

its physical length and a wide tuning range can also be realized through the Vernier effect in cascaded MRRs. A heterogenous MRRs-based laser with 110-nm tuning range and linewidth down to 220 Hz has been demonstrated [11]. However, ultra-low-loss waveguides on an SOI platform are only possible using an extremely shallow rib with very low lateral optical confinement, where a minimal ring radius of around 600 μm is required to avoid bending loss. This does not only increase the footprint of the chip, but also reduces the mode selection ability, requiring the implementation of a complicated triple-ring mirror structure to guarantee single-mode lasing.

To achieve better performance and broaden the application scope, the heterogeneous integration of narrow-linewidth tunable lasers on a silicon nitride (Si_3N_4) photonic platform is emerging. Compared with SOI, Si_3N_4-based waveguides provide much lower propagation loss and handle much higher on-chip power [12], which enables a higher quality factor of the laser cavity and thus a reduced laser linewidth. Through edge-coupling between a III-V gain chip and Si_3N_4 chip, hybrid Si_3N_4 lasers have shown unprecedented linewidth performance [13]. However, owing to the large refractive index mismatch between III-V and Si_3N_4 waveguides, heterogeneous integration is much more challenging. To overcome this, a multilayer III-V-to-crystalline Si (cSi)-to-Si_3N_4 structure based on wafer bonding has been proposed, which leverages an intermediate cSi layer as the index matching layer [14]. Following this approach, a sub-kHz single wavelength laser was demonstrated by using long Bragg gratings on Si_3N_4 [15]. By further integration of the III-V gain medium and ultra-low-loss Si_3N_4 waveguides with optical loss of around 0.5 dB/m, a Hz-level fixed wavelength laser was also demonstrated [6]. Recently, a combination of butt-coupling and evanescent coupling through an intermediate dielectric waveguide has been proposed to enable a heterogeneous laser at sub-micrometer wavelengths [16]. By using Vernier MRRs on Si_3N_4, a tunable laser with 20-nm tuning range and linewidth down to 2.8 kHz was realized around 980 nm. Our group has proposed using a plasma-enhanced chemical vapor deposition (PECVD) hydrogenated amorphous silicon (aSi:H) intermediate layer to bridge the Si_3N_4 and III-V and demonstrated a heterogeneously integrated amplifier and a multimode ring laser by means of micro-transfer printing (MTP) [17]. Both the Si_3N_4 and aSi:H layers used in this approach were directly deposited on a Si substrate, which simplifies the whole process flow. Following this approach, we presented a III-V-on-Si_3N_4 narrow-linewidth laser with discrete tuning bands [18], where the tunability was constrained by the performance of the micro-heater on the Si_3N_4 waveguide. Although recent demonstrations of heterogeneous integrated III-V-on-Si_3N_4 lasers have shown excellent performance at a fixed wavelength or in a narrow wavelength tuning range, a widely tunable laser in the C and L bands, where most photonics applications are clustered, is very attractive.

In this paper, we present the use of micro-transfer printing to realize a widely tunable narrow-linewidth laser in the C and L bands. Detailed design considerations of the tolerant III-V-to-Si_3N_4 vertical coupler, Si_3N_4-based MRR mirror, and micro-heaters are discussed. A widely tunable cascaded-MRR architecture is demonstrated to realize wavelength tuning among multiple Vernier periods. The device is implemented on IMEC's 200-mm low pressure chemical vapor deposition (LPCVD) Si_3N_4 platform, onto which a pre-fabricated III-V gain coupon realized by III-V Lab is integrated. The quality control of both the Si_3N_4 circuits and III-V devices is realized in its own foundry, which greatly enhances the integration yield and paves the way for large-scale integration.

2. TOLERANT OPTICAL COUPLING DESIGN

A. Coupler Structure

In order to realize efficient optical coupling between Si_3N_4 and III-V waveguides, a two-stage adiabatic taper structure using an aSi:H intermediate layer is implemented following the concept proposed in Ref. [17]. In this paper, a wide rib aSi:H waveguide, along with optimized III-V and aSi:H waveguide dimensions, is used to achieve better coupling efficiency and fabrication tolerance. Moreover, a 400-nm Si_3N_4 layer is implemented for efficient power coupling between Si_3N_4 and aSi:H waveguides. It also exhibits high optical confinement, which supports a tight bending radius as low as 50 μm and allows small footprints of the building blocks defined on the Si_3N_4 waveguide platform.

Figure 1(a) shows a schematic view of the proposed coupling structure and the fundamental TE (TE0) mode at different cross-sections [Figs. 1(a1)–1(a8)] along the coupler. We start with a single-mode Si_3N_4 strip waveguide [Fig. 1(a1)] followed with a short Si_3N_4 taper to get the preferred waveguide width [Fig. 1(a2)] for coupling. Then, an aSi:H strip waveguide taper that linearly widens the waveguide width from 0.15 μm [Fig. 1(a3)] to 0.4 μm [Fig. 1(a4)] is used to couple the optical field from the Si_3N_4 to the aSi:H waveguide. Next, a strip to rib transition and a waveguide taper are employed on the aSi:H layer to realize an aSi:H rib waveguide [Fig. 1(a5)] with a desired waveguide width of 5.5 μm [Fig. 1(a6)]. Finally, the mode is partially transferred to the III-V layer stack by using a deeply etched III-V taper, and a III-V strip to rib transition to widen the separate-confinement heterostructure (SCH) and multi-quantum wells (MQWs) layers. The widths of the p-InP ridge and SCH/MQWs are first widened linearly from 0.6 μm [Fig. 1(a6)] to 3.5 μm [Fig. 1(a7)] together, and then to 4 μm and 7 μm [Fig. 1(a8)], respectively.

In the design, the thickness of the aSi:H layer is crucial to effectively bridge Si_3N_4 and III-V materials. A thin aSi:H layer is preferred to provide a large propagation constant mismatch between the aSi:H taper tip and Si_3N_4 waveguide, which can reduce the residual optical field around the tip and facilitate both the power coupling and reduced reflection. However, a thick aSi:H layer is required so that the aSi:H waveguide could have an effective index significantly exceeding the III-V taper tip. Furthermore, the thickness of the aSi:H layer defines the mode confinement factor in the quantum wells in our partial coupling design. Trading off these factors, a 330-nm aSi:H layer was chosen.

B. Coupling Loss and Fabrication Tolerance

The coupling efficiency and back reflection of the proposed coupling structure are then simulated using the Ansys

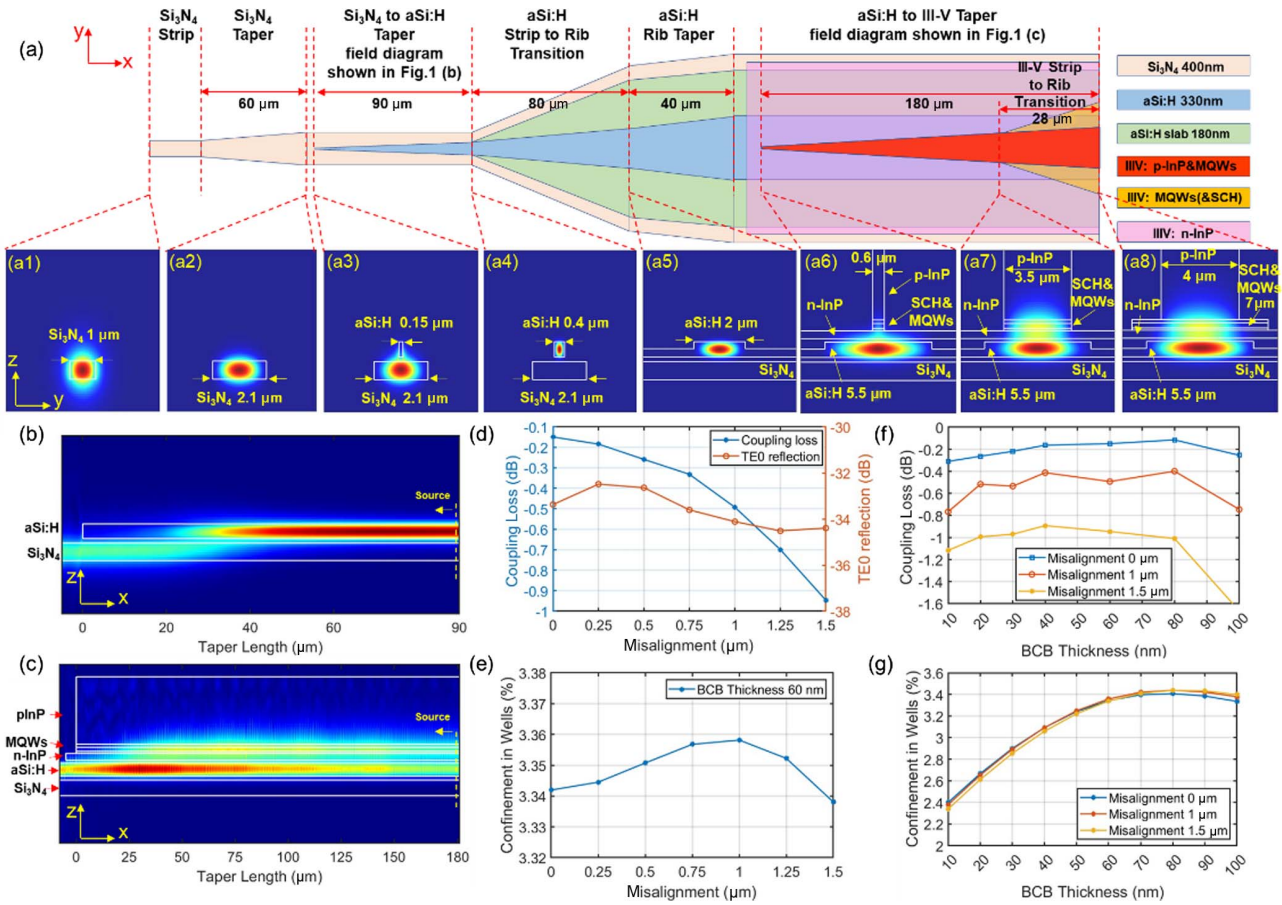

Fig. 1. (a) Schematic diagram of the Si_3N_4-to-aSi:H-to-III-V coupler. (a1)–(a8) Fundamental TE (TE0) modes at different cross-sections along the coupler (SCH, separate-confinement heterostructure; MQWs, multi-quantum wells). Field plots of (b) aSi:H-to-Si_3N_4 coupling and (c) III-V-to-aSi:H coupling along the cross-section. (d) Coupling loss and TE0 reflection and (e) optical confinement in wells as a function of lateral misalignment for the III-V-to-aSi:H coupler. (f) Coupling loss and (g) optical confinement in wells as a function of BCB thickness under different lateral misalignments for the III-V-to-aSi:H coupler.

Lumerical 3D FDTD solver [19], where the refractive indices of aSi:H, SiO_2, and Si_3N_4 were measured by ellipsometry, which are 3.544, 1.444, and 1.988, respectively, at 1550 nm. The refractive indices of III-V layers were calculated using the Tanguy model with parameters given in Ref. [20]. The detailed III-V epitaxial stack can be found in our previous publication [21]. The thicknesses of the MQWs and n-InP are 106 nm (barriers: 7 × 10 nm; wells: 6 × 6 nm) and 200 nm, respectively. Figures 1(b) and 1(c) show the simulated field plots of the two coupling stages along the cross-section, for coupling from III-V to Si_3N_4 waveguide. In the case of perfect lateral alignment, coupling efficiencies as high as 99.31% and 96.62% are achieved for the aSi:H-to-Si_3N_4 and III-V-to-aSi:H taper structures, respectively, while the corresponding reflections to the TE0 mode are −43.12 dB and −33.37 dB, respectively. In the simulation, the absorption loss from III-V layers and the side-wall scattering loss were not accounted.

As the coupling between aSi:H and III-V waveguides is implemented through heterogeneous integration, lateral misalignment [misalignment in the y direction shown in Fig. 1(a)] tolerance is crucial for the device uniformity in high-throughput wafer-level integration. In the case of lateral misalignment, the coupling efficiency drops mainly due to the reduction of the mode overlap between the two waveguides. When they are completely separated, the power coupling will tend to zero. In order to alleviate mode decoupling under lateral misalignment, we propose to use a wide aSi:H waveguide of 5.5 μm in the coupling structure. Figure 1(d) shows the coupling loss and TE0 reflection of the proposed coupler versus lateral misalignment. As can be seen, when the misalignment is within 1.5 μm, a coupling loss smaller than −0.97 dB and TE0 reflection below −32 dB can be expected. Figure 1(e) shows the optical confinement in quantum wells of the TE0 mode as a function of lateral misalignment. Benefiting from the wide aSi:H waveguide underneath, up to 1.5-μm misalignment can be tolerated with a small confinement variation within 0.02%.

Another critical point of fabrication is the tolerance to the thickness of the DVS-BCB bonding layer. Figures 1(f) and 1(g) show the simulated coupling efficiency and optical confinement as a function of DVS-BCB thicknesses under different

lateral misalignments. According to the simulation, the coupling loss stays less than −1 dB, and the optical confinement stays higher than 3% for DVS-BCB layer thickness varying from 40 to 100 nm when the lateral misalignment is below 1 μm.

3. LASER CAVITY DESIGN

A. Laser Architecture

Figures 2(a) and 2(b) show a microscope picture of the proposed tunable laser and the corresponding schematic diagram of the cavity structure, respectively. The gain section consists of an aSi:H rib waveguide with an InP coupon micro-transfer-printed on top. A $4 \times 840\ \mu m^2$ gain mesa together with 180-μm-long tapers at each side is used to provide sufficient gain for lasing and realize optical coupling between the coupon and aSi:H waveguide. In the laser cavity, the building blocks, including the MRRs, multimode interferometers (MMIs), connection waveguides, and grating couplers, are constructed in the Si_3N_4 layer. The left mirror comprises cascaded tunable add-drop MRRs with a total reflection Sagnac loop, which realizes both longitude mode selection and a wide tuning range through the Vernier effect. Tuning of its reflection spectrum is done by using the thermo-optic effect through the micro-heater that is defined on each ring. On the right side, a Mach–Zehnder interferometer (MZI) with a loop reflector is employed to form a mirror with controllable reflectivity. A thermal phase tuning section on Si_3N_4 is implemented between the gain and left mirror to align the longitudinal cavity mode with the Vernier resonance. Taking advantage of the tightly confined Si_3N_4 waveguide, the overall chip size is 5.6 mm × 0.8 mm, which is much more compact compared to the laser cavity on the shallow etched silicon waveguide [11,22].

B. Micro-Ring Resonator on Si_3N_4

When designing an MRR for an tunable laser, there is a tradeoff between quality factor (Q-factor) and insertion loss. For a symmetrical add-drop ring with the same coupling ratio in both directional couplers, the loaded Q-factor and the drop-port loss ($T_{d,\mathrm{res}}$) versus self-power coupling ratio (γ) at different waveguide losses (α) are shown in Figs. 3(a) and 3(b), respectively. The calculation is carried out based on Eqs. (1) and (2) [23]:

$$T_{d,\mathrm{res}} = \frac{(1-\gamma)^2 a}{(1-\gamma a)^2}, \tag{1}$$

$$Q = \frac{\pi n_g L \sqrt{\gamma a}}{\lambda_{\mathrm{res}}(1-\gamma a)}, \tag{2}$$

where a is the single-pass amplitude transmission coefficient, which can be expressed as $a = \exp(-\alpha L/2)$. L is the circumference of the ring, where the radius is set as 100 μm. λ_{res} and n_g are the resonance wavelength and group index, respectively. The corresponding measurement results are shown as the stars in the same figures, which are extracted from the fabricated MRRs with a range of gaps between the ring and bus waveguide, as shown in Fig. 3(c). The measured drop port loss shown in Fig. 3(b) indicates a Si_3N_4 waveguide loss of between 0.1 dB/cm and 0.6 dB/cm. Figure 3(d) shows a measured pass-port spectrum of a 600-nm-gap MRR and its theoretical fitting, where a loaded Q-factor of 47,300 is achieved. In order to achieve high Q-factor together with low loss, an MRR with 96% self-power coupling is chosen for a compact ring with a 100-μm radius, where the drop port loss per MRR is about −0.3 dB.

C. Vernier MRRs on Si_3N_4

A cascade of two MRRs together with a full-reflection Sagnac loop is used to form the mode-selective reflection mirror in the

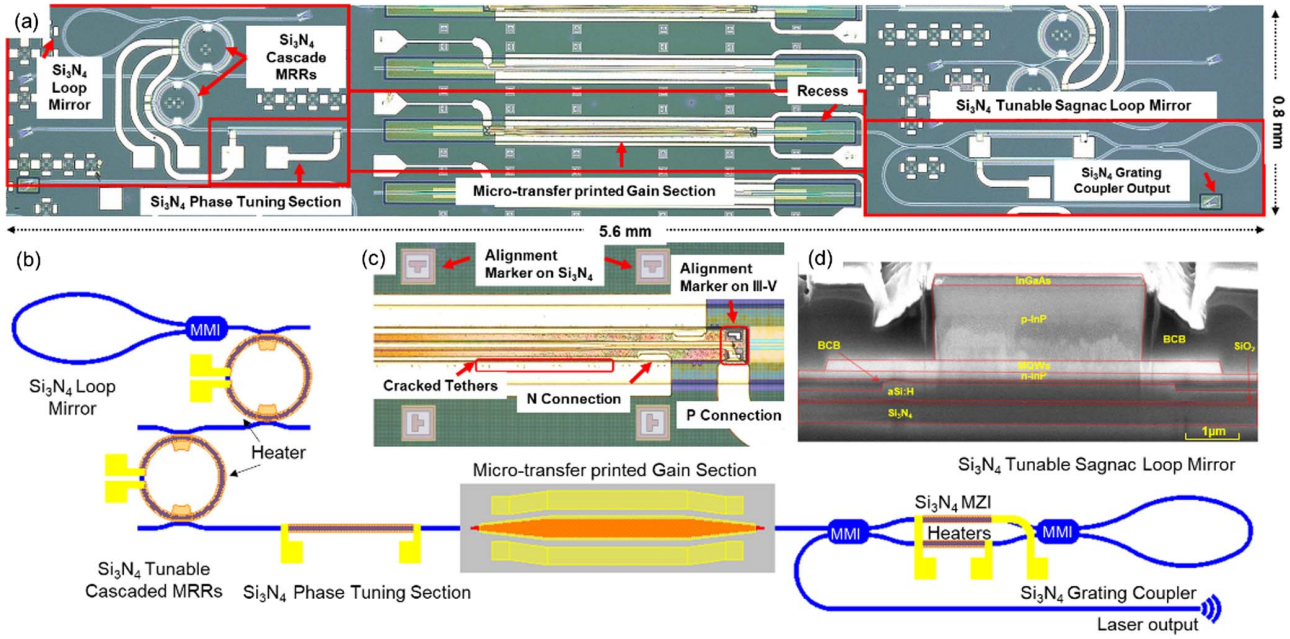

Fig. 2. (a) Microscope picture of the proposed tunable laser. (b) Corresponding schematic diagram of the cavity structure (MRR, micro-ring resonator; MMI, multimode interferometer). (c) A zoom-in view of the micro-transfer-printed III-V gain section on aSi:H/Si_3N_4 waveguides. (d) SEM image of a cross-section of the micro-transfer printed III-V gain element on the aSi:H/Si_3N_4 waveguide.

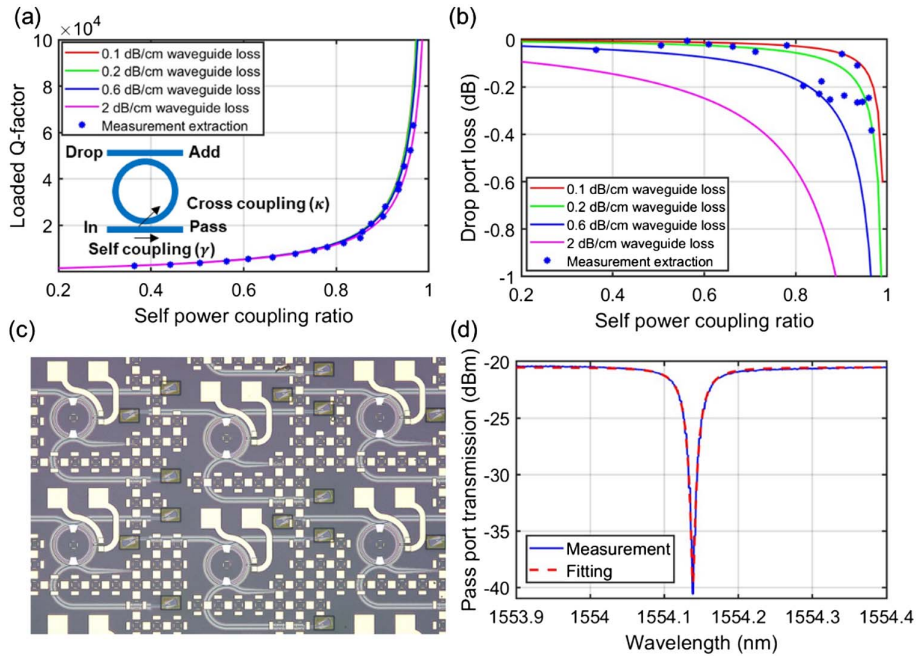

Fig. 3. Calculated and measured loaded quality factor (a) and drop port loss (b) as a function of self-power coupling ratio. (c) A microscope picture of the MRR test structure. (d) A measured pass-port spectrum of a 600-nm-gap MRR and its theoretical fitting.

laser cavity. The combination of the MRRs and the loop mirror has two configurations. The MRRs can be placed inside the loop, as shown in Fig. 4(a), or followed by a separated loop mirror, as shown in Fig. 4(b). When the two MRRs have slightly different free spectral range (FSR), an extended Vernier FSR can be achieved in both structures. Figure 4(c) shows a typical reflection spectrum of the latter structure with the two radii being 100 μm and 107.45 μm, respectively. When the same MRRs are employed in both structures, the optical mode will pass through the MRRs twice per round trip in the MRR followed by a loop mirror configuration, which would strengthen the mode selection ability and increase the photon lifetime. Comparisons of the reflection spectra and the effective lengths of the two reflectors are shown in Figs. 4(d) and 4(e), respectively. The Vernier inner side mode suppression ratio [Vernier inner SMSR, as marked in Fig. 4(c)] is significantly enhanced, with a doubled effective length at the resonance peak, in the structure of MRRs followed by a loop mirror. However, its disadvantage is the increase of the insertion loss, as the zoom-in view at the resonance peak shown in Fig. 4(f). Benefiting from the ultra-low-loss Si_3N_4 waveguides and the low-loss MRRs discussed above, the structure of MRRs followed by a loop mirror exhibits a small loss penalty of about −0.6 dB and is used in the laser structure in this work. The loss penalty would increase with the increasing Si_3N_4 waveguide loss, as shown in Fig. 4(g).

As the cascaded MRRs operate as the longitudinal mode filter in the laser cavity, the Vernier SMSR is a decisive factor for stable single-mode lasing. In order to enhance the Vernier inner SMSR, narrowing the bandwidth of the MRRs' resonances or increasing their separation is required. The resonance bandwidth corresponds to its Q-factor, which has a tradeoff with the insertion loss as has been discussed above. Increasing the MRRs' separation means increasing the FSR difference between the two MRRs, which can be realized by increasing the radius difference or by reducing the radius of both rings. However, large radius difference leads to small Vernier FSR, which normally limits the wavelength tuning range and would cause multimode lasing due to multiple Vernier periods existing within the gain bandwidth. Small rings have limited effective length, which affects the linewidth narrowing. Figure 5(a) shows the tradeoff between Vernier inner SMSR and Vernier FSR by sweeping the radius difference between the two MRRs. The calculation is carried out based on the structure shown in Fig. 4(b). While small rings with large radius difference exhibit excellent side mode suppression ability, MRRs with small radius difference are typically used to achieve large Vernier FSR.

Here, we propose to use Vernier MRRs with large radius difference to realize a wide tuning range. Its wavelength tuning can be extended among multiple Vernier periods, which breaks the tradeoff between the Vernier FSR and Vernier inner SMSR. The reflection spectrum of a cascade of MRRs with 100/107.45 μm radius is given in Fig. 4(c). Only one resonant peak dominates the spectrum rather than a series of resonant peaks with identical intensity and constant FSR. The Vernier outer SMSR is larger than 17 dB over 100-nm wavelength range. This superior Vernier outer side peak suppression ability is caused by the dispersion of mode refractive index with wavelength as shown in Fig. 5(b), a simulation performed by Ansys Lumerical Mode solver based on the material refractive index measured by ellipsometry. As shown in Fig. 4(c), when the refractive index dispersion is considered, the FSR of each MRR varies with wavelength. When the spectra of two MRRs align at one wavelength, they do not perfectly align at that wavelength

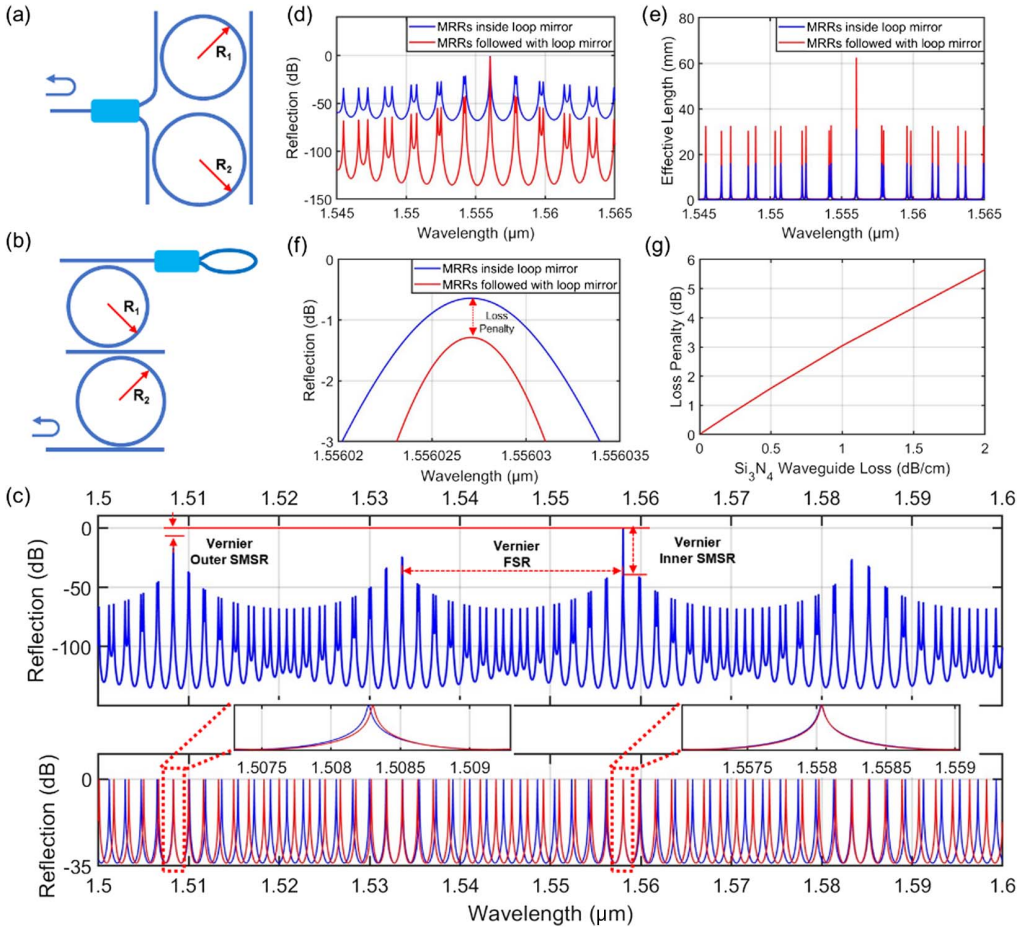

Fig. 4. (a) Schematic structure of MRRs inside the loop mirror. (b) Schematic structure of MRRs followed by a loop mirror. (c) A typical reflection spectrum of a cascade of MRRs followed by a loop mirror [structure in (b)], and the corresponding reflection spectrum of each MRR. Comparison of the reflection spectra (d) and the effective lengths (e) of the structures depicted in (a) and (b) when the same MRRs are employed in both structures. (f) A zoom-in view of the reflection spectra at the resonance peak. (g) Loss penalty as a function of Si_3N_4 waveguide loss.

position shifted by the Vernier FSR anymore, which induces addition wavelength selection. To verify the effectiveness of wavelength filtering over a wide tuning range, the Vernier outer SMSRs and the corresponding reflection spectra in a wavelength range of 1520 nm to 1600 nm are shown in Figs. 5(c) and 5(d), respectively, which are calculated by tuning the refractive index of one MRR. Lasing outside of the simulated band can be effectively suppressed by the shape of the gain spectrum and continuous tuning between each two adjacent wavelengths can be realized with the same Vernier outer SMSR by tuning the two MRRs simultaneously. A zoom-in view of resonance peaks is shown in the upper part of Fig. 5(d). Wavelength tuning over the whole simulation range with an amplitude variation below 1.7 dB and a Vernier outer SMSR over 11 dB is expected.

4. MICRO-HEATER DESIGN

A. Theory

In order to achieve wavelength tuning and maintain high Q-factor, micro-heaters are typically placed on top of the MRR waveguides to change their refractive index by using thermo-optic effect. Limited by the poor thermo-optic coefficient of Si_3N_4 material (2.45×10^{-5} K^{-1} [24]), thermal tuning of Si_3N_4 waveguides requires more design considerations compared with silicon waveguides. To be able to tune the MRR resonance over one FSR, a 2π phase shift is required, where both the heating efficiency and the heater's maximum power handling ability need to be carefully designed. We start with a general discussion on the design concepts of a micro-heater, which separately considers the effects of the two thermal resistances: the thermal resistance between the micro-heater and the substrate ($R_{\text{heater/Sub}}$), and the thermal resistance between the micro-heater and the waveguide ($R_{\text{heater/waveguide}}$).

The thermal power requirement for 2π phase shift ($P_{2\pi}$) of a waveguide can be defined as [25]

$$P_{2\pi} = \frac{\Delta T_{2\pi,\text{heater}} A_{\text{heater}}}{R_{\text{heater/Sub}}}, \tag{3}$$

where $\Delta T_{2\pi,\text{heater}}$ is the temperature rise of the micro-heater to achieve 2π phase shift, and A_{heater} is the area of the micro-heater traversed by the heat flow, which equals the product of heater length (L_{heater}) and width (W_{heater}). Given the micro-heater and the waveguide are separated by cladding layers, their

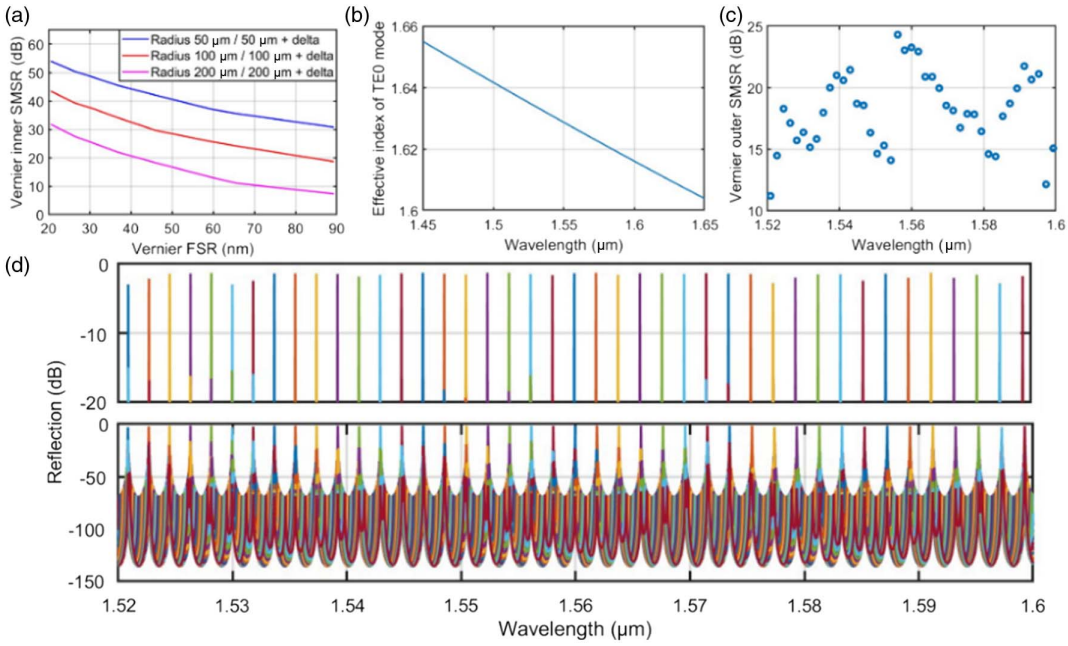

Fig. 5. (a) Vernier inner SMSR as a function of Vernier FSR for different radii (delta: radius difference between the two MRRs, which varies with the Vernier FSR). (b) Effective index dispersion of the Si_3N_4 waveguide. (c) Vernier outer SMSR as a function of resonant wavelengths while tuning the refractive index of one MRR. (d) Corresponding reflection spectra at different resonant wavelengths (upper part: a zoom-in view of resonance peaks).

temperature gradient ($\Delta T_{2\pi,\text{heater}} - \Delta T_{2\pi,\text{waveguide}}$) is determined by the thermal resistance between them as

$$\Delta T_{2\pi,\text{heater}} - \Delta T_{2\pi,\text{waveguide}} = \frac{P_{2\pi} R_{\text{heater/waveguide}}}{A_{\text{heater}}}. \quad (4)$$

In Eq. (4), the 2π waveguide temperature increase can be expressed as $\Delta T_{2\pi,\text{waveguide}} = \lambda / \left(L_{\text{heater}} \frac{dn}{dT} \right)$, where λ is the operation wavelength and dn/dT is the thermo-optical coefficient of the waveguide. By combining Eqs. (3) and (4), $P_{2\pi}$ can be expressed as

$$P_{2\pi} = \frac{\lambda}{\frac{dn}{dT}} \times W_{\text{heater}} \times \frac{1}{R_{\text{heater/Sub}} - R_{\text{heater/waveguide}}}. \quad (5)$$

Equation (5) indicates that reducing the thermal resistance between the micro-heater and waveguide, enhancing the thermal isolation of the micro-heater, and narrowing the heater width are the requisites to improve the thermo-optic efficiency.

B. Micro-Heater Design

In order to study how the waveguide structure affects the thermal resistances and optimize the heater efficiency, a cross-section of the micro-heater on the Si_3N_4 waveguide is simulated with the combination of a thermal solver and an optical mode solver in the Ansys Lumerical Device [19].

In the simulation, the temperature distribution on the waveguide cross-section is calculated using a steady-state heat transport solver. Then, the refractive index change of each mesh point induced by the temperature increase is implemented in the eigenmode solver to calculate the mode effective index and phase shift versus heater power. The temperature at the bottom of the thermal simulation region is fixed to 300 K, and the convection between the oxide layer and air above it is set as 10 $W/(m^2 \cdot K)$. The material properties used in the simulation are listed in Table 1.

Figure 6(a) shows the simulated temperature distribution of the waveguide cross-section at 2π phase shift, and Fig. 6(b) shows the phase shift of the fundamental TE mode versus heater power. A residual aSi:H layer adjacent to the Si_3N_4 waveguide is from a previous iteration and does not affect the subsequent discussion. The impact of the top oxide layer (TOX) thickness and lateral offset between the heater and waveguide on the performance is then simulated as shown in Figs. 6(c)–6(f).

Since the metal layers are highly absorptive, there is always a tradeoff between optical loss and how close can the heater and the waveguide be to reduce the thermal resistance between them. The extra loss, that is the difference between the waveguide with and without the heater, is simulated by considering the imaginary part of the refractive index of the metal layers in the optical mode solver. As shown in Fig. 6(c), the 2π phase shift power slowly increases with the thickness of the TOX due to its influence on both the $R_{\text{heater/Sub}}$ and $R_{\text{heater/waveguide}}$. Increasing the TOX thickness would benefit the waveguide loss, but inevitably increase the required temperature on the heaters [Fig. 6(d)], which affects the power handling of the heater [26]. After tradeoff of metal loss and heater temperature, a 1.58-μm-thick TOX is chosen.

Figure 6(e) shows the heater efficiency and extra loss versus the lateral offset between the center of the micro-heater and the Si_3N_4 waveguide under a fixed TOX thickness. It can be seen

Table 1. Thermal and Electrical/Optical Properties of Materials Used in FEM Simulations

Material	Density (kg/m^3)	Specific Heat [$J/(kg \cdot K)$]	Thermal Conductivity [$W/(m \cdot K)$]	Conductivity (S/m)	n @1550 nm	k @1550 nm
Si	2330	711	148	3.11×10^{-4}	3.477	0
SiO_2	2203	709	1.38	1×10^{-15}	1.444	0
Si_3N_4	3100	787	18.5	1×10^{-13}	1.9876	0
Ti	4506	720	21.9	2.38×10^{7}	4.04	3.82
Au	19,300	129	316	4.005×10^{7}	0.559	9.81

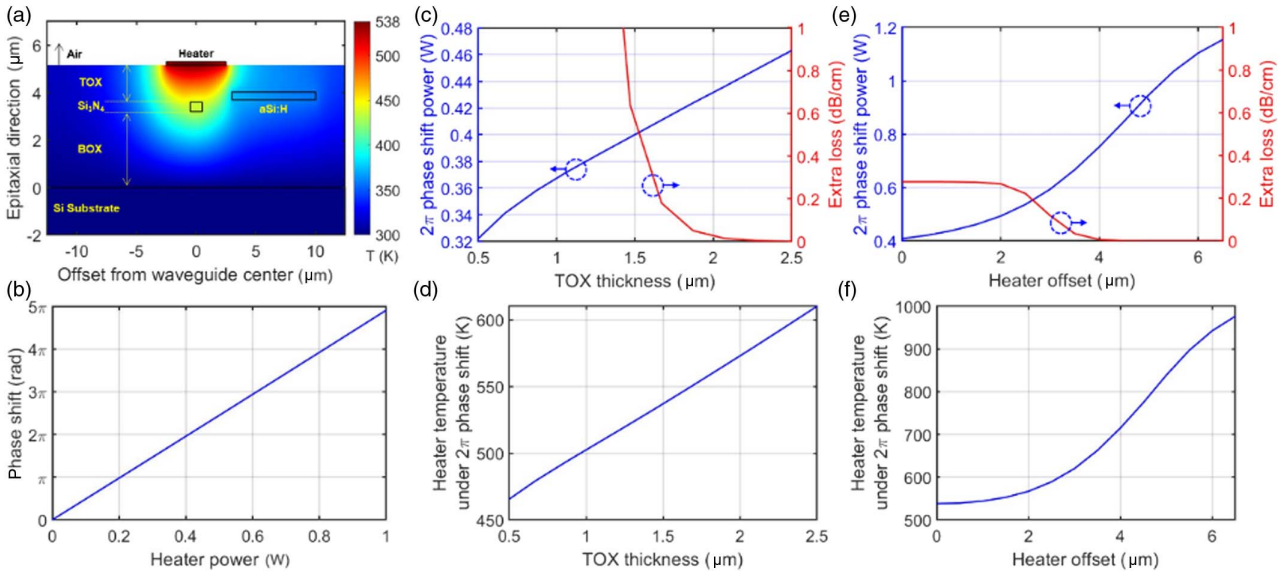

Fig. 6. (a) Simulated temperature distribution of the waveguide cross-section. (b) Phase shift of fundamental TE mode versus heater power. (c) 2π phase shift power and extra waveguide loss as a function of TOX thickness. (d) Heater temperature under 2π phase shift power as a function of TOX thickness. (e) 2π phase shift power and extra waveguide loss as a function of heater offset. (f) Heater temperature under 2π phase shift power as a function of heater offset.

that moving the heater away from the waveguide reduces the extra loss, but with a corresponding increase of 2π phase shift power and heater temperature. The rapid increase in 2π phase shift power also indicates a small thermal crosstalk.

Increasing the BOX layer thickness could also enhance the heater efficiency. It is, however, fixed to 3.2 μm to prevent mode leakage to the substrate and avoid further increasing the thermal resistance of the III-V gain section. Undercutting the heaters by etching the silicon substrate can locally increase the $R_{\text{heater/Sub}}$ and greatly reduce the 2π phase shift power, but this is beyond the scope of our current process flow. According to Eq. (5), a narrower heater width could also enhance the efficiency, but it will increase the current density on the micro-heater, and thus affects its maximum power handling ability [26]. Considering both current density and the used contact-litho-based micro-heater lift-off process, a 5-μm-wide heater is chosen.

C. Micro-Heater with Locally Reduced Resistance

When using a micro-heater to tune an MRR that includes a circular cavity and couplers, the coupling ratio of the coupler would unintentionally change during the tuning of the waveguide. In order to avoid the shift of the coupling ratio, we propose to locally reduce the heater resistance near the coupler, as in the schematic shown in Fig. 7(a). The simulated temperature distribution in the top view is shown in Fig. 7(b), where the temperature rise around the coupler is greatly reduced. A standalone add-drop MRR with the proposed micro-heater, as shown in Fig. 7(c), is then implemented to measure its tuning efficiency. Figure 7(d) shows the pass-port transmission spectra of the MRR with the tuning of the micro-heater. As a summary of the phase shift versus thermal power shown in Fig. 7(e), about 425 mW is required for a 2π phase shift, which is consistent with the simulation. The extracted loaded Q-factor versus thermal power stays around 47,000, which reflects a stable coupling ratio during the thermal tuning.

5. LASER FABRICATION

The integration of the III-V gain section on top of the silicon waveguide structure is based on MTP. And the principle of MTP is based on the switchable adhesion of an elastomeric poly-dimethylsiloxane (PDMS) stamp to the device of interest. The process starts with the fabrication of printable III-V structures (referred to as "coupons") on their native substrate (referred to as "source wafer"). Figures 8(a)–8(h) show the

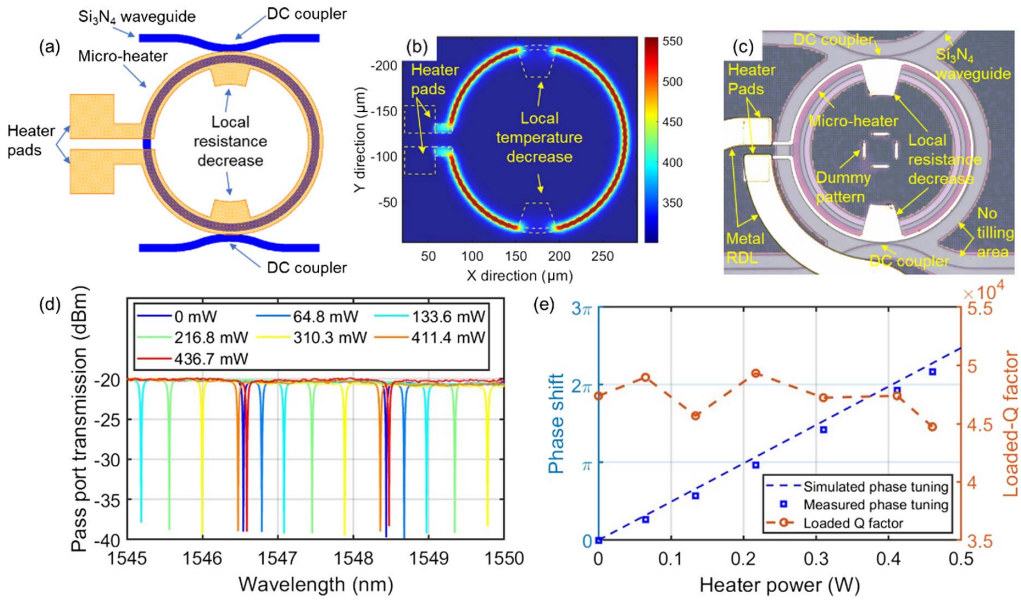

Fig. 7. (a) Schematic diagram of the micro-heater on the MRR. (b) Simulated temperature distribution on top of the MRR. (c) Microscope picture of a standalone MRR for tuning efficiency measurements. (d) Pass-port transmission spectra under heater tuning. (e) Simulated and measured phase shift and extracted loaded Q-factor as a function of heater power.

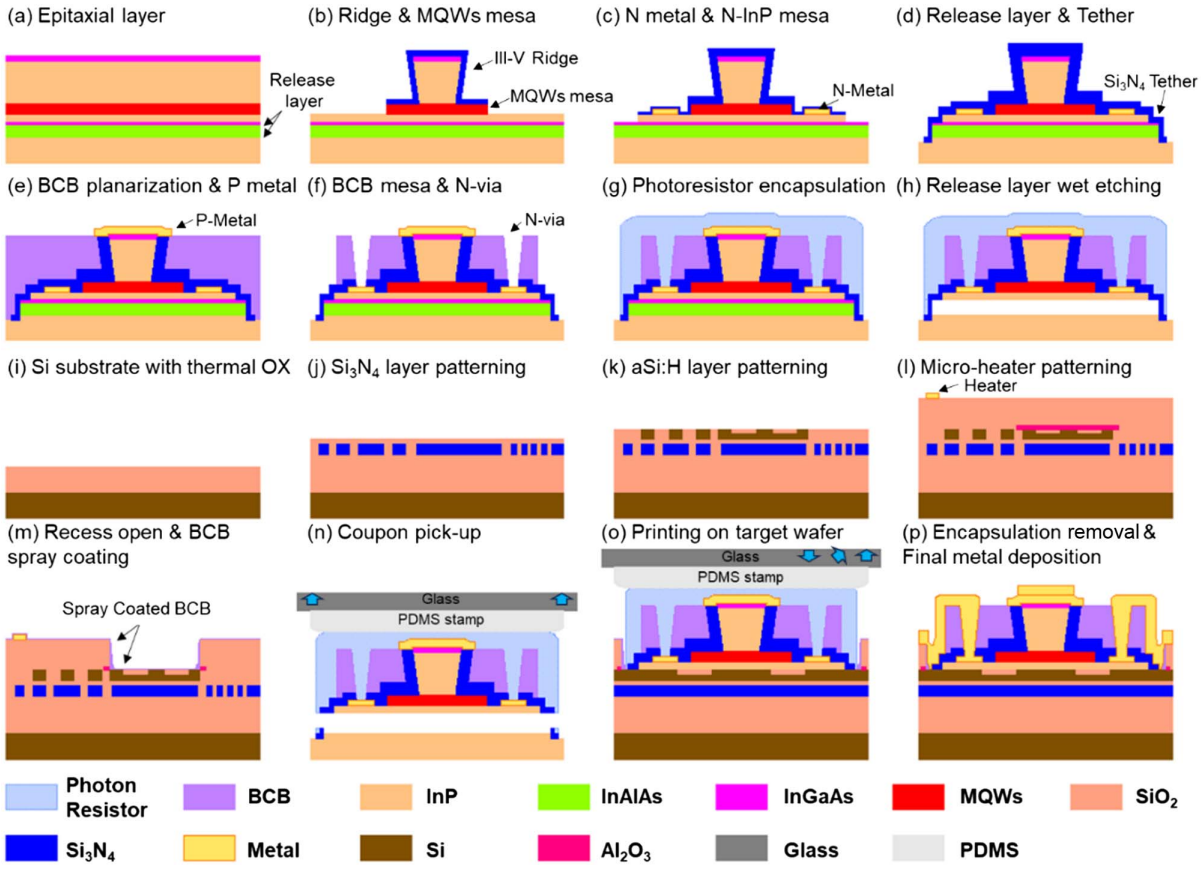

Fig. 8. Schematic process flow of (a)–(h) active coupons on III-V-substrate for micro-transfer printing, and (i)–(m) Si_3N_4/aSi:H circuits and preparation on the target substrate, and (n)–(p) heterogeneous integration and postprocessing.

schematic process flow on the source wafer, which is carried out by III-V Lab. In the layer stack [Fig. 8(a)], release layers consisting of a 50-nm-thick InGaAs layer and a 500-nm-thick InAlAs layer are inserted, which are chosen for their high etching selectivity against with InP. First, the ridge waveguide and MQWs mesa were patterned [Fig. 8(b)]. Followed by the n-side metal deposition and lift off, the n-InP layer was patterned to define the device island [Fig. 8(c)]. Next, the release layers were patterned, and the tethers were defined by Si_3N_4 deposition and dry etching [Fig. 8(d)]. Then, the whole device was planarized with a thick layer of DVS-BCB. After thinning the DVS-BCB and exposing the p-side contact layer, the p-metal was defined by lift-off [Fig. 8(e)]. After that, vias were opened to reach the n-metal. At the same time, a DVS-BCB mesa was defined to give access to the release layers [Fig. 8(f)]. Prior to the release etching, a layer of photoresist was spin-coated and patterned to encapsulate the whole coupon, which partially planarizes the top surface and reinforces the tethers [Fig. 8(g)]. The release layers were then selectively under-etched in a $FeCl_3$:H_2O solution, leaving the coupons suspended and kept in place by the tether structures [Fig. 8(h)]. After release etching, the coupons are ready for printing. During the coupon preparation, there are no restrictions on the waveguide structures and top surface, which means the proposed process flow is compatible with different kinds of InP-based devices, such as modulators and photodetectors. Moreover, all the III-V-based processes are done on the source wafer, which indicates that different III-V devices can be integrated on the Si/Si_3N_4-based photonic circuits simultaneously without increasing the process complexity. This advantage is crucial for the Si_3N_4 platform since it is purely passive and requires all the active building blocks.

In this work, the Si_3N_4 photonic circuits (referred to as "target wafers") were fabricated on IMEC's 200-mm pilot line. A schematic process flow of the target wafer is shown in Figs. 8(i)–8(m). It started from a silicon substrate with 2.5-μm thermal oxide [Fig. 8(i)]. Afterwards, a 700-nm-thick SiO_2 layer and a 400-nm-thick Si_3N_4 layer were deposited using high temperature PECVD and LPCVD, respectively, followed by annealing. Subsequently, Si_3N_4-based structures were patterned through DUV lithography and dry etching [Fig. 8(j)]. The same high-temperature PECVD SiO_2 layer was then deposited and the wafer was planarized by chemical mechanical polishing (CMP), which stopped 100 nm above the Si_3N_4 waveguide layer [Fig. 8(j)]. Next, a 330-nm-thick aSi:H layer and a 100-nm Si_3N_4 hard mask layer were deposited using PECVD. After patterning both the rib and strip waveguides on the aSi:H layer, the wafer was planarized again through low-temperature PECVD-based SiO_2 deposition and CMP, followed by an etch-back to remove the remaining Si_3N_4 hard mask on top of the aSi:H waveguide [Fig. 8(k)]. Hereafter, the wafer was cleaved into individual samples for further processing. A 50-nm Al_2O_3 etch stop layer was then deposited using an e-beam evaporator. After patterning the Al_2O_3 layer through wet etching, a PECVD-based 1.15-μm top oxide layer was deposited and the micro-heater was then defined on top [Fig. 8(l)]. Next, a local recess was opened on the top oxide through dry etching, which exposes the aSi:H waveguide for evanescent coupling [Fig. 8(m)]. The Al_2O_3 is used as the etch stop layer to maintain the quality of the surface in the recess for the following bonding process. Then, the Al_2O_3 inside the recess was etched away and a thin DVS-BCB adhesive layer with a thickness of 100 nm was spray-coated to have a high-yield printing process [Fig. 8(m)]. Buildup of the DVS-BCB at the side walls of the recess benefits the following metal connection. Before MTP, there was a soft bake of the spray-coated DVS-BCB bonding layer at 150°C.

After preparing the source and target samples, both of them were loaded into an X-Celeprint μTP-100 lab-scale printer. A single post PDMS stamp was used to pick up a 1260 μm × 45 μm coupon on the source. Although the single post stamp was used in this experiment, printing of multiple devices at the same time can be realized by using a dedicated stamp with multiple posts. In order to achieve accurate alignment, markers for digital pattern recognition are therefore defined on both the coupon and target wafer, as shown in Fig. 2(c). An alignment accuracy of 1.5 μm (3σ) can be achieved through the lab-scale printer, when the pick and printing processes are done at room temperature. After printing, the photoresist encapsulation layer was first removed by dry etching. Hereafter, the DVS-BCB layer is fully cured at 280°C. A scanning-electron microscope (SEM) image of a focused ion beam (FIB) cross-section of the integrated device after transfer printing is shown in Fig. 2(d). According to a zoom-in SEM image, the DVS-BCB layer shrunk to 80 nm after printing and curing. Finally, a thick layer of Ti/Au was deposited and lifted off to make electrical connection after removing the residual DVS-BCB layer where the metal wire passes. During printing and post-printing processing, there are neither processes for source and target materials, nor processes requiring high temperature, which means the source and target wafers can be fully implemented in their own established foundries, which greatly facilitates mass production and time to market.

6. LASER CHARACTERIZATION

The heterogeneously integrated tunable laser was electrically contacted through DC-probes on a temperature-controlled stage. The operation temperature was set to 15°C and controlled by a thermo-electric cooler (TEC). Multiple Keithley 2400 source-meters were used to bias the III-V gain section and the thermal phase tuning elements, including MRRs, phase shifter, and tunable loop mirror. The device was optically probed by a cleaved standard single-mode fiber through the grating coupler on the Si_3N_4 layer. A reference Si_3N_4 waveguide with the same grating coupler on both sides was fabricated on the sample to calibrate the coupling loss. Figure 9(a) shows a measured transmission spectrum of the reference waveguide, which indicates a −10 to −14 dB loss per grating coupler in a wavelength band of 1510 to 1590 nm. The laser output signal was characterized by an optical power meter (HP 8153 A) and an optical spectrum analyzer (Anritsu MS9740A).

Figure 9(b) shows a typical power-current-voltage (LIV) curve of the laser at an operation wavelength of 1571.56 nm. It can be observed that the threshold current is around 87.6 mA and the calibrated output power in the Si_3N_4 waveguide reaches 6.3 mW at 158.5-mA bias current. A coupling loss

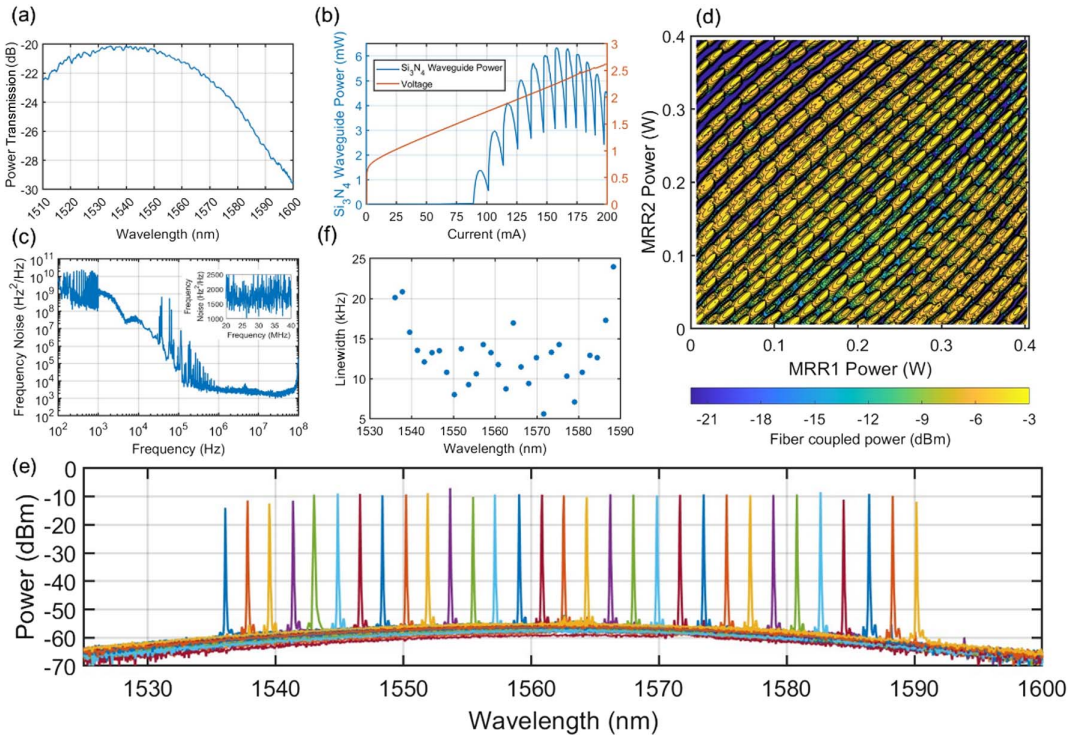

Fig. 9. (a) Transmission spectrum of the reference waveguide with grating couplers at both sides. (b) LIV curve of III-V on the Si_3N_4 tunable laser. (c) Laser frequency noise spectrum at 1571.56 nm (inset: zoom-in view of the spectrum from 20 MHz to 40 MHz). (d) Two-dimensional output power tuning map of the laser. (e) Optical spectra under different operation wavelengths. (f) Lorentzian linewidth as a function of wavelength.

of 11.2 dB is used in the calibration. The differential series resistance is about 9 Ω. During LIV measurement, only the gain current was swept with fixed biases of all the heaters. The periodic oscillation of the output power results from the phase change in the gain section, which shifts the position of cavity modes. High output power occurs when the cavity modes align with the MRRs' resonance, while low output occurs under mismatch. As the gain section sits on a thick buried oxide layer, thermal roll over starts at an electrical power dissipation of around 346 mW. The output power could be further improved by reducing the series resistance and the thermal resistance. The Si_3N_4 MRRs provide a high-Q cavity and enable a narrow laser linewidth. The frequency noise spectrum of the laser is measured using a commercial laser noise analyzer (OEwaves OE4000). Figure 9(c) shows a measured frequency noise spectrum, taken at 158.5-mA pump current and slightly detuned from the 1571.56-nm wavelength resonance peak. The insert shows a zoom-in view of the spectrum from 20 MHz to 40 MHz. The white-noise-limited frequency noise level is 1780 Hz^2/Hz, which corresponds to an intrinsic linewidth of 5.6 kHz. This linewidth can be influenced by the deviations of the MRR's self-power coupling ratio, as well as waveguide loss and coupling loss in the experiments.

Next, a two-dimensional sweep of the MRRs' heaters was carried out to achieve the tuning map for the laser. In the measurement procedure, the gain current was set at 158.5 mA and the biases of the phase tuning section and tunable loop reflector were fixed. By stepping the MRR heater bias in equal power amount, a tuning map of the fiber-coupled output power was obtained, as shown in Fig. 9(d). The variation in the output power originates from how well the spectra of the MRRs and the cavity modes are aligned to each other at the setpoints. The local peaks in the tuning map occur at precise alignment, which were extracted as the working points of the laser. The laser can be locked to such bias points through a feedback loop to get the preferred working conditions. Figure 9(e) shows optical spectra at different working wavelengths. A tuning range of 54 nm with SMSR larger than 40 dB is achieved. As we expected, the wavelength tuning breaks the limitation of Vernier FSR, which is about 25 nm in the laser design for two MRRs with a radius of 100 μm and 107.45 μm, respectively. It extends among three Vernier periods and further extension is blocked due to the limited gain bandwidth. The intrinsic linewidths at different wavelengths are measured, as shown in Fig. 9(f). Over the whole tuning range, the linewidth is below 25 kHz. The variation in linewidths at different wavelengths may result from imperfect operating points, and changes in the linewidth enhancement factor and output power at different locations on the gain curve.

One characteristic of the cascade MRRs-based laser is that the lowest linewidth occurs when the lasing wavelength is detuned to the longer wavelength side of the resonance, which is known as the detuned-loading effect [27]. This effect is observed in our measurement as shown in Fig. 10(a). The gain section was biased at a current of 158.5 mA and the microheaters of the two MRRs and phase section were tuned to

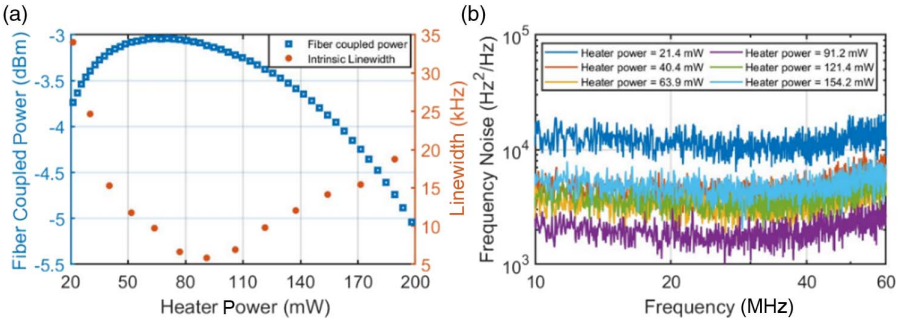

Fig. 10. (a) Fiber-coupled output power and laser linewidth as a function of heater power of phase tuning section. (b) Frequency noise spectra under different biases of phase tuning section.

obtain the maximum output power so that the resonance of cascade MRRs was aligned, and lasing occurred at the resonance peak. Then, the fiber-coupled output power and intrinsic linewidth were recorded with the tuning of the phase section heater power. As can be seen, it shows a clear detuning between the highest output power and the lowest linewidth. The linewidth increases rapidly at the negative side of the output power peak. In contrast, it decreases gradually to its lowest and then increases gradually under larger detuning on the positive side. The linewidth at the power peak is about 10 kHz, which is about twice the minimal value. The frequency noise spectra during the phase tuning are plotted all together in Fig. 10(b).

A tunable Sagnac loop is implemented as a reflectivity adjustable out-coupling mirror in the laser cavity. The mirror loss and hence the threshold and slope efficiency, can be optimized by controlling the phase difference between MZI arms. The effectiveness of this control is verified by sweeping its heater power after setting the bias points of the MRRs and phase tuning section at a gain current of 158.5 mA. Figure 11(a) shows the fiber-coupled output power as a function of heater power. The maximum output power is obtained at a small heater bias of 2.77 mW, which indicates a low mirror reflection for the unbiased MZI. The output can be nearly switched off at a heater power of 109.8 mW, where the loop works as a high-reflectivity mirror. By further increasing the heater bias, the output power gradually recovers with a sudden jump at ∼143 mW, which results from the switching between different longitudinal modes as an additional cavity phase is induced during the tuning of the MZI. Figure 11(b) shows the corresponding optical spectra at different MZI phases, where the amplified spontaneous emission floor varies due to the change of the threshold current. The working wavelength stays around the MRRs' resonance. The switch between longitudinal modes is not visualized due to the limited resolution of the optical spectrum analyzer. The LI curves at different biases of the tunable Sagnac loop mirror heater are plotted together in Fig. 11(c). The extracted threshold current and fiber-coupled slope efficiency are summarized in Fig. 11(d), showing

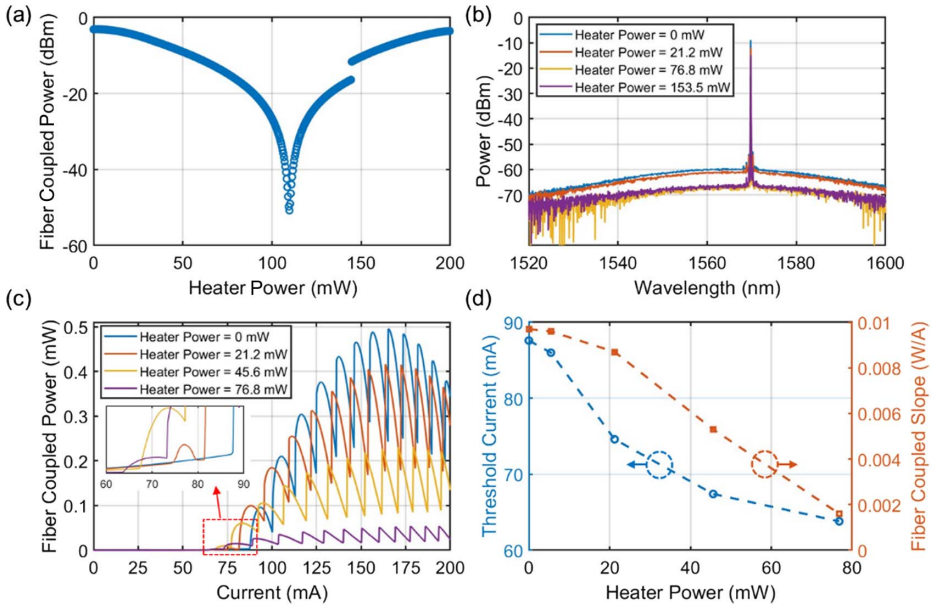

Fig. 11. (a) Fiber-coupled output power as a function of heater power on one MZI arm. (b) Optical spectra at different MZI phases. (c) LI curves at different biases of the heater (inset: zoom-in view of the curves from 60 mA to 90 mA). (d) Threshold current and fiber-coupled slope efficiency as a function of MZI heater power.

that the laser efficiency can be effectively optimized through the tunable loop mirror.

7. CONCLUSION

This paper demonstrates the design, fabrication, and characterization of a heterogeneously integrated narrow-linewidth tunable laser on IMEC's 200 mm silicon nitride platform through micro-transfer printing. By using a cascaded MRR mirror on low-loss Si_3N_4 waveguides, a wavelength tuning range of 54 nm in the C and L bands is achieved with a linewidth less than 25 kHz. By leveraging the dispersion of Si_3N_4 waveguide in the design, the proposed Vernier MRR structure extends the tuning range across multiple Vernier periods. By using a prefabricated III-V gain section and minimizing the post-printing processes, the quality control of both the III-V and Si_3N_4 fabrication is realized in its own foundry. The proof-of-concept heterogenous laser and the integration method therefore hold great potential for integrated photonic systems-on-a-chip applications.

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Disclosures. The authors declare no conflicts of interest.

Data Availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

REFERENCES

1. J. D. Reis, V. Shukla, D. R. Stauffer, *et al.*, *Technology Options for 400G Implementation* (OIF, 2015).
2. M. Cantono, R. Schmogrow, M. Newland, *et al.*, "Opportunities and challenges of C+L transmission systems," J. Lightwave Technol. **38**, 1050–1060 (2020).
3. M. Seimetz, "Laser linewidth limitations for optical systems with high-order modulation employing feed forward digital carrier phase estimation," in *Optical Fiber Communication/National Fiber Optic Engineers Conference* (2008), paper OTuM2.
4. W. Yi, Z. Zhou, Z. Liu, *et al.*, "Impact of laser phase noise on ranging precision within and beyond laser coherence length in FMCW LiDAR," in *Optical Fiber Communications Conference and Exhibition* (2023), paper M3F.3.
5. P. Lu, N. Lalam, M. Badar, *et al.*, "Distributed optical fiber sensing: review and perspective," Appl. Phys. Rev. **6**, 041302 (2019).
6. C. Xiang, W. Jin, O. Terra, *et al.*, "3D integration enables ultralow-noise isolator-free lasers in silicon photonics," Nature **620**, 78–85 (2023).
7. S. M. Kim, E. S. Lee, K. W. Chun, *et al.*, "Compact solid-state optical phased array beam scanners based on polymeric photonic integrated circuits," Sci. Rep. **11**, 10576 (2021).
8. A. E. Elsner and M. S. Muller, "Laser applications and system considerations in ocular imaging," Laser Photonics Rev. **2**, 350–376 (2008).
9. K. Wang, Q. Chen, C. Jiang, *et al.*, "Characterization of thermo-optically tuned multi-channel interference widely tunable semiconductor laser for quasi-continuous tuning," J. Lightwave Technol. **41**, 3084–3093 (2023).
10. D. Huang, M. A. Tran, J. Guo, *et al.*, "High-power sub-kHz linewidth lasers fully integrated on silicon," Optica **6**, 745–752 (2019).
11. M. A. Tran, D. Huang, J. Guo, *et al.*, "Ring-resonator based widely-tunable narrow-linewidth Si/InP integrated lasers," IEEE J. Sel. Top. Quantum Electron. **26**, 1500514 (2020).
12. J. Liu, G. Huang, R. Wang, *et al.*, "High-yield, wafer-scale fabrication of ultralow-loss, dispersion-engineered silicon nitride photonic circuits," Nat. Commun. **12**, 2236 (2021).
13. Y. Fan, A. van Rees, P. J. M. van der Slot, *et al.*, "Hybrid integrated InP-Si_3N_4 diode laser with a 40-Hz intrinsic linewidth," Opt. Express **28**, 21713–21728 (2020).
14. C. Xiang, W. Jin, J. Guo, *et al.*, "Narrow-linewidth III-V/Si/Si_3N_4 laser using multilayer heterogeneous integration," Optica **7**, 20–21 (2020).
15. C. Xiang, J. Guo, W. Jin, *et al.*, "High-performance lasers for fully integrated silicon nitride photonics," Nat. Commun. **12**, 6650 (2021).
16. M. A. Tran, C. Zhang, T. J. Morin, *et al.*, "Extending the spectrum of fully integrated photonics to submicrometre wavelengths," Nature **610**, 54–60 (2022).
17. C. Op de Beeck, B. Haq, L. Elsinger, *et al.*, "Heterogeneous III-V on silicon nitride amplifiers and lasers via microtransfer printing," Optica **7**, 386–393 (2020).
18. B. Pan, J. Bourderionnet, V. Billault, *et al.*, "III-V-on-silicon nitride narrow-linewidth tunable laser based on micro-transfer printing," in *Optical Fiber Communication Conference* (2023), paper Th3B.5.
19. Lumerical Inc., https://www.ansys.com/products/photonics (2024).
20. P. Runge and S. Seifert, "Refractive index of $In_{1-x-y}Al_yGa_xAs$ lattice-matched to InP," IEEE Photonics Technol. Lett. **34**, 483–486 (2022).
21. E. Soltanian, G. Muliuk, S. Uvin, *et al.*, "Micro-transfer-printed narrow-linewidth III-V-on-Si double laser structure with a combined 110 nm tuning range," Opt. Express **30**, 39329–39339 (2022).
22. P. A. Morton, C. Xiang, J. B. Khurgin, *et al.*, "Integrated coherent tunable laser (ICTL) with ultra-wideband wavelength tuning and sub-100 Hz Lorentzian linewidth," J. Lightwave Technol. **40**, 1802 (2022).
23. W. Bogaerts, P. De Heyn, T. Van Vaerenbergh, *et al.*, "Silicon microring resonators," Laser Photon. Rev. **6**, 47–73 (2012).
24. A. Arbabi and L. L. Goddard, "Measurements of the refractive indices and thermo-optic coefficients of Si_3N_4 and SiO_x using microring resonances," Opt. Lett. **38**, 3878–3881 (2013).
25. M. Jacques, A. Samani, E. El-Fiky, *et al.*, "Optimization of thermo-optic phase-shifter design and mitigation of thermal crosstalk on the SOI platform," Opt. Express **27**, 10456–10471 (2019).
26. Y.-K. Cheng, C.-H. Tsai, C.-C. Teng, *et al.*, *Temperature-dependent Electromigration reliability, Electrothermal Analysis of VLSI Systems* (Springer, 2002).
27. M. A. Tran, D. Huang, and J. E. Bowers, "Tutorial on narrow linewidth tunable semiconductor lasers using Si/III-V heterogeneous integration," APL Photonics **4**, 111101 (2019).