Low Frequency Noise Characterization of BEOL Metal-Insulator-Metal Capacitors

G. Giusi, N. Saini, K. Croes, I. Ciofi, G. Scandurra, C. Ciofi and D. Tierno

***Abstract*— Dielectrics are fundamental building blocks in both analog and digital electronic devices, serving various purposes, including insulating metal lines and interconnect levels in the back-end-of-line (BEOL). In this paper we investigate the leakage and low frequency noise (LFN) properties of three different types of dielectrics, from the low-*k* Organo-Silicate Glass (OSG3.0) and Silica (SiO_2) to the high-*k* Alumina (Al_2O_3). Test structures are large area (up to 200x200 μm^2) MIM capacitors, with TiN or TaNTa electrodes, that mimic well the BEOL architecture. In particular, to our knowledge, no LFN study has been reported for OSGs which are the most used class of dielectrics in the BEOL. From a physical side, Current-Voltage characterization reveals that in all three dielectrics the conduction is bulk dominated and assisted by traps, rather than limited by electrode injection. Low Frequency Noise measurements show a typical 1/*f* current power spectral density (S_I) for all three dielectrics with a strongly bias dependent *Gate Noise Parameter* $GNP \propto S_I/I^2$ (I being the DC current), suggesting a highly non-uniform energy trap distribution, especially for Al_2O_3 devices. SiO_2-based capacitors demonstrated the lowest leakage at equivalent fields and superior noise performance at comparable leakage currents. Al_2O_3 devices exhibited the highest leakage, while OSG3.0 samples showed the poorest noise characteristics, marked by pronounced electrical instability and non-stationary random telegraph signal (RTS) events.**

***Index Terms*— Metal Insulator Metal Capacitors, Leakage, Low Frequency Noise, Dielectric, Reliability, 1/f noise, DRAMs, Low Frequency Noise Measurements.**

I. Introduction

Dielectric materials are critical elements in a wide range of electronic devices [1], from complementary metal-oxide-semiconductor (CMOS) transistors [2] to dynamic random-access memories (DRAMs) [3], from NAND Flash Memories [4] to back-end-of-line (BEOL) interconnects [5]. The continuous evolution of transistor technology has necessitated dramatic scaling of interconnects [6], based on narrower metal lines, new integration approaches and new materials in the BEOL.

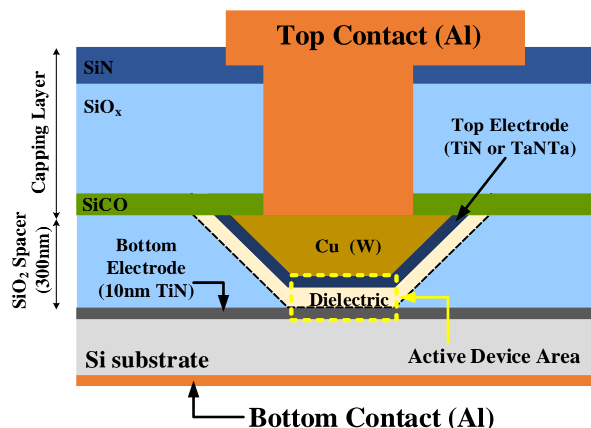

Fig. 1 - Schematic of the test vehicle used in the study. The MIM planar capacitors are defined within a deep oxide spacer. The top and bottom electrode are probed via Aluminum pads.

TABLE I

dielectric material	nominal thickness (t_{ox})	nominal relative permittivity(ε_r)	bottom electrode	top electrode
SiO_2	6 nm	4.2	TiN	TiN
Al_2O_3	5 nm	8.9	TiN	TaNTa
OSG3.0	12 nm	3.0	TiN	TiN

Metal-Insulator-Metal (MIM) structures investigated in this work (plate area from 20 x 20 μm^2 to 200 x 200 μm^2).

Porous organo-silicate glasses (OSGs) replaced SiO_2 as insulator in the lower metal levels because their lower *k*-value [5] allowed to reduce RC delay. Their reliability is a key challenge for interconnects [7, 8] and understanding the role of dielectric defects, as well as their behaviour at different stress conditions, is a key for future improvements. The characterization of dielectrics in complex device architectures, like transistors or memories, is always affected by the presence of other materials as well as by the integration methods and processes required for device manufacturing. Therefore, simpler Metal-Insulator-Metal (MIM) capacitors [9] are often used for fundamental studies while also allowing to capture the critical role played by the metal/electrode interface [9]. In this paper we study the electrical properties of three BEOL dielectrics, namely Alumina (Al_2O_3), Silica (SiO_2) and Organo-Silicate Glass

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G. Giusi (ggiusi@unime.it), G. Scandurra and C. Ciofi are with Dipartimento di ingegneria-University of Messina, Messina, Italy.
N. Saini (email: nishant.saini@imec.be) is with imec, 3001 Leuven, Belgium and also with the Department of Physics and Astronomy (Semiconductor Physics), Katholieke Universiteit Leuven, 3000 Leuven, Belgium.
K. Croes (email: kristof.croes@imec.be), I. Ciofi (email: ivan.ciofi@imec.be) and D. Tierno (email: davide.tierno@imec.be) are with imec, 3001 Leuven, Belgium.

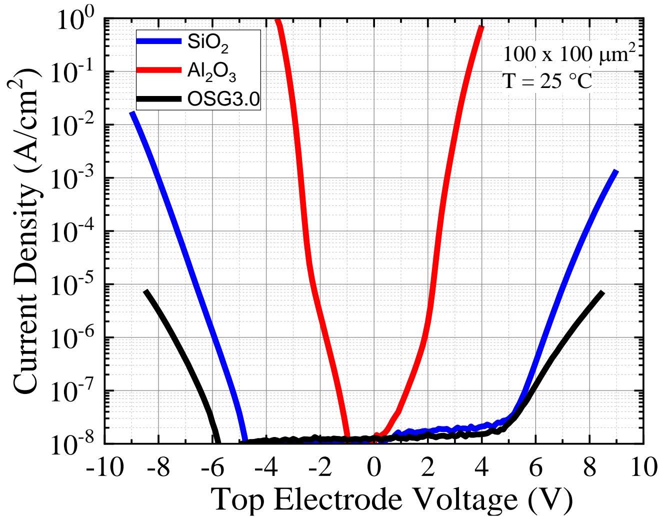

Fig. 2. Typical Current Density vs Top to Bottom Electrode Voltage (V) for the investigated structures at 25 °C (100 x 100 µm^2 plate area).

(OSG3.0), in large area (up to 200 x 200 µm^2) MIM Capacitors [9] with TiN (or TaNTa) electrodes. All three dielectrics have a wide bandgap (E_G > 8.5 eV), while the relative permittivity spans from the low values of OSG3.0 and SiO_2 (3.0 and 4.2 respectively) to the high value (8.9) of Al_2O_3. Most of reliability works on BEOL dielectrics, and in particular on OSG films [8-11], have been performed by using Time-Dependent Dielectric Breakdown (TDDB) measurements. In this work we perform the electrical characterization by means of Current-Voltage (IV) and Low Frequency Noise (LFN) measurements. In fact, while IV measurements are commonly used for electrical characterization of MIM capacitors, very few studies have been developed using LFN measurements (LFNMs) [12-16], notwithstanding the fact that LFNMs are a powerful tool to investigate material quality and charge transport mechanism involved in electronic devices. In particular, the rich LFN literature is focused especially on MOSFETs and, to a lesser degree on Metal-Insulator-Silicon (MIS) structures, with the objective of studying the Si/oxide interface [17-21]. This study aims to address this gap by providing a LFN analysis in OSGs, alongside more traditional dielectric materials like SiO_2 and Al_2O_3, in simple MIM structures. The remainder of this work is organized as stated in the following. In Section II details on samples characteristics and fabrication are given. In Section III we compare IV measurements at different temperatures to gain insights into the conduction mechanisms of the three dielectrics, while in Section IV we investigate them using low frequency noise measurements. Finally, in Section V, we draw our conclusions.

II. Device Structure and Preparation

The planar MIM capacitors [22] used in this study (Fig. 1) have areas ranging from 20 x 20 µm^2 to 200 x 200 µm^2 and were fabricated on device-grade silicon 700 µm-thick Si wafers, regularly used for advanced logic devices in imec 300mm pilot line. Three distinct classes of dielectrics were studied, namely SiO_2, Al_2O_3 and OSG3.0 with typical geometry and processing as shown in Table I. The choice of these three dielectric materials allows for a comprehensive comparison across a

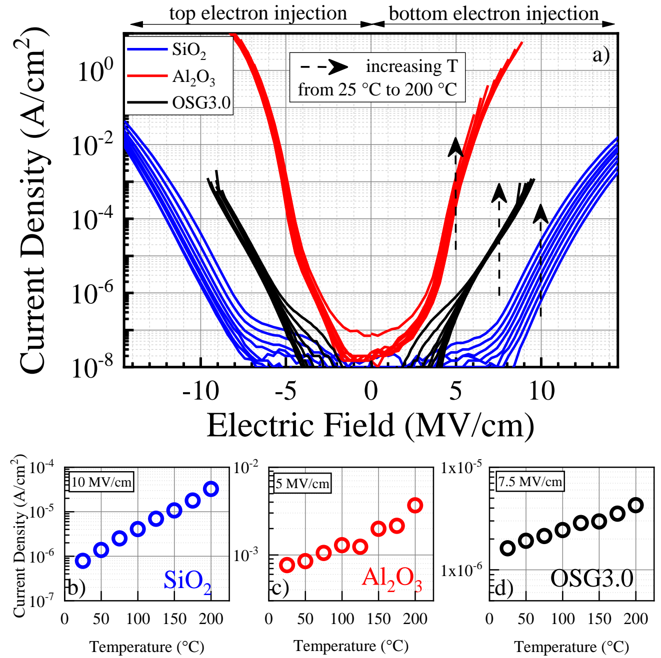

Fig. 3. a) Current Density (J) versus Electric Field ($E = V/t_{ox}$) at eight different temperatures (T) between 25 °C and 200 °C for the investigated samples; (b-d), J is plotted vs. T at a fixed E value (shown in the inset and correspondingly to the arrows location in (a)).

range of dielectric constants. In all the three cases, the bottom electrode (BE) consisted of a 10 nm thick TiN layer deposited by physical vapor deposition (PVD). The OSG3.0 was deposited by plasma-enhanced chemical vapor deposition (PECVD) while plasma-enhanced atomic layer deposition (PEALD) was used for Al_2O_3 and SiO_2 dielectrics. The deposition temperature for all three dielectric materials is compatible with a BEOL thermal budget, *i.e.* maximum 420 ºC. In particular, the PEALD Al_2O_3 (nominal thickness t_{ox} = 5 nm, ε_r = 8.9) was deposited at 300 ºC using a H_2O-based precursor; the film is amorphous as no post-deposition annealing was performed. The PEALD SiO_2 (t_{ox} = 6 nm, ε_r = 4.2) has also been deposited at 300 ºC. Finally, the OSG3.0 [11] (t_{ox} = 12 nm, ε_r = 3.0) was deposited by PECVD at 390 ºC without a subsequent curing step; the film has a 7 % porosity, and its relative permittivity was determined by Hg-probe and is estimated to be 3.0. Different metals were employed as top electrode (TE) for the three dielectrics. For SiO_2 and OSG3.0, a 10 nm thick ALD TiN layer was used while a 4 nm thick PVD TaNTa layer was instead deposited on top of the Al_2O_3 film. Fig. 1 highlights that the MIM is fabricated by depositing the dielectric in a cavity etched in a thick spacer. This approach minimizes damage to the dielectric during the patterning of the top electrode. The device structure was designed to ensure that the largest and uniform electric field would be within the "active device area". The sloped area (angle ≥ 45 °) is much smaller than the flat active area, approximately ~100 nm "extra" on each side of the active area and, in this region, the electric field decreases rapidly becoming negligible ensuring area scaling. Finally, the SiO_2/SiN capping layer prevents the absorption of moisture in the dielectric.

TABLE II

Mechanisms	Current density model
Poole-Frenkel	$J = q\mu N_C E \exp\left[-\frac{q\phi_T}{kT} + \frac{\beta\sqrt{E}}{kT}\right]$
FN-TAT	$J = \frac{q^3E^2}{8\pi h(q\phi_{TAT})}\exp\left[-\frac{8\pi(2qm_T)^{\frac{1}{2}}}{3hE}\phi_{TAT}^{3/2}\right]$
Hopping	$J = qanv \exp\left[\frac{qaE}{kT} - \frac{E_a}{kT}\right]$

Explored conduction mechanisms in the investigated samples. Symbols: q is the elementary charge, h is the Planck constant, k is the Boltzmann constant, T is the absolute temperature, E is the electric field, $\beta = \sqrt{q^3/(\pi \cdot \varepsilon)}$, ε is the dielectric permittivity, μ is the drift mobility, N_C is the conduction band density of states, $q\Phi_T$ is the trap energy level, $q\Phi_{TAT}$ is the barrier height, m_T is the tunnel mass in the dielectric, a is the mean Hopping distance, n is the electron density in the dielectric conduction band, v is the frequency of thermal vibration of electron at trap sites, E_a is the activation energy.

III. Static Device Characterization

Fig. 2 shows characteristic Current Density (J) vs Top to Bottom Electrode Voltage (V) curves for the investigated samples in structures with an area of 100 x 100 μm^2 at 25 °C. OSG3.0 devices show the lowest leakage, due in part to the greater thickness, while Al_2O_3 devices have substantially higher leakage currents, several orders of magnitude greater than both OSG3.0 and SiO_2 devices. It is important to note that the maximum applied voltage in these measurements was constrained by the onset of dielectric breakdown. However, a more fair comparison, from the physics point of view, should be done at the same injection electric field. To this purpose and to investigate the nature of the transport mechanisms in the three classes of devices, we measured (Fig. 3-a) the current density vs. the electric field $E = V/t_{ox}$ (where t_{ox} is the dielectric thickness), for top electron injection ($V < 0$) and bottom electron injection ($V > 0$), at eight different temperatures between 25 °C and 200 °C using a Keysight B1500 Semiconductor Device Parameter Analyzer. It is evident, from Fig. 3-a, that SiO_2 devices show the lower leakage at the same injection field, while Al_2O_3 devices have larger current. Table II summarizes the primary conduction mechanisms explored in the investigated samples and the related symbolism, namely Poole-Frenkel (PF), Hopping and Fowler-Nordheim (FN) [23]. Fig. 3 (b-d) shows the current density as a function of temperature, measured at constant electric field values chosen from regions where current increased monotonically with voltage across all temperatures. While SiO_2 exhibits an increase in J by about two orders of magnitude, suggesting a significant thermionic conduction mechanism contribution, a much lower increase in J is observed for both Al_2O_3 and OSG3.0, suggesting a major role of tunneling. In the following, based on the investigated transport models (Table II), the relevant parameters for the three dielectrics under examination are extracted.

SiO₂ dielectric

For SiO_2, the measured PF β value (see Table II) is very close to the theoretical value (~6) over the entire temperature range, confirming that PF is the dominant conduction mechanism [23]. By using an Arrhenius plot, we extracted the trap energy level (ϕ_T) for SiO_2, that was found to be $\sim 0.77 \pm 0.01$ eV.

OSG3.0 dielectric

For OSG3.0 we could not univocally determine the dominant conduction mechanism, although it appears to be trap-assisted. In fact, the IV vs. T analysis yields realistic parameters whether we assume the anomalous Poole-Frenkel or Hopping as dominant conduction mechanism. Both are bulk-limited and mainly differ in the process driving trap-to-trap transitions, thermionic effect for PF and tunneling for Hopping. The extracted PF β is lower than the theoretical value (~7) across the temperature range and it could be caused by the presence of a large number of traps, comparable to the number of donor sites [24]; this condition is known as anomalous PF. The extracted PF trap energy level ϕ_T for the OSG3.0 film is $\sim 0.44 \pm 0.01$ eV. To investigate whether Hopping is the dominant conduction mechanism, we plotted ln(J) vs. E, to extract the activation Energy (E_a) and the Hopping distance (d) from the slope and intercept, respectively [23]. The extracted values are $E_a = 0.47 \pm 0.02$ eV and $d = 0.6$ nm, that are reasonable for the film under investigation and consistent with the values obtained for the anomalous PF. The other commonly reported mechanism, *i.e.*, Schottky Emission, should be disregarded due to the substantial required energy barrier (≥ 4 eV) [25] at the metal/dielectric interface.

Al₂O₃ dielectric

The extracted β for the 5nm-thick Al_2O_3 film diverges greatly from the theoretical value, clearly indicating that PF is not the dominant conduction mechanism in this case. In particular, the extracted β is consistent with an $\varepsilon_r = 3$ while the actual effective permittivity for the Al_2O_3 film was verified via C-V measurements and found to be equal to 8.9. To verify whether Fowler-Nordheim (FN) is the dominant conduction mechanism, as suggested by the small temperature dependence observed for J in Fig. 3-c, we have extracted the slope ζ from the plot $\ln(J/E^2)$ vs. 1/E, where $\zeta = -8\pi\sqrt{2m^*}\,(q\phi_{TAT})^{\frac{3}{2}}/3qh$, m^* is the electron effective mass, h the Planck's constant and ϕ_{TAT} the injection barrier height. The calculated value for Φ_{TAT} is 1.36 ± 0.02 eV and 1.33 ± 0.01 eV for top and bottom interfaces, respectively. Considering the barrier heights of ~ 2 eV for both the TiN/Al_2O_3 and TaN/Al_2O_3 interfaces ($\Phi_{TiN} = 4.6$ eV [26], $\Phi_{TaN} = 4.65$ eV [27], $\chi_{Al2O3} = 2.58$ eV [28]), the barrier depth values suggest that the current is controlled by Trap-Assisted-Tunneling (TAT) within the Al_2O_3 film (FN-TAT). Indeed, TAT has already been reported in literature as dominant conduction mechanism in defective high-k dielectrics [29, 30]. Moreover, the similar and high energy values obtained for Φ_{TAT} for electron injections from the top and bottom electrodes, indicate the dominant role of deep traps within the dielectric. The small increase in the current density with increasing temperature observed for Al_2O_3 can be attributed to temperature-dependent phonon contributions, which facilitate electronic transport at higher temperatures [31]. These findings highlight the complex nature of charge transport in these dielectrics and underscore the importance of

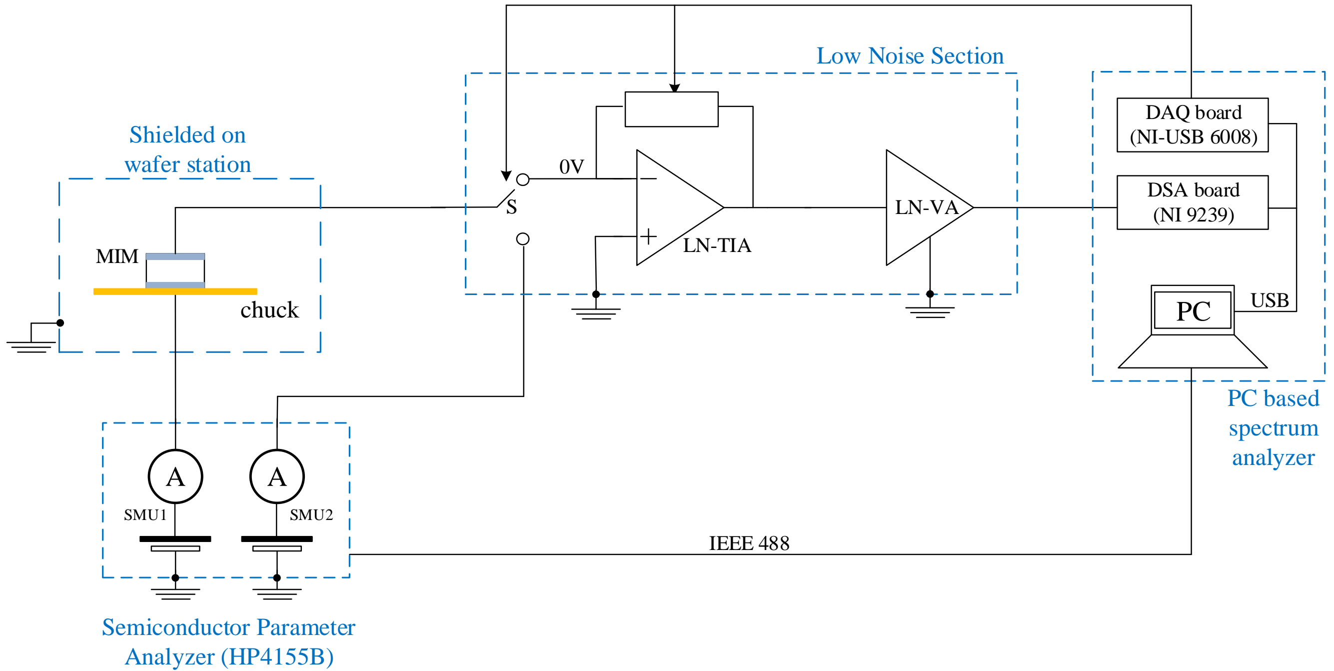

Fig. 4. Simplified schematic of the measurement system for LFNMs. The Bias is applied at the chuck (bottom contact) through a channel (SMU1) of the semiconductor parameter analyzer HP4155B while the noise is measured at the top contact by means of a high sensitivity measurement chain composed of a programmable Low Noise Transimpedance amplifier (LN-TIA) and a cascaded Low Noise Voltage Amplifier (LN-VA). Voltage fluctuations at the LN-VA output are elaborated by a PC based spectrum analyzer. A second HP4155B channel (SMU2) is used to measure the DC current at the top contact prior to the noise measurement.

considering multiple conduction mechanisms when analyzing BEOL materials.

IV. LFNM Setup and Device Characterization

Fig. 4 shows a simplified version of the measurement setup for Low Frequency Noise (LFN) measurements (for a complete description see ref [32]). Samples have a common bottom contact, available at the wafer back, which is accessible by the chuck of the measurement system. As shown in Fig. 4, the bias is applied to the chuck (bottom contact) by a channel (SMU1) of the semiconductor parameter analyzer HP4155B. Crucially, the noise is measured at the top contact by a chain of a programmable low noise transimpedance amplifier (LN-TIA), a low noise voltage gain (LN-VA) stage and a PC based spectrum analyzer equipped with the DSA board NI9239. The front-end LN-TIA has a zero common mode input voltage, due to the virtual short circuit at the LN-TIA input, so that the top contact is held at 0 V. The second voltage gain stage is used to insure sufficient signal-to-noise ratio at the input of the PC based spectrum analyzer. Prior to each noise measurement, we perform a DC current measurement using the HP4155B to check for any device degradation and to select the appropriate feedback impedance for the LN-TIA. The feedback impedance is composed by the parallel of a resistor R_F, to give gain and sufficient signal to noise ratio, and a capacitor, to prevent system instability [32]. The overall feedback capacitance, including the parasitic layout capacitance, is 16 pF while R_F is chosen as the largest value among the set (100 kΩ, 1 MΩ, 10 MΩ, 100 MΩ, 1 GΩ,) that satisfy the non-saturation condition $R_F \cdot I < 1$V (I is the measured DC current). To mitigate the effects of chuck leakage currents (about 10 nA), which can significantly impact low-current measurements, we employ a second HP4155B channel (SMU2) to measure the current at the top contact via a programmable switch (S). This approach allows us to isolate the device current from parasitic leakage paths. It is worth noting that the alternative approach of measuring the noise at the bottom contact (with the bias applied to the top) is not recommended because the LN-TIA input amplifies all interferences captured by the large floating chuck. Moreover, the large chuck capacitance, connected to the low impedance LN-TIA input, can bring the system to an instable behavior. After applying the initial bias through SMU1, we wait 30 seconds while maintaining the bias before starting the noise measurement to minimize the impact of displacement currents. Voltage fluctuations at the output of the LN-VA are sampled by the PC-based spectrum analyzer at a sampling frequency of 5 kHz and the total power spectral density (PSD) is calculated by averaging the PSD of 10 time-windows, each containing 32K points. Twenty-five devices were measured for each dielectric type. The set of applied voltages for top and bottom injection used for the LFN measurements have been chosen based on the IV data in Fig. 2, the lower bound being limited by the system sensitivity and the upper bound set by dielectric breakdown, ensuring the integrity of our devices throughout the measurement process. Fig. 5 (a-c) shows typical measured spectra, in terms of current spectral density S_I (A^2/Hz), for increasing top injection bias (not equally spaced) for the three dielectrics (similar results for bottom injection) in devices with an area of 100 x100 μm^2. At lower frequencies (f), the measured spectra show a clear $1/f^{\gamma}$, while at the higher frequencies the

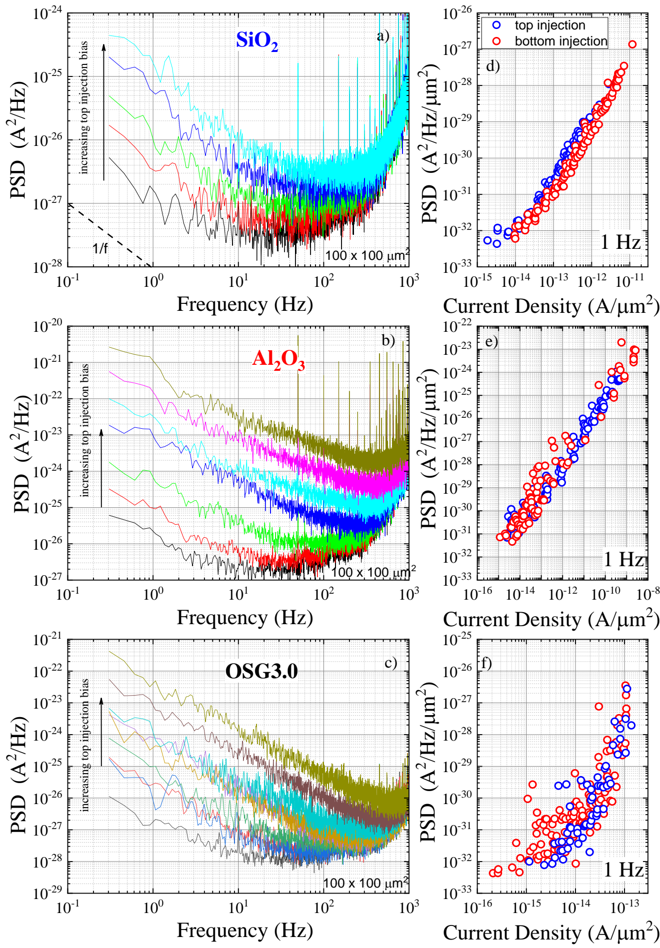

Fig. 5. (a-c) Typical Power Spectral Density S_I as function of the frequency f and for increasing top injection bias for the investigated structures (area A = 100 x100 μm^2); (d-f) S_I/A, evaluated at f = 1 Hz, as function of the current density J (increasing bias) for top (blue symbols) and bottom injection (red symbols) in the investigated structures for different plate area A from 20 x 20 μm^2 to 200 x 200 μm^2.

measured noise increases due to the instrumentation background noise, dominated by the coupling of the low LN-TIA equivalent input voltage noise to the large input capacitance [32]. The input capacitance is mostly due to the connecting cable capacitance (about 200 pF) but a not negligible portion is due to the device capacitance (tens of pF). Measured noise spectra have been fitted between 0.3 Hz and 3 Hz (one decade) resulting in a wide range of measured γ values, from 0 to 1.7. While it is normal to measure γ values different but close to 1 (due to the non uniform trap energy/space trap distribution), γ values significantly different from 1 are the results of Random Telegraph Signal (RTS) events that randomly switch-on. Such "instabilities" have been observed in all OSG3.0 samples, while they are rare for SiO_2 devices. Since, to have a physical meaning, spectra must be the result of stationary events, measurements (or time windows) which resulted in γ values outside the range [0.7 to 1.3] have been discarded. Moreover, the background noise spectra are estimated, for each bias point, based on the device impedance, cable capacitance and equivalent input noise of the measurement system [32]. Measurements for which the signal to noise ratio (device noise by instrumentation noise) was lower

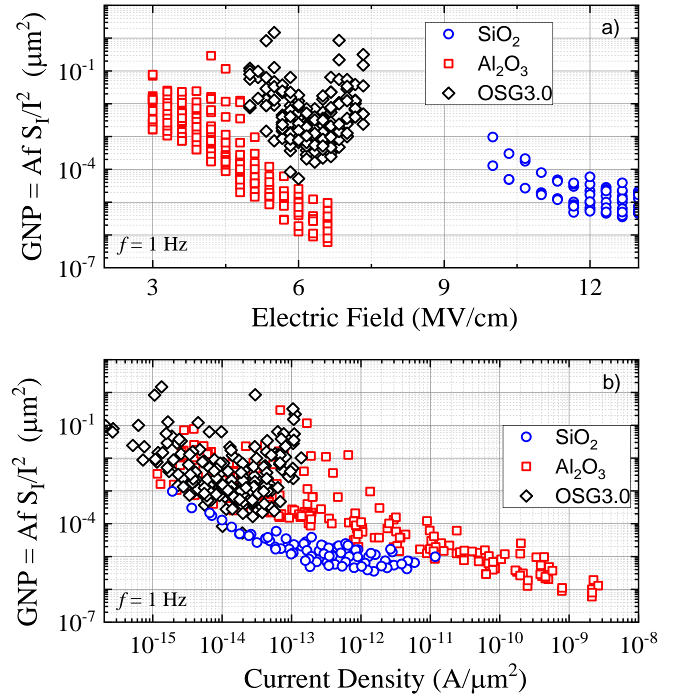

Fig. 6. Overall comparison, in terms of the Gate Noise Parameter (GNP) at f = 1 Hz, of the three investigated MIM structures: a) as function of the electric field; b) as function of the current density.

than a factor 10 at 1Hz have been filtered out. In the following, to support the discussion, we refer to the gate noise model presented in ref [33]

$$S_I = \frac{a^2 I^2 kT\lambda N_t}{Af} \qquad \text{(Eq. 1)}$$

where a is the one electron blocking area, k the Boltzmann's constant, T the absolute temperature, A the device area, $I = JA$ the current, λ is the tunnelling distance and N_t is the effective oxide trap density, assumed constant in space and energy. Because the noise S_I is expected to be proportional to the device area A (in Eq. 1 $I^2 \propto A^2$), Fig. 5 (d-f) shows the scaled noise S_I/A, evaluated at f = 1 Hz, as function of the current density J (increasing bias) for top (blue symbols) and bottom injection (red symbols) in the investigated structures for different plate areas, from 20 x 20 μm^2 to 200 x 200 μm^2. As expected, the noise S_I scales well with the area (A) of the device which is consistent with the bulk limited transport mechanisms obtained from IV measurements. OSG3.0 devices show a larger data dispersion consistent with the instability caused by trapping-detrapping events appearing as non-stationary RTS [31]. Devices with Al_2O_3 dielectric show very similar noise values for top and bottom injection, although the electrodes at the two interfaces are different. This result can be considered a further confirmation of bulk limited transport. Conversely, devices with SiO_2 dielectric which are symmetric in the electrode materials, show a small but clear difference in the noise measured for top and bottom injection. We think that this difference could be a consequence of the manufacturing process; in fact, PELAD SiO_2 low-temperature deposition relies

on O_2-plasma that might result in a top surface reach with O-dangling bonds [34].

The Gate Noise Parameter $GNP = S_I/I^2Af$ is a measure of the trap density (see Eq. 1) useful to compare samples with different geometries or characterized using different biases [19]. Fig. 6 shows the *GNP*, at $f = 1$ Hz, as function of the applied field (a) and of the current density (b) for the investigated samples. It appears evident that in all dielectrics the *GNP* is not constant with the bias, indicating that the energy distribution of the traps is not uniform. As shown in Fig. 6, the *GNP* in devices with Al_2O_3 and SiO_2 decreases with the bias, showing a flattening at the higher bias in the latter case. For OSG3.0 devices instead, the *GNP* seems to have a V shape, with an initial reduction and a subsequent rise as the bias is further increased. We believe that also such a behaviour is caused by the distinct trap distribution responsible for current fluctuations. At the same Electric Field, OSG3.0 devices show a much worse noise behavior (higher *GNP*) with respect to Al_2O_3 samples; a comparison with SiO_2 devices is not possible because of the different bias range used for its characterization. However, from a practical point of view, the comparison should be made at the same leakage current (b). In this case it is evident that the SiO_2 dielectric samples have the lower *GNP*, while Al_2O_3 and OSG3.0 are comparable at low leakage current.

V. Conclusion

In this paper, we have characterized MIM Capacitors with Alumina (Al_2O_3), Silica (SiO_2) and organo-silicate glass (OSG3.0) dielectrics by IV and LFN measurements. Devices with SiO_2 dielectric show the best performances both in terms of static leakage (at equivalent fields) and in terms of noise (at comparable leakage currents). Al_2O_3 devices show the highest leakage and OSG3.0 samples show the worst noise performances associated to a pronounced electrical instability demonstrated by numerous non-stationary RTS events.

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