A 7-bit 150-GSa/s DAC in 5-nm FinFET CMOS

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***Abstract*—We present a 7-bit wireline digital-to-analog converter (DAC), fabricated in 5-nm FinFET CMOS. The number of source-series terminated (SST) cells in the output stage is reduced to 34 by employing cells with relative weight 1 and 4. Each differential cell integrates two single-ended three-stage 8:1 return-to-zero (RZ) multiplexers with an integrated SST driver and a clock pulse generator (CPG), which generates the required clock pulses for the multiplexers from an eight-phase clocking scheme. The clock buffers driving these cells feature shunt inductors to reduce power consumption and jitter. At 150 GSa/s, the effective number of bits (ENOB) was measured to be 4.1 b for a 72.8-GHz sinewave. The DAC consumes 621 mW from a 0.9- and 0.96-V supply. Eye diagrams of 150-GBd NRZ, PAM-4, and PAM-6 are demonstrated, pre-equalized using a 10-tap feedforward equalizer.**

***Index Terms*—Digital-to-analog converter (DAC), FinFET, PAM-4, PAM-6, serializer/deserializer (SerDes), source-series terminated (SST), transmitter, wireline.**

I. Introduction

THE explosive growth of artificial intelligence (AI) and machine learning applications is driving an unprecedented increase in data center traffic. To meet the resulting bandwidth demands, data center interconnects are evolving toward ever-higher throughput, with Ethernet speeds progressing from 800 Gb/s and 1.6 Tb/s today [1] to a projected 3.2 Tb/s by 2030 [2]. These rates are achieved by aggregating multiple high-speed serial lanes. While adding lanes increases total bandwidth, scaling the serial link rate is more desirable, as it improves throughput density and energy efficiency [2].

Current deployments rely on 112 Gb/s (56-GBd PAM-4) serializer/deserializers (SerDes), but the industry is rapidly transitioning toward 224 Gb/s (112-GBd PAM-4) lanes [3]. To support this evolution, SerDes architectures are increasingly adopting DAC- and analog-to-digital converter (ADC)-based designs [3], [4], [5], [6] and digital signal processing (DSP).

Received 15 September 2025; revised 9 December 2025; accepted 5 January 2026. This article was approved by Associate Editor John Wuu. *(Corresponding author: Bart Moeneclaey.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2026.3654029.

Digital Object Identifier 10.1109/JSSC.2026.3654029

The next milestone—400 Gb/s per lane—is highly challenging and demands innovations in both circuit design and signal processing. DAC- and ADC-based designs can support higher-order modulation formats such as PAM-6 and PAM-8 [7], [8], [9], which offer increased spectral efficiency compared to PAM-4, thereby reducing the symbol rate at the cost of increased signal-to-noise ratio (SNR) requirements. These architectures also enable advanced DSP techniques such as maximum likelihood sequence estimation (MLSE), which has been shown to improve SNR by up to 3 dB for 224-Gb/s PAM-4 [10].

Achieving 400 Gb/s per lane requires DACs with significantly higher sample rates and analog bandwidth than today's 112-GSa/s PAM-4 DACs. Depending on the modulation format, the required sample rate increases by a factor of 2 (PAM-4), 1.6 (PAM-6), or 1.33 (PAM-8), assuming similar forward error correction (FEC) overhead. Additional challenges include maintaining low jitter, high ENOB.

This article presents a 7-bit DAC operating at 150 GSa/s in 5-nm FinFET CMOS, employing a three-stage 8:1 multiplexer and a SST driver. The design achieves an ENOB of 4.1 b at 72.8 GHz and demonstrates generation of 150-GBd NRZ, PAM-4 (300 Gb/s), and PAM-6 (375 Gb/s) signaling formats, paving the way toward 400-Gb/s lane rates. Compared to our prior work [11], this invited paper provides a more detailed architectural analysis, expanded circuit-level discussion, and additional experimental results.

The remainder of this article is organized as follows. Section II presents the overall DAC architecture and key design decisions. Section III discusses the 128:8 serializer and associated clocking. The implementation of the high-speed data path is detailed in Section IV, showing clock pulse generation, 8:1 serialization, and the output matching network. Section V describes the employed resonant clocking scheme. Experimental results are presented in Section VI, including the frequency response and ENOB, eye diagrams, and jitter measurement results, as well as static linearity. Finally, Section VII offers a comparison with recent state-of-the-art DACs and concludes the article.

II. DAC Architecture

A. Overview

Fig. 1 shows the block diagram of the DAC operating at a sample rate $f_s = 150$ GSa/s. The DAC output stage is segmented: the 5 least significant bits (LSBs) $B_0, \ldots, B_4$ are

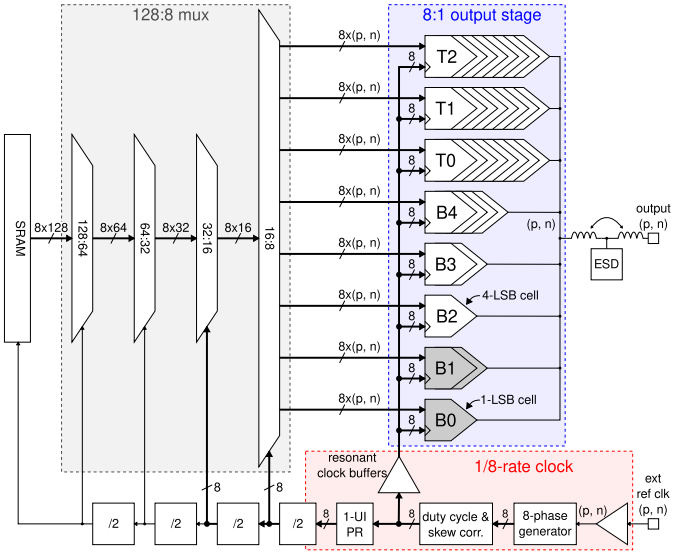


Fig. 1. Prototype DAC architecture block diagram. Signals marked (p,n) are differential.

binary scaled, and the 2 most significant bits (MSBs) are implemented using 3 thermometer bits T_0, T_1, T_2. The binary and thermometer bits of the samples are stored in an on-chip static random access memory (SRAM), generating parallel data at $f_s/128$, which is subsequently multiplexed by the 128:8 mux, producing bit streams at $f_s/8$.

The output stage comprises several cells, each implementing the final 8:1 mux step and a SST driver. Slices B_0 and B_1 are constructed using a single and two parallel 1-LSB cells, respectively. Similarly, the remaining slices $B_2, \ldots, B_4, T_0, T_1, T_2$ make use of one or more parallel 4-LSB cells. The differential outputs of each cell are bundled and connected to the output bumps using a matching network containing a T-coil to absorb the electrostatic (ESD) diode capacitance.

The clock path starts with an external differential clock reference running at $f_s/8$. After buffering, 8 phases are generated using a tapped delay line, wherein each inverter has a tunable delay set by a capacitive bank (coarse tuning). Each of the tap outputs is further delayed and buffered by two inverters with programmable load (fine-tuning). The eight clock phases are subsequently sent to a duty cycle and skew correcting block. These 8 phases branch to resonant clock buffers driving the 8:1 output stage cells, and the clocking of the 128:8 mux. A phase rotator allows adjusting the timing of the data, in steps of 1 unit interval (UI), relative to the output stage clock. The subsequent clock dividers provide the necessary clocks for the 128:8 mux and the $f_s/128$ clock for the memory.

B. Driver

The SST driver and current-mode logic (CML) driver are the two main circuit topologies used in SerDes TX drivers [4]. The basic single-ended SST driver, shown in Fig. 2(a), consists of N multiple identical cells of which the outputs are shorted. The individual digital inputs pull the corresponding node V_y up or down, and the resulting open-circuit output voltage $V_o = V_{\mathrm{DD}} \sum_n b_n/N$ and output resistance $R_{\mathrm{out}} = (R_{\mathrm{on}} + R)/N$,

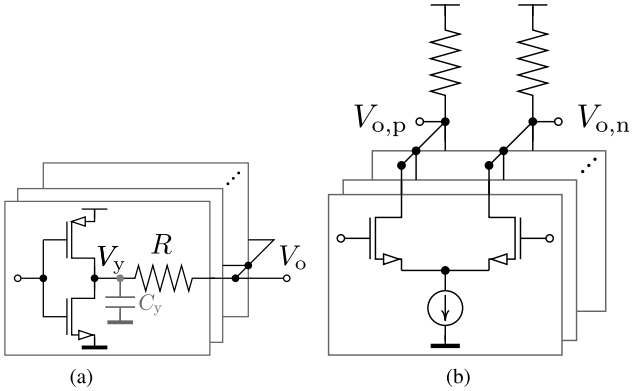


Fig. 2. (a) Basic single-ended SST driver and (b) CML driver.

with V_{DD} the driver supply voltage and R_{on} the transistor ON-resistance. The circuit is straightforward to implement and works seamlessly with preceding CMOS logic [4]. It also provides enhanced ESD robustness because the linearization resistor R attenuates the ESD pulse before reaching the transistors [12]. When loaded with a resistance $R_L = R_{\mathrm{out}}$, typically 50 Ω, the single-ended peak-to-peak output swing equals $V_{\mathrm{DD}}/2$. Because the internal drain voltage V_y goes rail-to-rail, the driver supply voltage cannot be raised beyond the transistor's safe operating voltage V_{max} [13], which ultimately limits the single-ended swing to $V_{\mathrm{max}}/2$. Additionally, achieving a high linearity with an SST driver requires wide driver transistors (their nonlinear ON-resistance R_{on} must be small compared to the linearization resistor R), which in turn leads to a high power consumption [4].

The basic CML driver, shown in Fig. 2(b), consists of multiple cells steering current toward either output $V_{o,p}$ or $V_{o,n}$, both terminated with a resistor. Because the drains are connected directly to the output, CML drivers can support higher single-ended output swings than SST drivers, as demonstrated in [3], [4], but lack the enhanced ESD protection of SST drivers. For the presented DAC, the SST architecture was selected primarily for its implementation simplicity.

Another design choice is the DAC segmentation into cells with varying weights. Using only 1-LSB cells leads to a total of 127 cells, resulting in excessive output parasitics, while implementing each slice with a single cell results in an impractical 1:32 cell weight spread. Making use of two cell variants, weighted 1 LSB and 4 LSB, all slices are constructed by arraying one or more of these cells as illustrated in Fig. 1, resulting in a total of 34 cells. In this design, both cell variants employ the same SST transistor size; only the linearization resistor is scaled to achieve a nominal 4:1 weight ratio. Apart from implementation simplicity, this has the additional benefit that the $R_{\mathrm{on}}C_y$ time constant is the same for both cells when the capacitance C_y on node V_y does not scale proportionally to transistor size. Furthermore, weight tunability was added to each cell to correct deviations due to PVT variation and mismatch.

C. Clocking and Output Stage Serialization

DACs reach high sample rates by making use of multiphase clocks, in which an N-phase clock runs at f_s/N and the

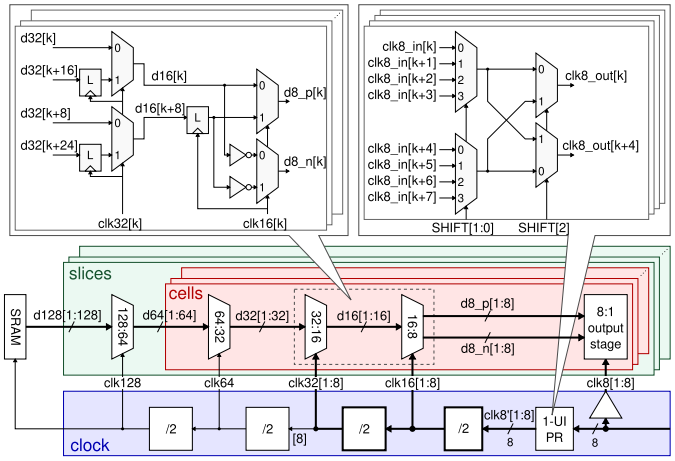


Fig. 3. Block diagram of 128:8 serializer and clock dividers.

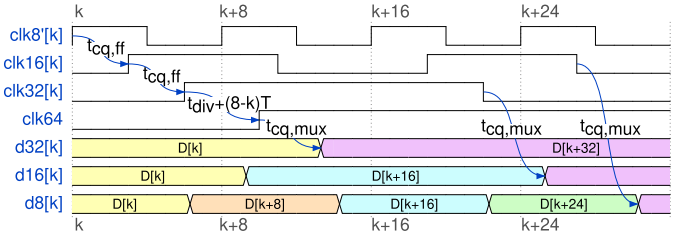


Fig. 4. Timing diagram of the 128:8 serializer and clock dividers.

final serialization step is N:1. Recent high-speed DACs have commonly resorted to four-phase clocking, with only a few adopting eight clock phases [3], [14]. On the one hand, increasing the number of clock phases N reduces the clock frequency, which in turn enables the use of higher-fan-out clock buffers, reducing power consumption [4]. Additionally, clock generation may benefit from a lower clock frequency. On the other hand, increasing N adds more complexity to clock routing and calibration. The bandwidth of the final mux is another hurdle, becoming more severe with increasing N. Eight-phase clocking has been selected for the presented design, resulting in a clock frequency of 18.75 GHz.

III. Low-Speed Serialization and Clocking

The low-speed 128:8 mux and associated clock dividers are detailed in Fig. 3. For each slice, the data path comprises four cascaded 2:1 mux stages, with the last three stages arrayed per cell. The clock path is shared between all slices. Clock buffers were omitted from the figure for clarity.

The output stage requires data inputs d8[1:8] to be staggered in 1-UI steps. To avoid an explicit retiming stage, this staggering is implemented within the preceding 128:8 mux by clocking the 32:16 and 16:8 mux stages with multi-phase divided clocks clk32[1:8] and clk16[1:8], respectively. The multi-phase clk16[1:8] generator is implemented by dividing one of the clk8′ phases and subsequent retiming of the divided clock with clk8′[1:8]. The clocks clk32[1:8] are generated similarly from clk16[1:8]. From clk32[8], a single clk64 is derived, from which a single clk128 is generated. Fig. 4 shows the resulting timing relationship between the various clocks, with $t_{\mathrm{cq,ff}}$ clock-to-output delay of the retiming flip-flops, and t_{div} the clock divider delay.

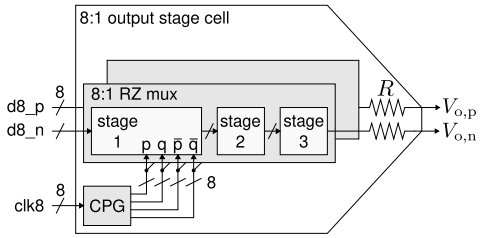


Fig. 5. Output stage differential 8:1 mux cell block diagram.

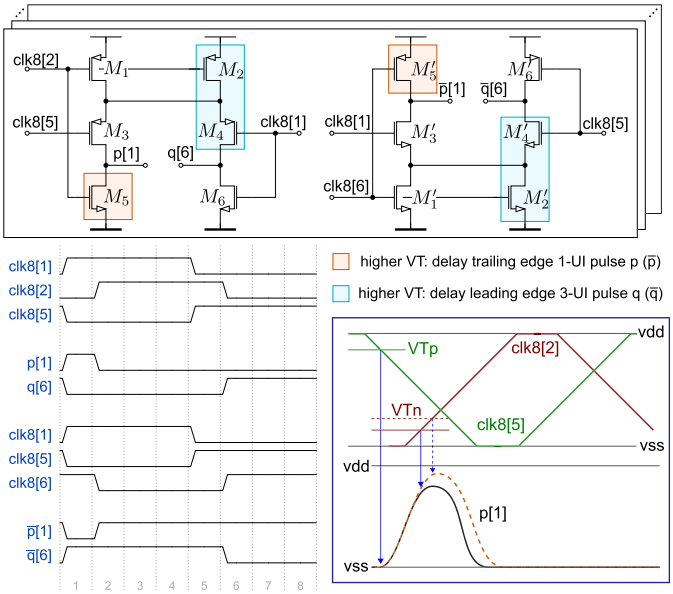


Fig. 6. Clock pulse generator schematics, timing diagram, and 1-UI pulse widening illustration.

The schematic of the 32:16 and 16:8 mux stages is shown in the inset of Fig. 3. Making use of the basic single-latch 2:1 mux cell, eight interleaving channels $k = 1, \ldots, 8$ are clocked with clk32[k] and clk16[k], respectively. The final 16:8 stage includes inverters to generate the complementary output; these are placed ahead of the final 2:1 mux to minimize skew between differential outputs. Fig. 4 shows the timing between various clock and data signals, with $t_{\mathrm{cq,mux}}$ the clock-to-output delay of the 2:1 mux cells.

To align d8 with the output stage clock clk8, a programmable phase rotator circularly shifts all clk8′[1:8] phases by SHIFT = $0, \ldots, 7$ UI, implemented as shown in Fig. 3.

IV. High-Speed Data Path

The output stage consists of several cells, each incorporating 8:1 multiplexing with an SST driver. Fig. 5 shows the block diagram of such a cell. A differential output is generated by employing two single-ended muxes, driven with complementary data inputs. Each cell also includes a CPG, which generates the required pulses for the two single-ended multiplexers from the 8 clock phases.

A. Clock Pulse Generation

Fig. 6 shows the schematic of the CPG, along with the associated timing diagram. From the eight clock phases clk8[1:8]

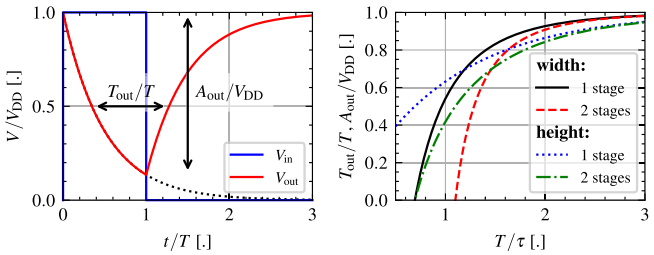


Fig. 7. Illustration of pulse height and width reduction due to bandwidth limitations. (a) Single-stage response to a pulse of width T. (b) Pulse height and width reduction after multiple stages.

with approximately 50% duty cycle, eight 1-UI pulses $p[1{:}8]$ and eight 3-UI pulses $q[1{:}8]$ are generated, as well as their complements $\overline{p}[1{:}8]$ and $\overline{q}[1{:}8]$, respectively. All pulses have an 8-UI period and drive the first stage of the three-stage 8:1 mux.

Due to bandwidth limitations at the CPG output, as well as in the subsequent mux, the 1-UI pulse will not fully reach the supply (ground) before being pulled down (up) again 1 UI later, which results in a pulsewidth (measured at $V_{DD}/2$) less than 1 UI. Pulse narrowing has been demonstrated in [15] by means of simulation, but the following simplified model aids in understanding the effect. Consider an inverting stage which—when the input crosses $V_{DD}/2$—pulls the output high or low with a time constant τ. Applying an input pulse with width T yields an output pulse that has been reduced in height to $A_{out} = V_{DD} \cdot (1 - e^{-T/\tau})$ and narrowed to a width of $T_{out} = T + \ln(1 - e^{-T/\tau}) \cdot \tau$, as illustrated in Fig. 7(a). Applying the same input pulse to a chain of these stages results in the pulse shrinking in height and width increasingly as it progresses through the chain, with the effect more pronounced for smaller T/τ, as shown in Fig. 7(b).

To counteract the pulse narrowing due to a limited bandwidth at the output of the CPG and the mux, transistors M_5 and M_5' have an increased threshold voltage V_T to delay the trailing edge of the 1-UI pulses $p[k]$ and $\overline{p}[k]$. The mechanism is illustrated in the inset: for a trapezoidal clk8 waveform with rise and fall time T_{slew} and a V_T increase of Δ_{VT}, the transition is delayed by $T_{slew} \cdot \Delta_{VT}/V_{DD}$.

As will be discussed in Section IV-B, the mux stages have separate inputs to pull the output high or low. In the first mux stage, the trailing edge of the 1-UI pulse $p[k]$ ($\overline{p}[k]$) will turn off the NMOS (PMOS) pulling the output low (high), whereas the leading edge of the 3-UI pulse $\overline{q}[k+1]$ ($q[k+1]$) will turn on the PMOS (NMOS) pulling the output high (low). To avoid excessive crowbar current in that stage, the leading edge of the 3-UI pulses $q[k]$ and $\overline{q}[k]$ is delayed accordingly. To this end, a higher V_T is selected for M_2 and M_2'. To comply with layout rules, M_4 and M_4' also have a higher V_T.

Finally, the drains of M_1 and M_2 (M_1' and M_2') are shorted. That does not affect the functionality, but it creates a stronger pull-up (pull-down) for both $p[k]$ and $q[k]$ ($\overline{p}[k]$ and $\overline{q}[k]$). In the case of $q[6]$, on the falling edge of clk8[2], both transistors pull up the intermediate node, reducing that output's rise time. Three UI later, on the falling edge of clk8[5], the intermediate node is already pulled up, reducing the rise time of $p[1]$.

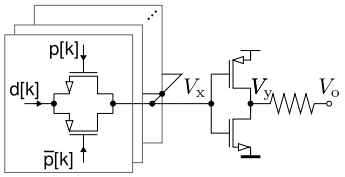


Fig. 8. Transmission gate 8:1 mux driving an SST cell.

B. 8:1 Multiplexer

SST DACs commonly employ a 4:1 transmission gate (TXG) mux to generate the full-rate bit stream driving the SST stage [12], [16]. The presented DAC, however, employs 8-phase clocking and requires an 8:1 mux. In the following, an 8:1 TXG mux implementation is discussed, emphasizing its bandwidth limitations. A new three-stage multiplexer design is then introduced, demonstrating improved bandwidth capabilities. Finally, the performance of both designs is evaluated and compared.

1) Transmission Gate 8:1 Mux: The familiar 4:1 TXG mux architecture is readily modified to support 8:1 muxing, by increasing the number of TXGs from four to eight and supplying pulses $p[1{:}8]$ and $\overline{p}[1{:}8]$ to the NMOS and PMOS gates, respectively, as illustrated in Fig. 8. However, this architecture does not scale well for increasing muxing ratios N:1, due to the capacitive overhead at its output node V_x scaling proportional to N while the drive strength is that of a single TXG, ultimately limiting achievable bandwidth at this node. This is exacerbated by the TXG structure itself: both the NMOS and PMOS transistors contribute to the capacitive overhead, while the NMOS (PMOS) contributes less than its counterpart to the TXG pull-up (pull-down) drive strength. This combination of effects ultimately restricts the achievable bandwidth at the output node, particularly problematic since it carries full-rate data.

2) Three-Stage Return-to-Zero 8:1 Mux: The proposed 8:1 mux overcomes these drawbacks: by adopting a three-stage design, the capacitive overhead on bandwidth-critical nodes is reduced, and by employing RZ signaling, TXGs can be replaced by a single NMOS or PMOS.

Each stage employs the basic block containing two NMOS and two PMOS transistors, with their drains tied together and individually driven gates, shown in Fig. 9. In its simplest form, the NMOS and PMOS sources are connected to the ground and supply, respectively, as shown in Fig. 9(a). To avoid excessive crowbar current, the gate signals should be conditioned such that no NMOS and PMOS are simultaneously activated. Then, the output is pulled low (high) if either NMOS (PMOS) is activated, unless none of the transistors are activated, in which case the previous output is held. Alternatively, the NMOS (PMOS) sources can be connected to data signals: the output is then only pulled low (high) when the corresponding data signal is low (high), resulting in a data-modulated output signal, as illustrated in Fig. 9(b).

Fig. 10 shows the schematic of the proposed 8:1 mux, employing this basic building block in each of its three stages. In the first stage, the gates are driven by the 1-UI and 3-UI pulses originating from the CPG, producing 1-UI pulses with

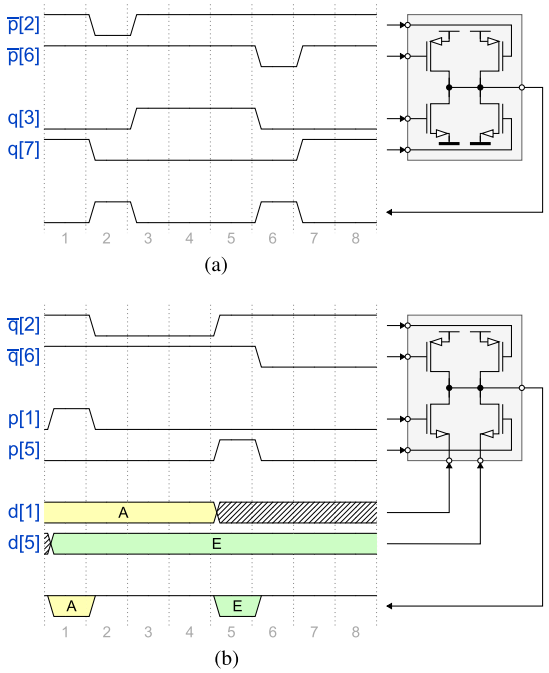


Fig. 9. Example usage of the basic building block used in three-stage RZ mux. (a) Unmodulated. (b) Modulated.

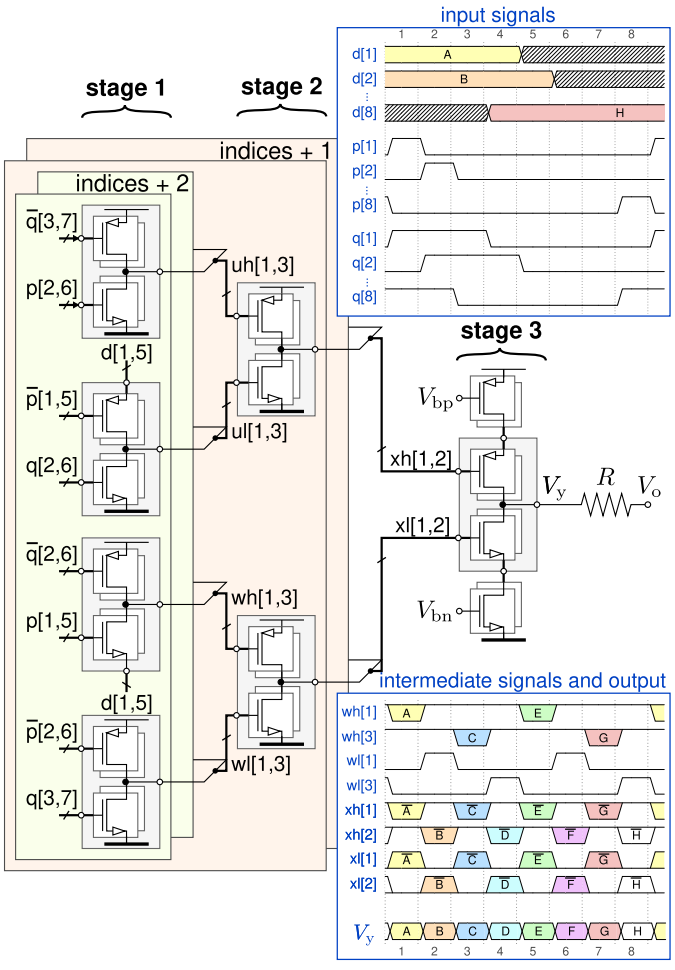


Fig. 10. Schematic of three-stage 8:1 RZ mux and signals.

a 4-UI period. Additionally, for 8 out of 16 first-stage blocks, either the NMOS or PMOS sources are connected to 8-UI

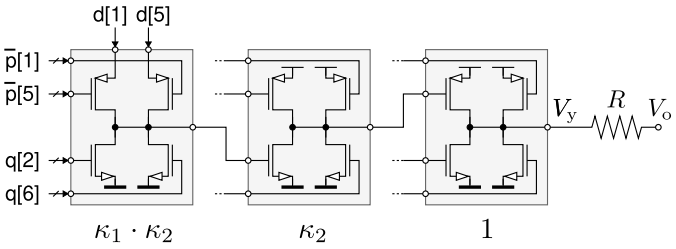


Fig. 11. Sizing of three-stage 8:1 RZ mux.

data, modulating the output pulses. Note that the data streams $d[1{:}8]$, generated by the preceding 128:8 mux, are staggered in 1-UI increments, as shown in the timing diagram in Fig. 10. This is done to avoid retiming in the output stage. Thus, from pulses and data with 8-UI period, the first stage creates pulses and RZ data with a 4-UI (symbol) period. The second stage combines these modulated and unmodulated pulses to produce RZ data with a 2-UI symbol period. Finally, the third final stage merges these signals into a full-rate data stream on V_y. By adding a series resistor at the output of the third stage, it effectively serves as an SST stage.

Additionally, the last stage contains header and footer transistors, controlled by the analog bias voltages V_{bp} and V_{bn}, respectively. For each slice, two on-chip DACs generate V_{bp} and V_{bn}, shared among the constituting cells, to allow tuning the slice weight. The maximal slice weight is obtained for $V_{bn} = V_{DD}$ and $V_{bp} = 0$.

The same building block was used in the final SST stage of [17], implementing 2:1 muxing, and [18], where it performs the final 2:1 muxing step in a 4:1 mux. To the authors' best knowledge, this is the first implementation in which this block is used for multiple stages.

3) Comparison: Fig. 8 shows a simplified circuit diagram of a single-ended 8:1 transmission gate (TXG) mux driving an SST stage. Let the transistors of the SST stage have unit size, and those in the TXG have relative size κ. Equal size for NMOS and PMOS is assumed, as FinFET NMOS/PMOS beta ratio is approximately 1 [8]. The resulting capacitance on the critical node equals $C = 16\kappa c_D + 2c_G$, with c_G and c_D the unit gate and drain capacitances. The mux represents a total capacitive load of $C_{in} = 16\kappa c_G$ to the circuitry generating the 1-UI clock pulses $p[1{:}8]$ and their complement $\overline{p}[1{:}8]$. The drive strength of the transistors is modeled by means of an effective resistance [19], with r the effective resistance of a unit transistor. Due to the abovementioned improved pull-down (pull-up) drive strength of a TXG compared to an NMOS (PMOS), the resulting drive strength of the circuit in Fig. 8 equals $R = r/(\kappa\eta)$, where $1 < \eta < 2$.

Fig. 11 shows a portion of the RZ mux with annotated relative device sizes $\kappa_1 \cdot \kappa_2$, κ_2, and 1 for stage 1, 2, and 3, respectively. By choosing $\kappa_1 = \kappa_2 = \kappa$, the inter-stage nodes have the same time constant $RC = 4rc_D + rc_G/\kappa$. With 4^3 transistors in the first stage, the total capacitive load presented to the clock pulse generators—for a single-ended implementation—equals $C_{in} = 64\kappa^2 c_G$.

For both mux architectures, the calculated 3-dB bandwidth is plotted versus normalized input capacitance C_{in}/c_G in Fig. 12, with $c_D/c_G = 1/4$, $\eta = 4/3$, and $1/(2\pi r c_G) =$

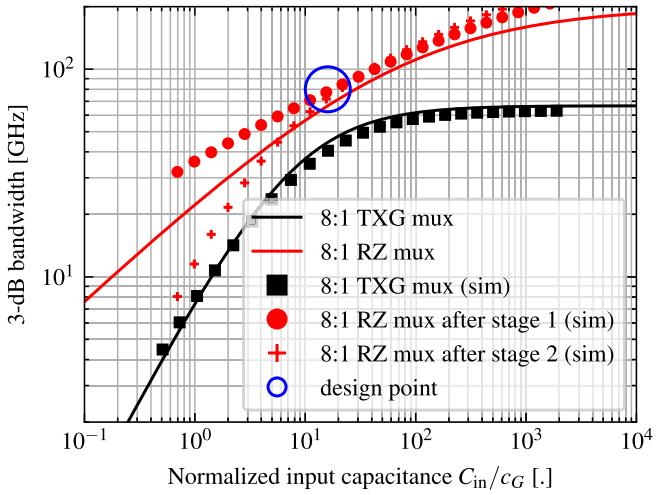


Fig. 12. Simulated and calculated bandwidth versus normalized clock loading for the 8:1 TXG mux and three-stage 8:1 RZ mux.

200 GHz. Additionally, the circuits of Figs. 8 and 11 were replicated in simulation for various values of κ. Static input data, corresponding to a full-rate output 0101… pattern, was supplied using ideal voltage sources as well as the required clock pulses corresponding to a 150-GSa/s sample frequency. The 3-dB bandwidth of each toggling node was calculated from the magnitude of the signal component at $f_s/2$, assuming a rectangular pulse subjected to first-order low-pass filtering. The resulting bandwidth was plotted versus normalized input capacitance in Fig. 12, with $c_G = 2$ fF.

With the selected parameter values, simulation results agree reasonably well with calculated results. Note that, in the case of the RZ mux, when κ is very low, the first stage lacks sufficient bandwidth to deliver adequate swing to the second stage within the 1-UI timeframe of 6.7 ps. As a result, the second-stage effective resistance exceeds the nominal value. Consequently, the second-stage simulated bandwidth is lower than predicted by the simple calculation model.

From both the simulated and calculated results, the bandwidth limitations of the 8:1 TXG mux are evident. For the same clock loading, a higher bandwidth can be achieved using the RZ mux. The selected design point is annotated in Fig. 12, corresponding to $\kappa_1 = \kappa_2 = \kappa = 1/2$ which results in a 3-dB bandwidth of about 75 GHz according to this simplified simulation. In the final design, κ_2 was increased to 2/3 to overcome significant routing parasitics between stages 2 and 3.

While the reduced capacitive overhead on the critical nodes of the RZ mux enables high bandwidths, a high power consumption is required to reach the required bandwidth for 150-GSa/s operation. Moreover, due to a large number of bandwidth-critical nodes, the layout is complex and significantly burdened by routing parasitics.

C. Output Matching Network

Fig. 13(a) shows the layout of the output matching network, containing a differential transmission line section, two

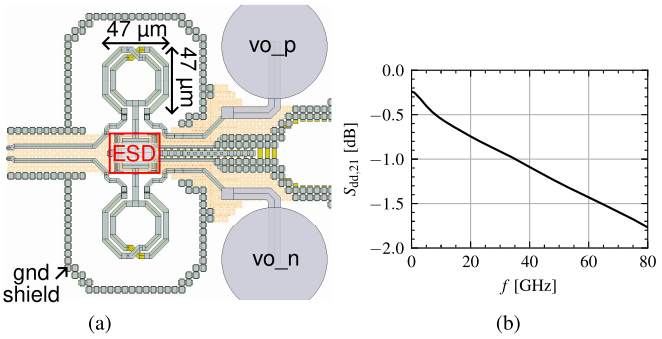


Fig. 13. (a) Output network layout and (b) simulated differential-mode transmission.

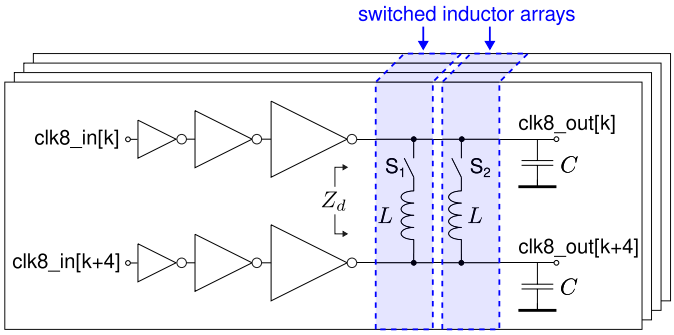


Fig. 14. Resonant clock buffers.

$47\,\mu\text{m} \times 47\,\mu\text{m}$ T-coils, ESD diodes, and the output pads. The ESD diodes have an equivalent capacitance of 90 fF. The T-coils, each with an inductance $L = 65$ pH and coupling coefficient $k = 0.52$, absorb this capacitance at their center tap. The output matching network has a simulated 1.68-dB differential-mode transmission loss at 75 GHz, as shown in Fig. 13(b).

V. Resonant Clocking

Fig. 14 shows a simplified schematic of the clock buffers which drive the output stage cells. These cells represent a significant capacitive load on each clock phase: $C = 1.2$ pF, including interconnect capacitance. To achieve sufficient clock swing with limited power consumption, resonant clocking was employed: a shunt inductor placed in parallel with the capacitive load allows current to circulate in the LC tank, reducing the amount of current that needs to be sourced from the clock buffer [4], [20]. Additional advantages include bandwidth extension and a reduction in jitter originating from the clock buffers or preceding stages, thanks to the bandpass characteristic [4]. To this end, two parallel $L = 240$ pH inductors were placed between each complementary pair of clock phases, yielding a resonance around 19 GHz.

A series switch is placed in the center of each inductor, normally closed for full-rate operation. Since the inductor is driven by complementary clock signals, its center acts as a virtual ground; thus, the parasitic capacitance of the switch does not affect full-rate operation. For lower rates, one or both switches can be opened to lower or remove the resonance frequency, respectively. The resulting differential tank impedance

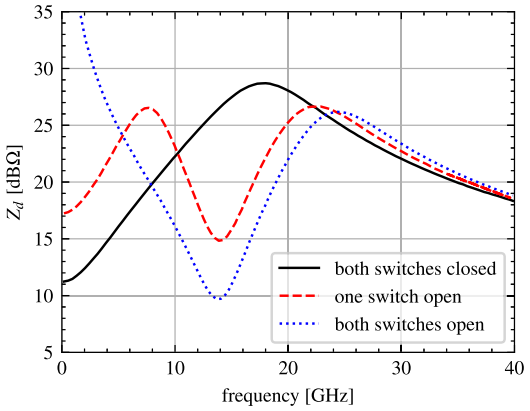


Fig. 15. Simulated loaded tank impedance versus frequency.

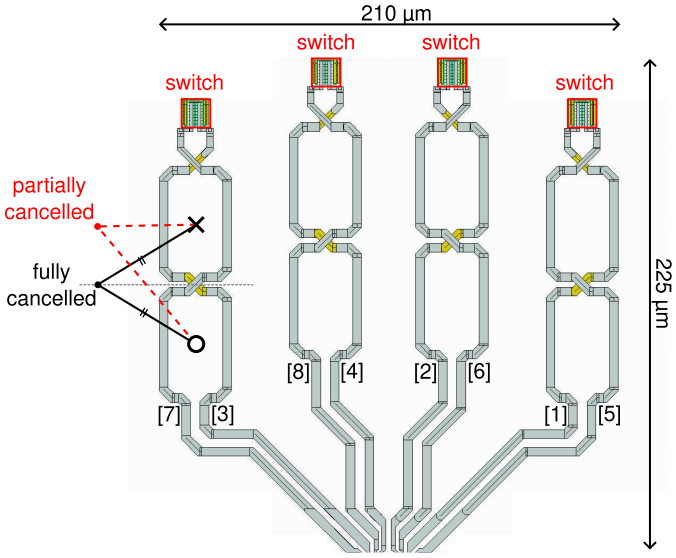


Fig. 16. Layout of the switched inductor array, with Fig. 8 inductor (partial) magnetic field cancellation illustrated.

$Z_d(f)$, simulated including post-layout parasitics, is shown in Fig. 15. The Q-factor equals 2.0 when both switches are closed and 1.8 when one switch is opened. The dominant contribution to this damping is parasitic interconnect resistance, not the switch on-resistance R_{sw} = 1.75 Ω nor the inductor series resistance.

The switched inductors are organized into two identical arrays, which were symmetrically placed to the north and south of the output stage. Fig. 16 shows the switched inductor array, taking up an area of 210 μm × 225 μm, with the corresponding clk8 phases marked and the switches highlighted. To minimize the overall footprint, inductors associated with different clock phases were placed in close proximity. However, this compact arrangement introduces non-negligible magnetic coupling between adjacent inductors, inducing phase and amplitude offsets in neighboring clock signals. These distortions manifest as interleaving spurs at the output and necessitate clk8 skew correction. To mitigate crosstalk, the inductors are drawn in a Fig. 8 pattern. Due to the opposing current flow within the two turns, the resulting magnetic fields (partially) cancel, reducing coupling between adjacent inductors [21], [22], as illustrated in Fig. 16.

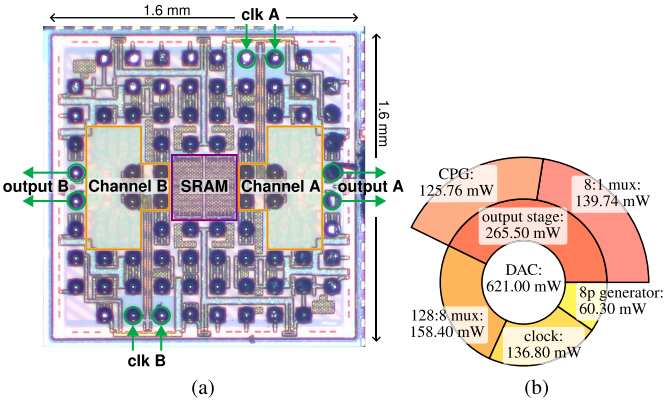


Fig. 17. (a) Micrograph of the prototype die containing two DAC channels and (b) single DAC channel power consumption breakdown.

VI. Experimental Results

A. Prototype and Measurement Setup

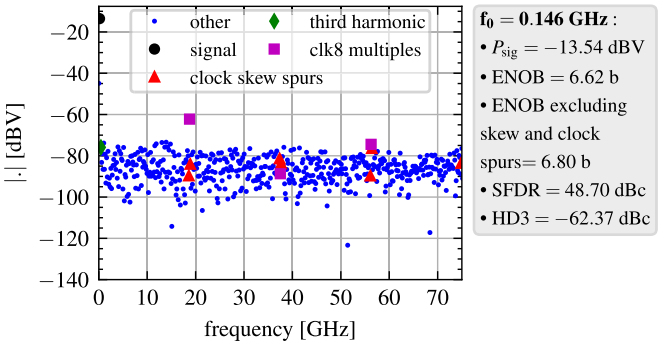
The DAC was fabricated in a 5-nm FinFET process and flip-chipped on an interposer on which the clock inputs and high-speed outputs lead to RF probe pads. The fabricated prototype die, consisting of two DAC channels, is photographed in Fig. 17(a). The die size is 1.6 mm × 1.6 mm. Excluding memory, a single DAC channel occupies 0.23 mm^2 and consumes 621 mW from a 0.9- and 0.96-V supply. Fig. 17(b) presents the DAC power consumption breakdown.

An external 18.75-GHz clock reference was applied using a balun to the probed differential DAC reference clock input, resulting in f_s = 150 GSa/s. The differential DAC output probe was connected via dc blocks to the remote heads of a sampling oscilloscope. The losses of the interposer traces, RF probe, cable, and dc blocks, connecting the DAC output to the remote heads, were measured and de-embedded in oscilloscope software. Foreground calibration was employed, wherein the DAC generated multi-tone stimuli, the differential output voltage was captured, and the clock skews and duty cycles were corrected using an iterative least-squares algorithm.

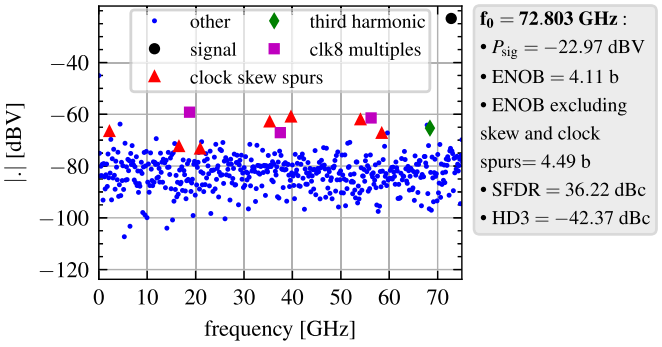
B. Sinewave Spectrum

To evaluate the DAC amplitude response and ENOB, sinewaves of various frequencies f_0 were generated. For each frequency, a pattern of N = 1024 samples was stored in on-chip memory and repeatedly applied to the DAC. Coherent sampling was employed: $f_0 = (M/N)f_s$ was selected, with M odd [23]. The oscilloscope waveform corresponding to the de-embedded differential DAC output voltage was transformed into the frequency domain, from which the signal power and the combined power of noise and distortion up to the Nyquist frequency $f_s/2$ were calculated.

Fig. 18 details the spectra for a sinewave with the lowest (0.15 GHz) and highest (72.8 GHz) applied frequency with corresponding ENOB of 6.62 b and 4.11 b, respectively. Spurs at multiples of the clk8 frequency ($f = mf_s/8$), skew spurs ($f = mf_s/8 \pm f_0$), as well as the third harmonic ($f = 3f_0$ or $f = f_s \pm 3\ f_0$) are discerned. Combining the results of



(a) signal frequency $f_0 = 0.15$ GHz



(b) signal frequency $f_0 = 72.8$ GHz

Fig. 18. Measured spectra for a sine with (a) f_0 = 0.15 GHz and (b) f_0 = 72.8 GHz.

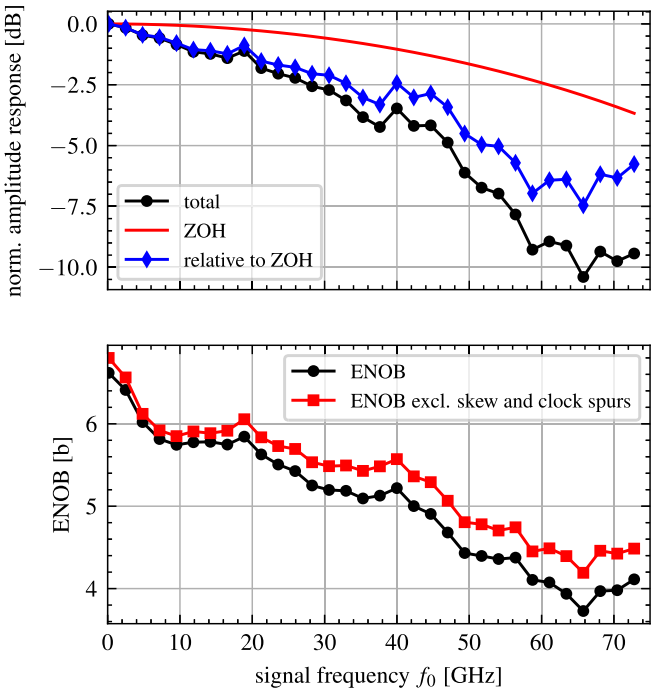
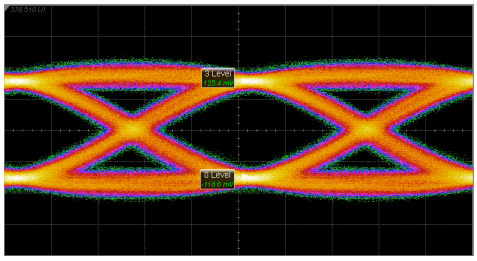
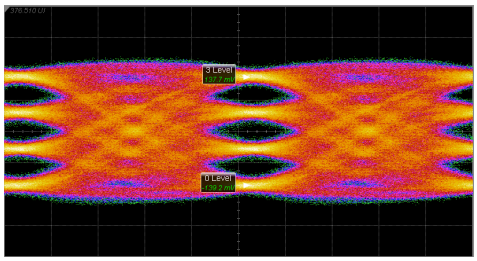


Fig. 19. Measured DAC amplitude response (top) and ENOB (bottom) versus signal frequency f_0.

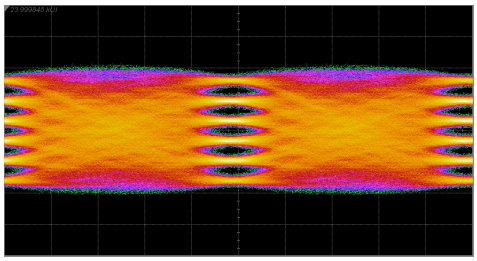
the generated sinewaves leads to Fig. 19 showing the DAC amplitude response and ENOB versus signal frequency f_0. The amplitude response is subdivided into a zero-order hold (ZOH) response $H(f_0) = \text{sinc}(f_0/f_s)$ and additional loss. Relative to



(a)

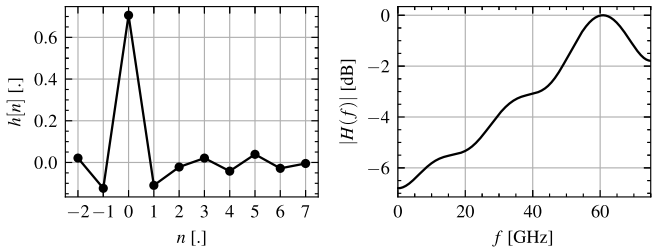


(b)



(c)

Fig. 20. Captured 150-GBd (a) NRZ, (b) PAM-4, and (c) PAM-6 with pre-equalization and fixture de-embedding. Vertical scale is 80 mV/div.



(a) (b)

Fig. 21. Applied 10-tap symbol-spaced equalizer: (a) impulse response $h[n]$ = [0.021, 0.124, 0.706, −0.110, −0.022, 0.021, −0.042, 0.039, −0.028, −0.005] and (b) frequency response $H(f)$.

the low-frequency amplitude ($V_{od,pp}$ = 594 mV), the highest applied frequency f_0 = 72.8 GHz incurs a loss of 9.43 dB: 3.67 dB from ZOH response and 5.76 dB of additional loss. The ENOB when excluding the power of the skew spurs and clk8 multiples is plotted as well: at the highest applied signal frequency f_0 = 72.8 GHz, the ENOB degrades from 4.49 b to 4.11 b due to skew and spurs.

C. Eye Diagrams

Fig. 20 shows eye diagrams for 150-GBd PRBS11 NRZ, PAM-4, and PAM-6, which were pre-equalized by applying in software a 10-tap symbol-spaced equalizer to the samples

TABLE I
COMPARISON WITH STATE-OF-THE-ART PAM-4 DACS

	[14]	[24]	[25]	[5]	[3]	[6]	[12]	**This work**
Technology	5 nm	10 nm	28 nm	3 nm	3 nm	5 nm	4 nm	**5 nm**
Driver architecture	CML & post-amp	CML	CML	CML	CML	CML & post-amp	SST	**SST**
Sample rate [GSa/s]	160	112	100	112	112	106.25	72	**150**
Power supply [V]	0.6/0.94/1.2/1.8	0.85/1/1.5	N/A	0.75/0.9/1.2	0.75/1.1/1.5	0.65/0.94/1.2	0.95	**0.9/0.96**
PAM-4 bit rate [Gb/s]	279.2	224	200	224	224	212.5	144	**300**
Power efficiency [pJ/b]	0.90	1.88	4.63	0.92	1.00	1.33	2.00	**2.07**
Equalized eye swing [mVpp]	650	900*	300*	700*	960	780	410*	**277**
Core area [mm^2]	0.59†	0.088	0.30	0.1	0.1	0.28	0.047	**0.23**

*estimated from eye diagram
†estimated from die micrograph

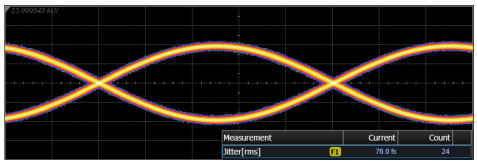
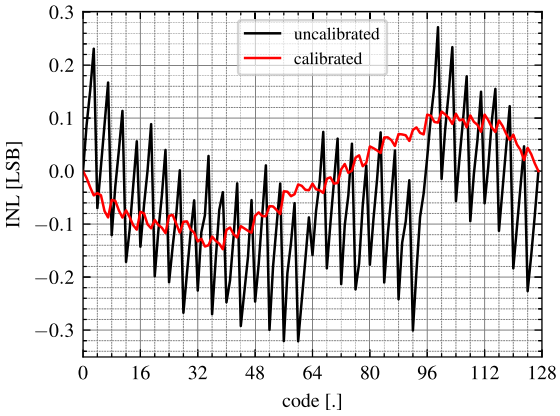
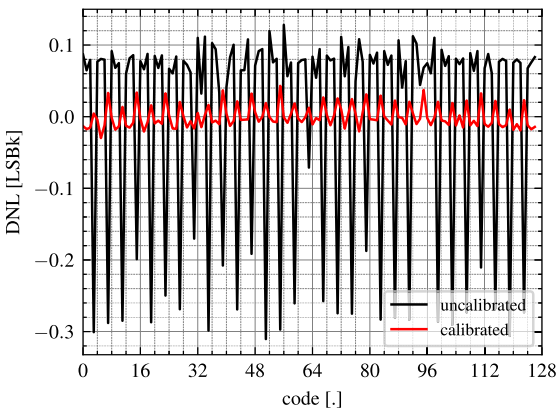


Fig. 22. Measured jitter generating an $f_s/2$ = 75-GHz tone, showing 76-fs rms jitter.



(a)



(b)

Fig. 23. Static linearity measurements: (a) INL and (b) DNL.

stored in the on-chip memory. A voltage difference between the highest and lowest level of 244.0 and 276.9 mV is reported for NRZ and PAM-4, respectively. Fig. 21(a) and (b) shows the impulse response and frequency response of the equalizer.

The random jitter on a $f_s/2$ = 75-GHz clock signal generated by the DAC was measured on the oscilloscope as 76-fs rms, as shown in Fig. 22.

D. Static Linearity

Static linearity measurements were performed by connecting the DAC outputs to a 100Ω differential load, and measuring the differential dc output voltage for static codes 0 to 127. Fig. 23 reports static linearity measurements, showing an integral nonlinearity (INL) between −0.32 LSB and 0.27 LSB and a differential nonlinearity (DNL) between −0.31 LSB and 0.13 LSB without calibrating the cell weights. After correcting the weights of each of the five LSB and three MSB slices by adjusting the corresponding bias voltages V_{bn} and V_{bp}, the INL improves to between −0.15 LSB and 0.11 LSB and the DNL ranges between −0.03 LSB and 0.04 LSB.

VII. CONCLUSION

A 7-bit wireline 150-GSaps DAC, fabricated in 5-nm FinFET CMOS, was presented. It employs eight-phase clocking and the output stage cells contain CPGs, a three-stage 8:1 RZ mux and an SST driver. The clock buffers driving these cells feature shunt inductors to reduce power consumption and jitter.

Table I compares the performance of the presented DAC with state-of-the-art high-speed PAM-4 DACs. The proposed design achieves a sample rate of 150 GSa/s—second only to the 160 GSa/s reported in [14]—and demonstrates the highest PAM-4 transmission rate at 300 Gb/s. However, the equalized eye swing of 277 mV_{pp} is the lowest among the compared designs, reflecting the swing limitations of the SST architecture and the signal loss at 150 GHz. While most CML-based DACs are more energy efficient, this work pushes the sample rate significantly beyond the 72-GSa/s limit of prior SST-based designs [12], while maintaining a comparable energy efficiency of 2.07 pJ/b. The DAC has demonstrated its capability across 150-GBd NRZ, PAM-4 (300 Gb/s), and PAM-6 (375 Gb/s) signaling formats, paving the way toward 400-Gb/s lane rates.

ACKNOWLEDGMENT

The authors acknowledged TSMC for chip fabrication, J. Aravind and S. Zagrocki for layout support, H. Suys,

D. Santolaya, and J. Schelkens for PCB and interposer design, N. Singh, S. Niu, and A. Vandierendonck for support with the measurements.

REFERENCES

[1] *IEEE P802.3Dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force*. Accessed: Sep. 12, 2025. [Online]. Available: https://www.ieee802.org/3/dj/index.html

[2] P. Ossieur et al., "Integrated photonics and electronics for optical transceivers supporting AI/ML applications," *IEEE J. Select. Topics Quantum Electron.*, pp. 1–18. [Online]. Available: https://ieeexplore.ieee.org/document/10876612/

[3] D. Pfaff et al., "A 224 Gb/s 3 pJ/bit 40 dB insertion loss transceiver in 3-nm FinFET CMOS," *IEEE J. Solid-State Circuits*, vol. 60, no. 1, pp. 9–22, Jan. 2025. [Online]. Available: https://ieeexplore.ieee.org/document/10716779/

[4] J. Kim et al., "A 224-Gb/s DAC-based PAM-4 quarter-rate transmitter with 8-tap FFE in 10-nm FinFET," *IEEE J. Solid-State Circuits*, vol. 57, no. 1, pp. 6–20, Jan. 2021. [Online]. Available: https://ieeexplore.ieee.org/document/9537159/

[5] M. Cusmai et al., "A 0.92-pJ/b PAM-4 and 0.61-pJ/b PAM-6 224-Gb/s DAC-based transmitter in 3-nm FinFET," *IEEE J. Solid-State Circuits*, vol. 60, no. 1, pp. 23–34, Jan. 2025. [Online]. Available: https://ieeexplore.ieee.org/document/10684878/

[6] J. Q. Wang et al., "7.1 a 2.69 pJ/b 212 Gb/s DSP-based PAM-4 transceiver for optical direct-detect application in 5 nm FinFET," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2024, pp. 123–125. [Online]. Available: https://ieeexplore.ieee.org/document/10454275/

[7] F. O'Mahony. *Scaling SerDes Beyond 100 Gb/s in Advanced CMOS Technologies*. Accessed: Sep. 14, 2025. [Online]. Available: https://resourcecenter.sscs.ieee.org/education/webinars/sscsweb4040

[8] J. E. Proesel. *High-Speed and Mixed-Signal Circuit Design Techniques in FinFET Technology for Wireline and Optical Interface Applications*. Accessed: Sep. 14, 2025. [Online]. Available: https://resourcecenter.sscs.ieee.org/education/short-courses/sscs2020sc0021

[9] T. Dickson et al., "Digital-to-analog converters for 100 + Gb/s wireline transmitters: Architectures, circuits, and calibration," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, France, Apr. 2024, pp. 1–8. [Online]. Available: https://ieeexplore.ieee.org/document/10528971/

[10] T. Ali et al., "F1: Transceivers for exascale: Towards Tbps/mm and sub-pJ/bit," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2023, pp. 519–521. https://ieeexplore.ieee.org/document/10067791/

[11] B. Moeneclaey et al., "A 7-bit 150-GSa/s DAC in 5 nm FinFET CMOS," in *Proc. Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2025, pp. 1–3. [Online]. Available: https://ieeexplore.ieee.org/document/11075168/

[12] T. O. Dickson et al., "A 72-GS/s, 8-bit DAC-based wireline transmitter in 4-nm FinFET CMOS for 200 + Gb/s serial links," *IEEE J. Solid-State Circuits*, vol. 58, no. 4, pp. 1074–1086, Apr. 2022. [Online]. Available: https://ieeexplore.ieee.org/document/9997502/

[13] E. Groen et al., "10-to-112-Gb/s DSP-DAC-based transmitter in 7-nm FinFET with flex clocking architecture," *IEEE J. Solid-State Circuits*, vol. 56, no. 1, pp. 30–42, Jan. 2020. [Online]. Available: https://ieeexplore.ieee.org/document/9272325/

[14] F. Ahmad et al., "An 8b 160 GS/s 57 GHz bandwidth time-interleaved DAC and driver-based transmitter with adaptive calibration for 800 Gb/s coherent optical applications in 5 nm," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2024, pp. 342–344. [Online]. Available: https://ieeexplore.ieee.org/document/10454480/

[15] D. Seebacher, "Predistortion of digital RF PWM signals considering conditional memory," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 62, no. 9, pp. 2342–2350, Sep. 2015. [Online]. Available: https://ieeexplore.ieee.org/document/7214321/

[16] M. A. Kossel et al., "An 8b DAC-based SST TX using metal gate resistors with 1.4pJ/b efficiency at 112Gb/s PAM-4 and 8-tap FFE in 7 nm CMOS," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, vol. 64, France, Feb. 2021, pp. 130–132. [Online]. Available: https://ieeexplore.ieee.org/document/9365784/

[17] M. Pisati et al., "A sub-250 mW 1-to-56 Gb/s continuous-range PAM-4 42.5 dB IL ADC/DAC-based transceiver in 7 nm FinFET," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 116–118. [Online]. Available: https://ieeexplore.ieee.org/document/8662428/

[18] A. Chowdhury et al., "A 0.9 pj/b 9.8–113 Gb/s XSR SerDes with 6-tap TX FFE and AC coupling RX in 3 nm FinFet technology," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, Jun. 2024, pp. 1–2.

[19] N. H. E. Weste and D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed., Reading, MA, USA: Addison-Wesley, 2011.

[20] P. Restle, "Processor clock generation, distribution, and clock sensor/management loops," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Sep. 2021, pp. 1–166.

[21] N. M. Neihart, D. J. Allstot, M. Miller, and P. Rakers, "Twisted inductors for low coupling mixed-signal and RF applications," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2008, pp. 575–578. [Online]. Available: https://ieeexplore.ieee.org/document/4672150/

[22] P. Guan et al., "8-shaped inductors: An essential addition to RFIC designers' toolbox," *IEEE Open J. Solid-State Circuits Soc.*, vol. 4, pp. 131–146, 2024. [Online]. Available: https://ieeexplore.ieee.org/document/10668829/

[23] *IEEE Standard for Terminology and Test Methods of Digital-to-Analog Converter Devices*. Accessed: Aug. 7, 2020. [Online]. Available: https://ieeexplore.ieee.org/document/6152113/

[24] J. Kim et al., "A 224 Gb/s DAC-based PAM-4 transmitter with 8-tap FFE in 10 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Sep. 2021, pp. 126–128. [Online]. Available: https://ieeexplore.ieee.org/document/9365840/

[25] M. Choi et al., "8 an output-bandwidth-optimized 200 Gb/s PAM-4 100 Gb/s NRZ transmitter with 5-tap FFE in 28 nm CMOS," in *Proc. IEEE Int. Solid- State Circuits Conf. (ISSCC)*, vol. 64, Feb. 2021, pp. 128–130. [Online]. Available: https://ieeexplore.ieee.org/document/9366012/

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Dr. Yin is a member of the ECOC and Optica APC Technical Program Committee (TPC). He has led a team including international researchers from imec, Bell Labs USA/Alcatel-Lucent, and Orange Labs France, which won the GreenTouch 1000x Award in recognition of the invention of the Bi-PON protocol and sustained leadership.

Ewout Martens (Member, IEEE) received the M.Sc. degree in electronic engineering and the Ph.D. degree (summa cum laude) from Katholieke Universiteit Leuven, Leuven, Belgium, in 2001 and 2007. His research is focused on modeling techniques for Delta–Sigma modulators and RF front ends.

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Jan Craninckx (Fellow, IEEE) received the M.S. and Ph.D. degrees (summa cum laude) in microelectronics from the ESAT-MICAS Laboratories, KU Leuven, Leuven, Belgium, in 1992 and 1997, respectively. His Ph.D. work was on the design of low-phase noise CMOS integrated VCOs and PLLs for frequency synthesis.

From 1997 to 2002, he worked with Alcatel Microelectronics (later part of STMicroelectronics) as a Senior RF Engineer on the integration of RF transceivers for GSM, DECT, Bluetooth, and WLAN. In 2002, he joined imec, Leuven, Belgium, as the Principal Scientist working on RF, analog, and mixed-signal circuit design. He is currently with imec. He has authored and co-authored more than 200 papers, book chapters, and patents. His research focuses on the design of RF transceiver front ends in nanoscale CMOS, covering all aspects of RF, mm-wave, analog, and data converter design.

Dr. Craninckx is/was a regular member of the Technical Program Committee for several SSCS conferences, was the Chair of the SSCS Benelux chapter from 2006 to 2011, an SSCS Distinguished Lecturer from 2012 to 2013, and an elected SSCS AdCom member from 2017 to 2019. He was a co-recipient of the ISSCC 2015 Jan Van Vessem Award and the ISSCC 2019 Lewis Winner Award. He was an Associate Editor from 2009 to 2016 and the Editor-in-Chief from 2016 to 2019 of IEEE JOURNAL OF SOLID-STATE CIRCUITS.

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Dr. Ossieur was a member of the Technical Program Committee of the European Conference on Optical Communications (ECOC) and is a member of the Wireline Subcommittee of the International Solid-State Circuits Conference (ISSCC).