High-resolution Scanning Spreading Resistance Microscopy (SSRM) for carrier mapping in nanoscale gate-all-around (GAA) transistors

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For decades, transistor scaling enabled increasing the number of devices on a chip and thus complying with the growing compute and memory requirements of advancing technologies. As transistors reach nanometer scale dimensions, transistor short-channel effects are an obstacle to the efficient control of electrical carriers, leading to leakage currents and performance degradation. For this reason, precise control of the carrier distribution through dopant engineering at the channel junction has become critical in modern integrated circuits.

Scanning Spreading Resistance Microscopy (SSRM) is an AFM-based technique considered as the standard approach for mapping electrical carriers in 3D structures [1]. However, as the industry moves to scaled gate-all-around (GAA) transistor architectures, SSRM faces unprecedented obstacles. The heterogeneity of materials in exposed cross-sections induces surface roughness that degrades spatial resolution, while the proximity of high-conductivity metal to very thin, high-resistive silicon requires an amplifier fast enough to handle large current variations during scanning. Although SSRM has been demonstrated on devices at relaxed dimensions with channel length of 50 nm and thickness of 10nm [2], transistors for sub-2 nm nodes have target channel lengths under 14 nm and thicknesses under 6 nm [3], making the improvement of the spatial resolution of SSRM a necessity.

In this work, we present how our development of the SSRM technique, ranging from sample preparation, new current amplifier, and new dedicated AFM probes, allows us to map the carriers in GAA Nanosheet-based transistors (NSFETs) with gate pitch of 45 nm, gate length of 12 nm and channel thickness of 5 nm. This advancement enables us to capture the influence of different thermal budgets on dopant diffusion inside the devices. Samples with different processing conditions are analysed and compared to process and device simulations to demonstrate the new capabilities of SSRM in mapping carriers in GAA transistors with channels four times smaller than ever measured before.

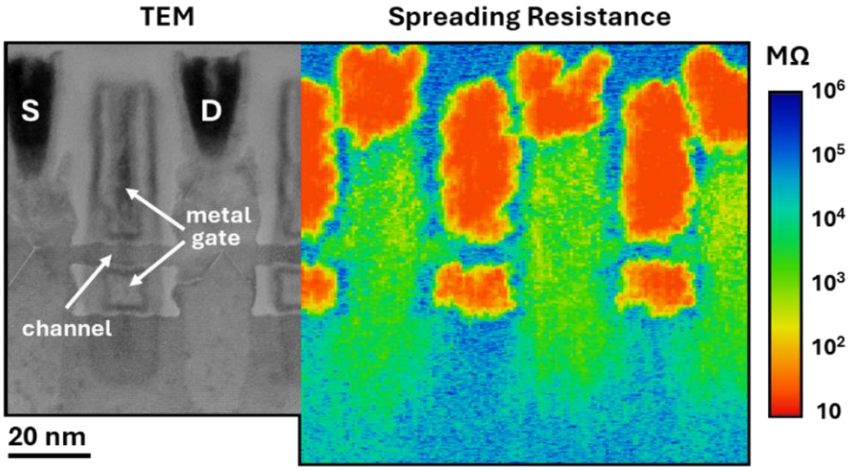

Figure 1 : Adjacent Transmission Electron Microscopy (TEM) image (left) and Scanning Spreading Resistance Microscopy (SSRM) map (right) of 45 nm gate-pitch gate-all-around (GAA) Nanosheet-based transistors (NSFET). The spreading resistance data shows how carriers diffuse from source-drain regions inside the channel and below the metal gate.

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